MASTER THESIS

REPORT:

Designing an understandably Simple and Secure Smartphone: Designing the MEGAphone PCB schematic

Topic Number and Name:

ENGR9700 A-D MASTER THESIS

Semester and Year:

Semester 2 – 2017

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Date of Report Submitted:

16/10/2017

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Declaration

I certify that this work does not incorporate without acknowledgment any material previously submitted for a degree or diploma in any university; and that to the best of my knowledge and belief it does not contain any material previously published or written by another person except where due reference is made in the text.

Name: Mr Karthik Srinivasa Puranik Date: 16th October 2017

Acknowledgments

I would like to express gratitude to my Project supervisor Dr. Paul Gardner – Stephen for his invaluable input in producing this report. Also, I would like to thank Mr. Bejamin Gerblich for his timely input in interpreting this design. Last but not the least, I would like to thank my family and friends for always being supportive.

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List of Abbreviations and Symbols

ADC: Analog to Digital Converter

CMOS: Complementary Metal Oxide Semiconductor

CPU: Central Processing Unit

C65: Commodore65

FDD: Frequency Division Duplexing

FPGA: Field Programmable Gate Array

GPIO: General Purpose Input Output

GPS: Global Positioning System

GPU: Graphics Processing Unit

IPS: In-Plane Switching

IC: Integrated Circuit

I2C: Inter Integrated Circuit

LTE: Long Term Evolution

LiFePO4: Lithium Iron Phosphate

OTG: On the Go

PCB: Printed Circuit Board

RAM: Random Access Memory

RGB: Red Green Blue

SD: Secure Digital

SIM: Subscriber Identity Module

SoC: System on Chip

SPI: Serial Peripheral Interface

TDD: Time Division Duplexing

TFT: Thin Film Transistor

UART: Universal Asynchronous Receiver/ Transmitter

UV: Ultra - Violet

GHz: Giga Hertz

mAh: milli-ampere hour

V: Volt

dBm: decibel-mill watts

Ω: Ohm

bps: bits per second

mA: milli-ampere

ABSTRACT

The modern Smartphone design are quite complex. The complexity of design in terms of tight integration of all the functional modules that are collectively responsible for the Smartphone functioning. Due to this tight integration of functional modules, the normal Smartphone users are unable to interpret the entirety of the design. This leads to security issue as the design is not understandable. Furthermore, this complex design has not been much user friendly as it has increased the booting time. The main aim of this project lies in deriving a simple and secured design of Smartphone which provides the precise understandability to the user. As, a result, the user can be aware of hardware and software functioning involved in the functioning of the Smartphone.

The initial design consideration for this project was employing the modular phones as platform. The detailed discussion regarding the modular phones has been included in the later section of the report. Considering the Fairphone 2 (modular phone) as platform for wider secure mobile computing efforts within the mobile telecommunication laboratory and this involved designing and performing the rudimentary functional testing for replacement of main board for Fairphone 2. Basically, the plan was to replace the existing main PCB of the Fairphone 2 with new PCB incorporating an FPGA, small external memory and cellular radio which leads to the interest of creating an FPGA based Smartphone platform. But, in the way of doing so, liaising with the Fairphone 2 manufacturers were necessary and this did not happen as company was unwilling to provide the necessary information. Consequently, the plan had to be terminated.

The other approach to proceed with implementing the proposed design was by considering the process of designing the Smartphone from scratch. Each component that are necessary for the proposed design are selected individually by setting certain criteria to meet the design requirement. The simplicity design concept guarantees understandability and this solves the issue of security. In the way of providing the understandability, 8-bit computer design were reviewed, as these computers are the only rationally trustable computers. The MEGA65 computer design derived within the telecommunication laboratory is the foundation for this project of designing a simple and secured Smartphone, which is coined as, MEGAphone.

After the final selection of the necessary components for the functionality of the MEGAphone, the functional features for the MEGAphone has been framed and the selected components pinouts are considered for deriving the schematic. The integrated schematic design was the main target, due to various design challenges and time constraint, the main functional blocks

individual schematics has only been derived. The entire design involves single serial interface approach and this ensures the design simplicity and thereby facilitating the user to easily interpret the design and make informed deduction about its security and other properties.

1. MOTIVATION

1.1 Modern Smart-Phones are Insecure

It is evident that the normal smartphone poses severe security threat due to the close integration of cellular radio, CPU and other peripherals.

According to Stacy Collet, contributing writer, CSO' a decade ago, the mobile malware was considered a new and unlikely threat and many mobile users even considered themselves immune for such threats'. But in 2017, the scenario is astounding as more than 1.5 million fresh incidents of mobile malware have been recorded by McAfee Labs merely in first quarter of the year (Collet, 2017). None of the Operating system platform are excluded from security vulnerability.

According to Joel Lee, 'not so long ago, vulnerabilities were revealed in SS7 (Signalling System 7), the international network that telecom companies use to transmit calls, texts, etc. These vulnerabilities, when exploited, makes it possible to listen in on any calls and track the location of any user' (Lee, 2015).

The SS7 (Signalling System 7) is basically an international telecommunications standard that is responsible for defining the information exchange that occur between network elements in a public switched telephone network (PSTN) and digital signal network (Russell et al., 1998).

The security breakdown is also possible by designing a backdoor to the device. The cellular backdoor is quite a common issue that is posing security threat and was first discovered in Samsung Galaxy S2 and this not limited to only Android OS.

According to the security researcher, Jonathan Zdziarski, even 'the backdoors are built into every iOS device' and this lets the personal information from any iOS device to be accessible on demand. This issue was raised with Apple and it has accepted such existence (Parrack, 2014).

The reducing costs, and increasing functionality of mobile telephones, this architecture also creates the possibility for an adversary to subvert the cellular radio, and in the process, gain control over the primary CPU of a device.

The System on a Chip (SoC) can be consider as the brain of the mobile device as it incorporates CPU. The different components that are surrounding it are memory (RAM), storage, integrated circuits and user input/output. As mobile phone is telephony enabled it consists of a modem which is one of the key component in setting up the mobile telephone network. For most handsets, the cellular modem is containing a CPU of its own, together with its own memory

and storage. The modem runs proprietary closed-source software, which cannot be easily reverse-engineered, tested or modified by end-users, making it untrustworthy.

The primary problem arises, not because the cellular modem is untrustworthy, but because it is tightly integrated with other components and is able, to influence the behaviour of them. This often includes the primary CPU of the phone, with the net result being that it is impossible to secure a modern mobile telephone, because of the risk that malicious software may reside in the cellular modem, and that there is no practical way to verify that this is not occurring. The remedy to this situation is to isolate the modem from the rest of the hardware, so that the modem is unable to seize control of the phone's primary CPU or other components, such as input and output peripherals (Replicant, n.d).

1.2 Insecurity because of complexity

Figure 1, depicts the degree of integration commonly found in modern mobile telephones. The cellular modem typically has direct access to the RAM, GPS receiver, audio path, and camera, so that it can facilitate audio and video calls in an efficient manner. On some devices, the modem may also have direct access to the bulk storage, and may be able to otherwise directly influence the operation of the primary CPU, for example, through DMA (Direct Memory Access) requests.

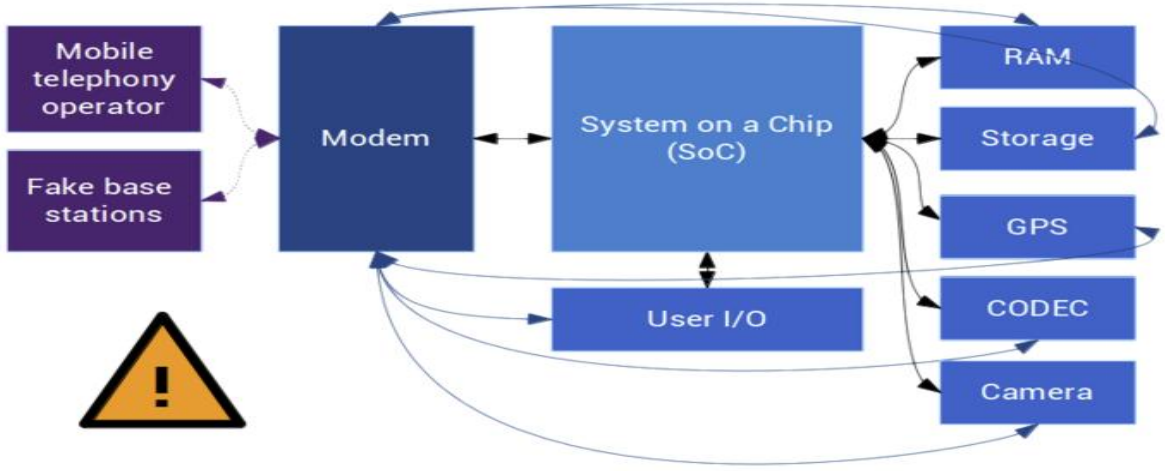

Figure 1: Tight integration = poor isolation of cellular modem (Replicant, n.d).

These are accessible to mobile network operator and currently attackers are also able to install fake base station in order, to access the private information of a smartphone user. There is a necessity to curb these intruders to some extent through a fair isolation design for the modem from the rest of the hardware is the solution to avoid the direct connection for modem to SoC. The below figure depicts the solution setup:

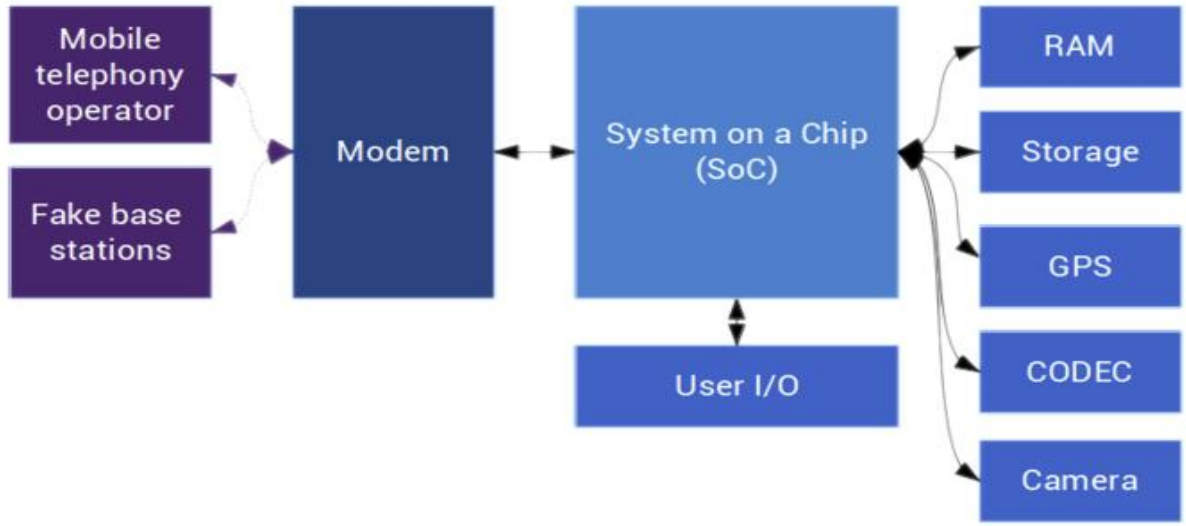

Figure 2: Better modem isolation (Replicant n.d)

From the above setup, the modem can access the device peripherals only when, SoC allows to access. Also, above setup will solve the security concerned issue to a favourable extent. But, it is a big step towards security threat elimination.

In addition to these, normal smartphones are so complex, that it is essentially impossible to produce strong security guarantees about their operation. Operating system consisting of million lines of code, and the hardware is complex, and the cellular radio firmware and operating system is closed source. These factors make it impractical for a user to verify that their device is running exactly the software that they expect, and none other.

1.3 Security through simplicity

In the present scenario of mobile communication, smartphone requires approximately 1 minute to boot, which is equivalent to the time fetched by modern computer as well. But, the computers in the 1980s were simple in design and the boot time was often less than a second. In addition to the variation in the booting time, software was small with minimal complexity. Due to this, it was able, to verify and prove with core software being only few kilo-bytes in size. A user could verify software byte-for-byte, to ensure that had not been tampered with. This approach has numerous advantages that can eliminate the problem addressed above. The system can also be simple enough to be subject to a comprehensive security audit.

1.4 Scope and research questions

The focus of this project is to work towards the creation of proof-of-concept hardware that can be used to create a loosely-coupled, and thus intrinsically more secure, mobile telephone handset. As the work is occurring within the resilient telecommunications laboratory, it will be based on the security through simplicity work based around the MEGA65 computer being developed in that laboratory. Also, in the way, the possibility of considering the modular phones as physical platform are dealt with.

In that way, modular phones such as Google's Project Ara and Fairphone's Fairphone 2 hardware and its case structure has been thoroughly analysed. It was intended to employ Fairphone 2 as platform. Unfortunately, due to the lack of the documents available for the Fairphone 2 with respect to its PCB design involving various interface. Also, considering the process of reverse engineering the entire PCB design would fetch a lot of time. With all these drawbacks and delay prediction, the design of the MEGAphone using Artix7 FPGA was considered. The design process of the MEGAphone was initiated with the identification of the hardware features, selection of appropriate components to provide those features, and development of the electronic schematics surrounding each of those components are all within the scope of this project. It was originally intended that the development of a complete, integrated schematic would also be within the project scope, however the limited time available has caused this to fall out of the final scope. Also, out of scope for this project is the development of the necessary software to run on the hardware, as well as the testing of the hardware and industrial design of the handset.

Thus, the tasks documented in this thesis are:

- In Chapter 2, conceptualising the simple and secured smartphone has been discussed.
- In Chapter 3, involves quick overview on main components assembled with respect to mobile phone, followed by modular phone discussion and then followed by detail discussion regarding security problem with respect to smartphone with some examples and finally concluding this chapter with cellular module overview and FPGA.
- In Chapter 4, a brief overview on MIPI alliance and then followed by analysis of the MEGA65 project to understand the hardware capabilities and interfaces that can be used in development of a mobile handset version: The MEGAphone is included.
- In Chapter 5, Identifying and enumerating the various hardware features and interfaces required for the MEGAphone design, to make a minimally useful device.

- Having identified those hardware functional requirements, from Chapter 6 to 8, selection of appropriate hardware components for MEGAphone to provide each feature identical to a smartphone has been sorted out.
- In Chapter 9, the components that are finalised for the MEGAphone design are discussed along with the MEGAphone functionalities.
- In Chapter 10, some of the miscellaneous interface that can be included in the future are discussed.
- Then in Chapter 13, working towards the schematic for the MEGAphone, through developing schematics for each hardware interface or sub-system are dealt with.
- In Chapter 14, future work discussion has been included.
- Ultimately, a conclusion in Chapter 15.

Through this structure, the following research questions will be explored and answered:

1. What are the interfaces of the Fairphone 2 internal modules?
2. Exploring the possibility for implementing all the necessary interfaces required to derive the MEGAphone from scratch through an Artix7 FPGA.
3. Schematic design development for the individual functional blocks of the MEGAphone.
4. Analysing feasibility of the MEGAphone design.

2. DESIGNING A SIMPLE AND SECURE SMART-PHONE

We can add such minimal hardware extensions to an old 1980s computing platform that are required to provide strong security operation, e.g., through the addition of memory protection. Rather than integrated design of CPU and cellular radio, we can isolate the cellular radio from the main CPU in a loosely-coupled way, such that the cellular radio appears simply as a serial peripheral to the core CPU, and with the core CPU having the ability to physically turn the cellular radio on and off when desired, so that there is no chance of the cellular radio subverting the system or eavesdropping on operation when the operator wishes to prevent this. Thus, the resulting device will boot more rapidly than earlier.

It will still have a wide library of software available to it, if we make it truly compatible with one of the older computing platforms. For example, the Commodore 64 has more than 10,000 games, and many hundreds if not thousands of productivity titles. Also, the existing base of people with experience programming such systems could easily create new software for the system. Thus, it would begin already with a wide variety of software that could be further extended, once the device is created.

It was in 1981 that Commodore 64 was introduced which is basically an 8-bit computer and accommodates a disk drive. The design of updated version of Commodore 64 was started in 1989 and was named as Commodore 65. The Commodore 65 reached pre-production prototype stage, before production was cancelled. It would have remained completely unknown, except that in 1994 the pre-production prototypes were sold off when Commodore was liquidated (Zimmers, n.d.). Following image shows the appearance of Commodore 65.

Figure 3: Top view of Commodore 65 (Detlef Hastik et al., n.d.)

Figure 4: Side and Rear view of Commodore 65 with various peripherals connection slot (Detlef Hastik et al., n.d.).

3. LITERATURE REVIEW AND BACKGROUND

3.1 What is in a mobile phone?

In present mobile market, there are ample number of smartphone and some of the popular smartphone vendors include Samsung, HTC, Apple, Motorola, LG and many more in the list. It is very complex to generalise what is inside the phone as there are at least ten or more number of CPU's and different GPU's also there is a plenty combination for display hardware (Schiesser, 2012).

Other factor that makes complex in describing is, that retailers use different marketing and technical terms to define the smartphones (Ginny Mies et al., 2010). But setting aside all the confusions we are trying to describe general components inside the smartphone and are as follows,

3.1.1 Processor

Description regarding SOC's were briefed in the earlier section. Whenever the discussion regarding the processor happens it is like indirectly referring to SOC's as it is one of the prime component present on the mainboard inside a smartphone which is basically brain of the device. It justifies this term by managing almost all the device central processing function within a single chip (Ginny Mies et al., 2010).

The major manufacturers in 1 GHz processor section are Qualcomm (snapdragon), Texas instruments (OMAP) and Samsung (Ginny Mies et al., 2010). The latest smartphone is equipped with 2.5 GHz processor.

Currently, there are many latest Qualcomm's processor trending in the market such as Snapdragon 800 and 600 series and these are highly sophisticated processor. But, it is quite expensive and not possible to consider for the current design from the economic perspective. As a result, inexpensive processor of Qualcomm's is considered such as snapdragon series S1 to S4 with former being first in snapdragon range while the latter is the latest version. S1 and S2 snapdragon SOC's are having single core with processor range up to 1.5 GHz. With S1 being the first in range of snapdragon was used in the initial series of windows phone and in some Android devices. (Schiesser, 2012).

The S2 Snapdragons are used in more number of products compared to S1 as it incorporates a powerful graphics processor. Additionally, the process is decreased from 65nm to 45nm which results in less power consumption and heat output during large CPU clocks.

The S3 snapdragon basically takes a leap from single-core to dual core SoC's with boost increment being another added feature. These are manufactured using 45nm process and delivers processing speed of 1.2 - 1.5 GHz (Schiesser, 2012).

3.1.2 Camera

Nowadays, camera section is one of the prime component in the smartphone as it is the major feature observed by photography enthusiast. Day by day, the users are expecting a better camera feature in terms of increased pixels and resolution. Due to portability advantage, which also eases capturing, the OEM (Original Equipment Manufacturers) are proposing camera unit as one of the main feature. Before, rear camera was playing pivotal role for user to consider a Smartphone to buy. But, now the selfie camera (front camera) has gained huge popularity, with the user expecting higher pixel even with the front camera (Schiesser, 2014).

There are many parameters involved in the design of a Smartphone camera which includes hardware, pixel sizes and f-stops etc. and are discussed in detail in the further section. It's quite common that, all the smartphone cameras basically have two major components namely, sensor and lens. It's almost impossible to capture the image even if one of the either components is absent. So, they both are isolated into one unit which makes connection to PCB via ribbon cable attached to it. The below image depicts the smartphone hardware physical appearance (Schiesser, 2014).

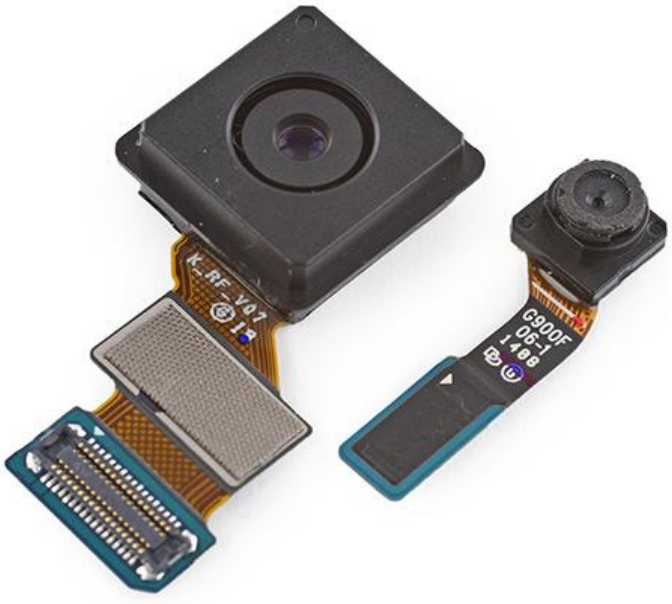

Figure 5: Samsung Galaxy S5 camera module with f/2.2 lens and Samsung S5K2P2XX1/2.6" sensor (Schiesser, 2014).

The component that is responsible for capturing the image is sensors. Basically, sensor collectively integrates photodetectors, amplifiers, transistors, power management and some type of processing hardware. The photodetector functions by capturing light. The CMOS technology is inducted in the smartphone camera sensors. CMOS technology is better compared to other sensor technology such as CCD, as CCD results in excess power consumption, also expensive to adopt this technology in smartphones (Schiesser, 2014).

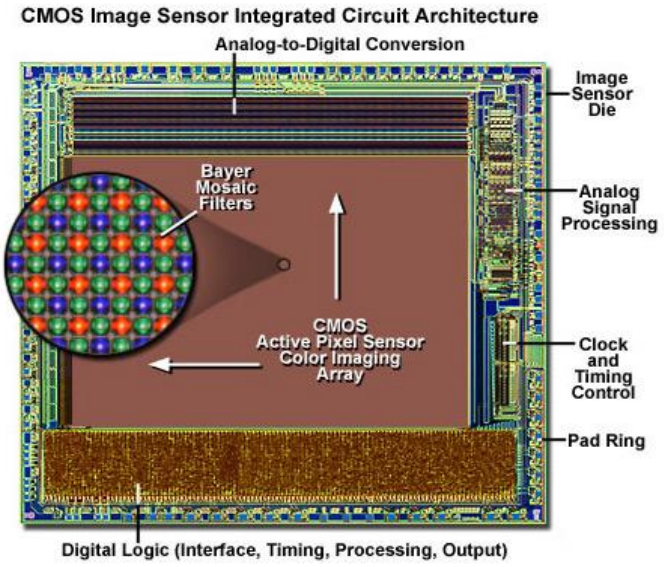

Figure 6: CMOS image sensor integrated circuit architecture (Schiesser, 2014).

The photodetectors connected to each pixel in the image encapsulates the Analog information of photons striking it. This recorded information is amplified and transformed into a digital signal corresponding to the brightness of photons. The colour image is usually obtained by layering RGBG Bayer filter over the line-up of photodetectors. In the means of obtaining a fully coloured image, interpolation software algorithm is used. This is structure of working of a CMOS sensor. The concept of megapixel is that megapixel of a camera is directly proportional to number of photodetectors in the sensor's line-up. Therefore, a twelve megapixel relatively has twelve million photodetectors in the array. The main component that is responsible for a clear crisp image is lens and if suppose if its missing, resulting image will be blur as the photons strikes the sensor from all the angles. An ensemble of glass or plastic elements forms a lens, with glass providing high quality and sharp images (Schiesser, 2014).

3.1.3 RAM

Nowadays, while evaluating a smartphone performance RAM is becoming one of the critical parameter in deciding that. The various functions that are carried out by CPU is quite easy to understand but it is very complex to define the functioning of the RAM. Basically, acronym of RAM is Random Access Memory which the direct access to any bit of data that is stored in it. The access is provided instantly as there is no sequential scanning process, which is a tedious process. The smartphone RAM is comparatively having higher speed than the external memory with 16 GB storage capacity such as Micro SD card. The current data that are being used by smartphone are stored in RAM, that is, when the application starts running, collective data of the corresponding app are stacked onto the RAM. Consequently, stacked data in the RAM is moved again to a small group of memory having high speed comparatively (Williams, 2016).

The RAM is responsible for multi-tasking. The user tests the multitasking efficiency and these days, smartphones are equipped with authentic window-style multi-tasking with two apps running simultaneously on screen. This multi-tasking performance is solely dependent on the amount of the RAM being used. Consequently, multitasking enables switching between the applications (Williams, 2016).

As the RAM capacity decreases, certain issue evolves, for example, basic Android phones equipped with only 1GB of RAM results in cluttering when operating with Android version 5.1. While, with the Android version 6.0, systematic memory handling is not possible. Ultimately, to avoid this performance problem, it would be ideal to set the minimum RAM requirement to 2GB (Williams, 2016).

3.1.4 Display

This is one of the key component in any smartphone for establishing user interface that includes messaging, web browsing, viewing videos. To ensure all these features, considerably large display equipped with high pixel resolution to ensure sharp output. When the mobile era began, a display size of 2.7 inches were more enough to carry out basic surfing and manage e-mails. The limitation of this screen size is, it was not sufficient to play games and stream video. In the process of overcoming this limitation, it is better to increase the screen size to 3.5 inches (Ginny Mies et al., 2010).

At present large screen size is trending in the market with range of, 5-inch to 6-inch. There are various technologies that are used to design display which gives a different viewing experience in terms of clarity. Most commonly used technology is LCD (liquid crystal display) which

outputs sharp graphics and even economic. The LCD display are further classified into two types TFT and IPS, the former uses thin-film transistor technology which aimed in improving the image clarity but it failed in providing good viewing angles additionally it is prone to direct light falling on display which results in poor visibility. In addition to all the above, the major drawback is high power consumption and thus were characterised as feature phone rather than as a smartphone (Ginny Mies et al., 2010).

So, to overcome all these drawbacks latter type, that is, IPS (In-Plane switching LCD) were designed which is featured in major firm smartphone manufacturers such as iPhone, Motorola though with different marketing terms which solved all the problems that occurred in TFT LCD (Ginny Mies et al., 2010).

Presently, AMOLED (Active-Matrix Organic Light-Emitting Diode) is trending slowly and are incorporated in top end smartphone such as Google Nexus series, Samsung edge series are some of them. The performance of this type of display is impeccable as it provides the user with better viewing clarity even in the bright light when compared to LCD. Recently, some minor flaws are pointed out by the users stating that it produces oversaturated colours. Even though the manufacturers claim it consumes less power when compared to LCD displays but in real, it consumes same amount of power as that of the LCD display (Ginny Mies et al., 2010).

3.1.5 Touch screens

The user interaction with the smartphone in mainly to establish the interface and access to the operating system is possible through touchscreen. Currently, two types of touchscreen are trending in the market known as capacitive and resistive. When the smartphones evolved, resistive touchscreen were very commonly employed. Basically, a resistive touchscreen consists of two conductive layers with a minute gap in between them. Whenever the user taps the screen through finger, screen gets distorted at that point resulting in the union of two layers. Ultimately, it leads to circuit formation at that particular point and thereby the interface with smartphone processor is established (Ginny Mies et al., 2010).

Currently capacitive touchscreen is equipped and this basically has a layer of glass which is often coated with a diaphanous conductor such as indium tin oxide. The electric conduction also happens through human body and this distorts the electrostatic field when finger is tapped on glass coating and the processor has the responsibility of finding this location to enable interfacing (Ginny Mies et al., 2010).

3.1.6 Battery

Mostly, today's smartphones are equipped with lithium-ion battery and are rechargeable. Basically, the movement of the lithium ions from cathode to anode takes place during discharging and it is vice versa during charging process. The durability of this type of battery is longer when compared to alkaline batteries by two to three times. As present smartphones have a minimum screen size of 5 inch, it consumes more power and thus it is equipped with 2000mAH battery. The smartphone battery capacity is expressed in milli-ampere-hour (mAh). The battery optimisation is possible by controlling screen brightness, mobile data usage and Wi-Fi usage (Ginny Mies et al., 2010).

3.1.7 4G LTE

Currently, third generation network are being upgraded to fourth generation while the latter one is almost ten times faster than former, with the speed ranging between 20 Mbps and 30 Mbps (Kumaravel, 2011).

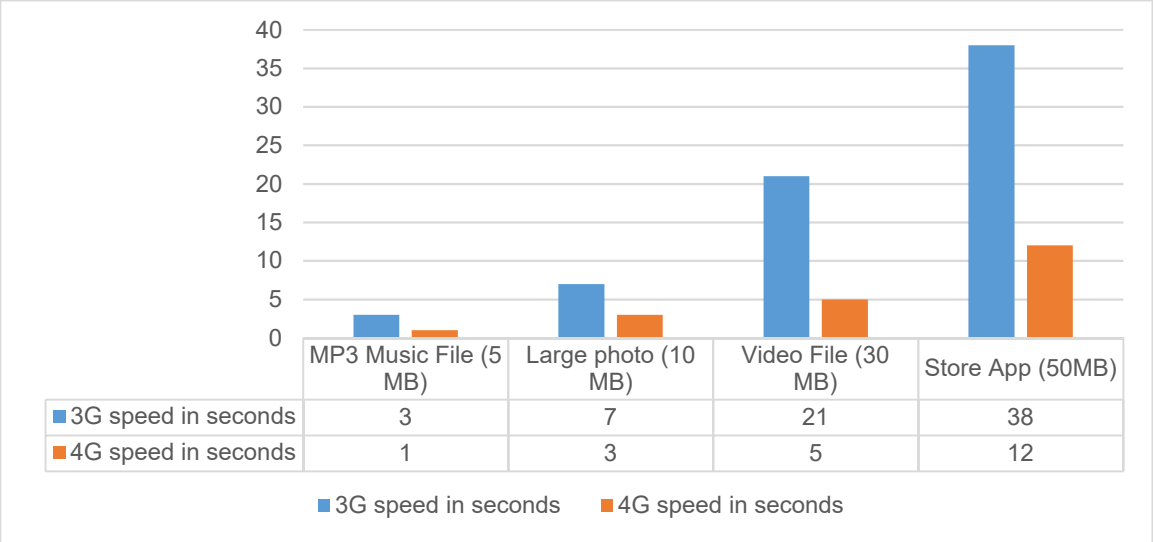

Figure 7: Bar graph depicting comparison between 3G and 4G download time for various types of file (Kumaravel, 2011).

3.1.8 Bluetooth and Wi-Fi

Wireless technology is playing a vital role in all the electronic gadgets. The smartphone is equipped with Bluetooth module which enables data transfer between the devices within a limited range. There has been a lot of upgradation in Bluetooth technology with number of versions in the market with the present version being, Bluetooth 5.0. The current trend in adoption of Bluetooth technology is that it is solely used to pair the devices from external sources within limited range such as Bluetooth headphones and earpieces (Genie, 2017).

It has been very common in the present smartphones that has been equipped with Wi-Fi technology which enables the possibility of establishing the connection with other device over a wireless local area network (WLAN). The specific standard for this type of communication is IEEE 802. 11 and its compulsory to all the devices which incorporates Wi-Fi to abide by this standard and are permitted to use the logo if the certification has been approved by Wi-Fi alliance (Genie, 2017).

These days 'hotspots' are very popular in commercial and public spots such as cafes, airports, stations, sports arena to name a few while its very common in homes and connection is established by installing a wireless broadband router. Ultimately, this is how a smartphone is utilising the Wi-Fi technology (Genie, 2017).

3.1.9 GPS

The position or the location of the smartphone are determined with the help of GPS technology incorporation. The Global Positioning System (GPS) technology traces the location by co-ordinating with satellite. Normally, a smartphone is equipped with A-GPS and this model is common in most of the current smartphone and of recent years as well (Genie, 2017).

3.1.10 Ambient light sensor

Presently, every smartphone is equipped with ambient light sensor that detects the environmental light and thereby manipulates the screen brightness. This sensor employment plays a vital role in providing user with the accurate brightness for viewing in various situation. Furthermore, it also optimises the power consumption (Fryer and Blakesley, 2005).

3.1.11 Proximity sensor

The proximity sensor has the capability of detecting the object nearing it even in the absence of physical contact. There are various kinds of proximity sensors in the market that suits wide range of application.

One of the most common proximity sensor employed in the smartphone device is, the Infrared (IR) based sensors. These IR sensors are responsible for detecting human ear approaching towards it (Khan et al., 2013).

The basic phenomenon is that, the IR sensor emits the Infrared radiation to detect the target approaching towards it. If the target is detected, the changes in the returning Infrared signal is noticeable when compared with emitted signal.

So far, the type of proximity sensor employed in smartphone and concept of detecting the target has been overviewed. Now moving on further, regarding the role it plays after the detection of

the target, the smartphone LCD panel backlight is forced to inactive state thereby, power is conserved. Additionally, accidental touch that may occur through cheek can be eliminated by inactivation of LCD panel backlight (Khan et al., 2013).

3.1.12 Microphone

The fundamental purpose of the mobile phone is to enable the voice communication and the entity that is responsible for this functional implementation is, microphone. There has been a lot of revolution in the field of microphone for the telecommunication purpose. During the initial days of the mobile phone evolution, the electret condenser microphone was employed and this was so economic that the currently trending MEMS (Micro-Electro-Mechanical-Systems) microphone was unable to the gain the commercial success with respect to bulk production since, twenty years of its entry in to the market. Contrary to this, the electret condenser microphone is susceptible to higher temperature. As a result, currently every consumer application oriented device including mobile phone is assembled with MEMS microphone due its ideal features such as, surface mount capability, signal processing enabled and even it withstands the acceleration effects (Weigold et al., 2006). Further details of the MEMS microphone and the ideal one that is employable for the MEGAphone design is discussed in the later section.

3.1.13 Out of scope components

There are many other entities that are integral part of mobile phone and some even, provides security oriented features. The corresponding entity components are not researched at this stage of the thesis work as the initial target is to obtain a minimally functional device. So, the selection of these components would be carried out in near future. In this section, quick overview of some of those entities are included followingly.

Firstly, the storage in any mobile phone is one of the most essential entity and this serves multiple purpose such as to store the data files including images, audio files and documents. Normally, the current mobile phones are assembled with internal flash storage, an external SD card slot and even, a certain amount of RAM (Random Access Memory). The internal flash storage embeds all the prime system partitions such as bootloader and kernel partition, system settings, recovery, preinstalled system application and finally, the user installed application data. Alternatively, the external storage is basically used for storing the media files of the user (Kim et al., 2012). The detail discussion regarding the RAM has been carried out in the earlier section of 3.1.3.

Now moving on to the most trending security oriented technology included in the mobile phone, that is NFC. The NFC (Near-field communication) is basically a radio technology that functions within a short range and the communication is enabled between two NFC enabled devices. The communication between the two NFC enabled devices is established when both the devices are less than four centimetres away or even tapping would be ideal. The frequency of operation of NFC is 13.56 MHz with the data transfer capability of up to 424 Kbps (Kilobits per second). During the NFC communication, two devices are necessary. So, out of two devices, the first device is known as initiator which is basically active and initiates the communication and the second device is known as target, this basically responses to the initiator requests (Ok et al., 2011).

Ultimately, one of the most sophisticated technology that is employed currently in mobile phone is, the biometric sensors. The biometric sensor is basically a transducer input from a person such as fingerprint, voice and face into an electrical signal. Normally, the sensor measures pressure, temperature, light, speed, electrical capacities and other various energies (Parziale, 2015). In the present scenario, most of the mobile phones are equipped with biometric technology such as fingerprint scanner and iris scanner. The currently available fingerprint recognition has adequate precision that is required for verification system. Even multiple fingerprints of a person can be recorded using the present fingerprint technology that enable large-scale recognition involving millions of data (Jain et al., 2004). The complex iris present in human eye embeds a very distinctive information that aids in personal recognition. The accuracy and speed of iris scanner is commendable. The iris scanner is considered as the most sophisticated biometric technology as tampering the texture of iris through surgical means is highly complex (Jain et al., 2004).

3.2 Modular Phones

Every smartphone, features an integrated design. During a situation if there is an issue with one of the component and if suppose it should be replaced, it's not possible by common user to disassemble the various modules and replace it and thus, it requires a mobile technician to fix it. Furthermore, the durability of these phones due to complex circuitry and less provision for repairing will make it to last for a few years.

To overcome all the problems stated above, the concept of modular phones has evolved and is slowly gaining the popularity. The key idea of modular phone design is, each individual module can be disassembled and can be reassembled. This disintegration and integration can be carried

out by common user itself. Thus, one could fix the problem by changing the component by replacing it with a new one.

Modular phones also provide the benefit of customization of hardware of the device like upgradation of camera, speaker, graphics etc. Consequently, with all these added advantages it enables the user to stick on a handset for a long time and therefore it increases the durability of the phone. Moreover, there is no need of changing the whole handset which is expensive rather than that, there will be a second option which works out economically by upgrading only required components (LA, 2017).

Currently, there are a variety of modular phones and modular accessories and lot more to enter the market. The modular accessories enable the user to modify the handset by attaching them thereby considerably improving the performance. But it is not possible to alter the core hardware as of now. Presently, four major mobile manufacturers are undertaking and executing this project and it includes Google Project Ara, Motorola with their flagship of Moto Z and Z Force, LG G5 and Fairphone 2 (LA, 2017).

3.2.1 Google Project Ara

Google's project Ara is one of the most anticipated modular phones but it's not out in the market yet. This phone is designed in such a way that different components of the phone can be assembled like Lego bricks thereby allowing the user to customise and upgrade every component of the smartphone. This has opened a platform for revolutionising feature-phone to high interface enabled smartphones due to fundamental transformation in science and engineering (Yadav and Yadav, 2015).

The main aim of project Ara is to create a base for open hardware for the implementation of modular phones. Here endoskeleton is designed as base frame which accommodates the custom modules selected by the user namely camera, display, additional battery and sensor. During the failure of any component or in case of upgradation, the user can replace with a new component resulting in improvement in terms of durability of handset for a long time. Consequently, electronic waste is minimized (Yadav and Yadav, 2015). Following image depicts the endoskeleton model.

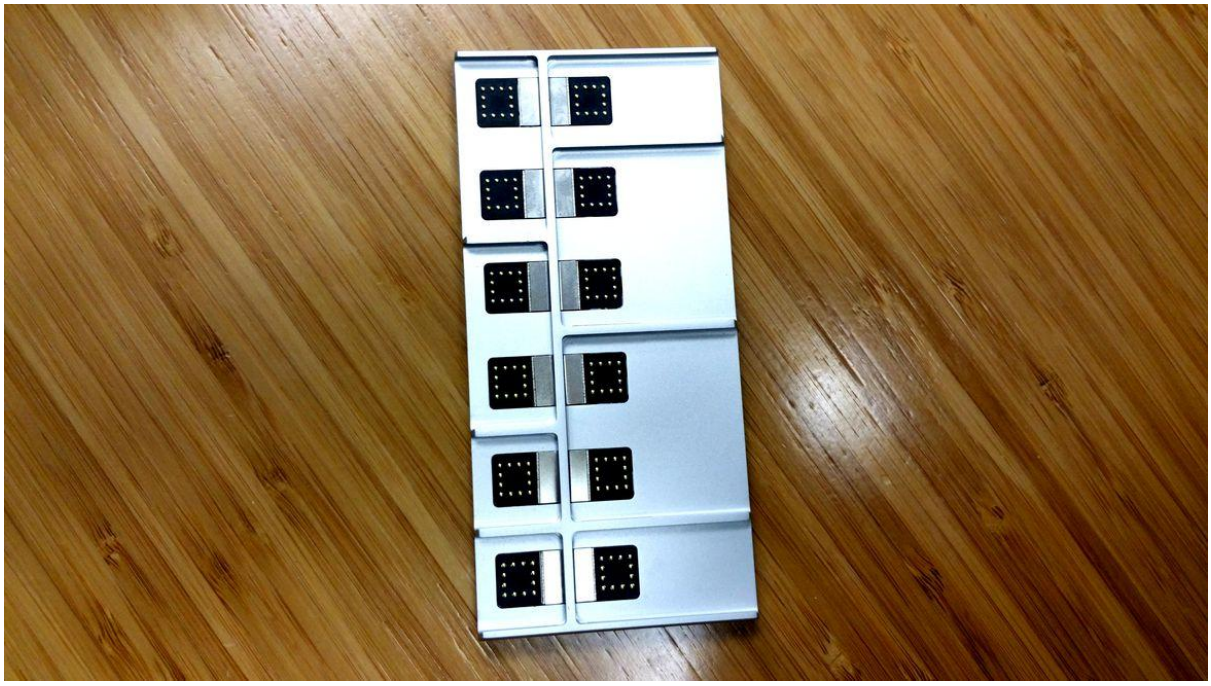

Figure 8: Endoskeleton model of project Ara phone (CNET).

Below image depicts the endoskeleton providing provision for front camera slot:

Figure 9: Skeleton head of project Ara phone (CNET).

Apart from the common features like smartphone, this modular phone is equipped with more sophisticated features namely receipt printers, laser pointers, pico-projectors, night vision sensors, mini joystick and these could be accommodated if module fits on a slot of the frame (Yadav and Yadav, 2015).

The slots are of different size and functions properly if the components with specific dimensions are plugged in properly and it can be observed in the below image:

Figure 10: The slot and various slot modules of project Ara phone (CNET).

As per Google, replacement of modules such as battery allows the user to do so without the need of turning off the smartphone. In general, there is no necessity for switching off the phone which eliminates time required for booting. Unfortunately, CPU and display cannot be replaced. For case replacement and upgradation of modules, Google is about to set up an online platform identical to play store through which the new modules can be ordered. (Yadav and Yadav, 2015).

It is slated, that Ara frames would be made available in three sizes with small frame being named as mini and its size would be identical to feature phone. On the other hand, **medium** and large frames have Nexus 5 and Galaxy Note 3 size approximately. In the initial, the frame comprises of basic circuitry and some components interface to provide basic communication with each other (Yadav and Yadav, 2015).

The number of grids in mini, medium and large are consecutively 10, 18 and 28 square blocks in array of 1, 2 or 4 in the rear of the frame. Project Ara provides an open platform thereby benefitting by cutting down the barrier for the third-party developer entry. Eventually, opportunity increases the growth of smartphone industry. Additional advantage of this open platform is the growth of individual component manufacturers in the design which they are

specialised and thereby regaining lost fame and business due to encroachment by smartphone (Yadav and Yadav, 2015).

There are few drawbacks around this project which is delaying the launch into the market. As there is a huge investment for in R&D for designing of flexible smartphones allowing to warp and enfold with Ara being block design phone there are some concern over the popularity and success that may get once it is out in the market and finally, Software optimisation is also one of the major concern. Meanwhile there are few advantages such as, getting rid of pre-installed hardware and software as Project Ara enables customisation of these. Hassle free environment when it comes to repairing and upgradation of the phone (Yadav and Yadav, 2015).

Google has exhibited during its I/O (Input/ Output) conference, also it has posted the video in YouTube. It has come up with two prototypes namely Spiral 1 and Spiral 2. Spiral 2 sports custom Toshiba chips with operating system being Android. The Spiral 2 prototype can accommodate up to eight modules and could be observed from the following image:

Figure 11: The project Ara, Spiral 2 prototype (CNET).

As mentioned earlier, the project includes, exploring the possibility of including modular phone as platform. The following section unveils the Fairphone 2 and its specification.

3.2.2 Fairphone 2

Fairphone 2 is the successive model of Fairphone which is manufactured by the company, Fairphone established in 2013. Perhaps this is one of the first modular phone to enter the consumer market. Basically, this phone consists of seven removable parts such as main chassis, removable battery, display assembly, rear camera, receiver module, the speaker module and back protective cover. Total thickness of the phone is 11mm measured from back of case to top of glass. Buttons are part of transceiver sit on flexible printed circuits (FPCs) that are spring connected to main board. The detailed specifications of the Fairphone 2 is tabulated as below:

Display	5-inch, LCD TFT/IPS, Gorilla glass 3
OS	Android 5.1 (Lollipop)
SIM slots	Dual SIM
Platform	Qualcomm Snapdragon 801
RAM	2GB
Camera	8 MP rear camera
Storage	32GB internal storage, Expandable storage micro SD slot
Battery	2420mAh (removable lithium ion battery)
Connectivity	4G LTEW/ 3G/ 2G
Wi-Fi	802.11 b/g/n/ac
Bluetooth	4.0 LE
GPS	Enabled
Interface and connectors	Buttons – power, Volume, Camera (programmable)
USB Port	micro-B 2.0 with OTG support
Micro SD Support	SDHC, SDXC, UHS
Notification LED	3-colour
Sensors	Ambient light, Proximity, 3-axis compass, 3D Accelerometer, 3D Gyroscope

Table 1: Fairphone 2 specification (Fairphone, 2017b).

A close-up view of various parts inside Fairphone 2 can be observed from the following images:

Figure 12: Front view of Fairphone 2 (Fairphone, 2017b).

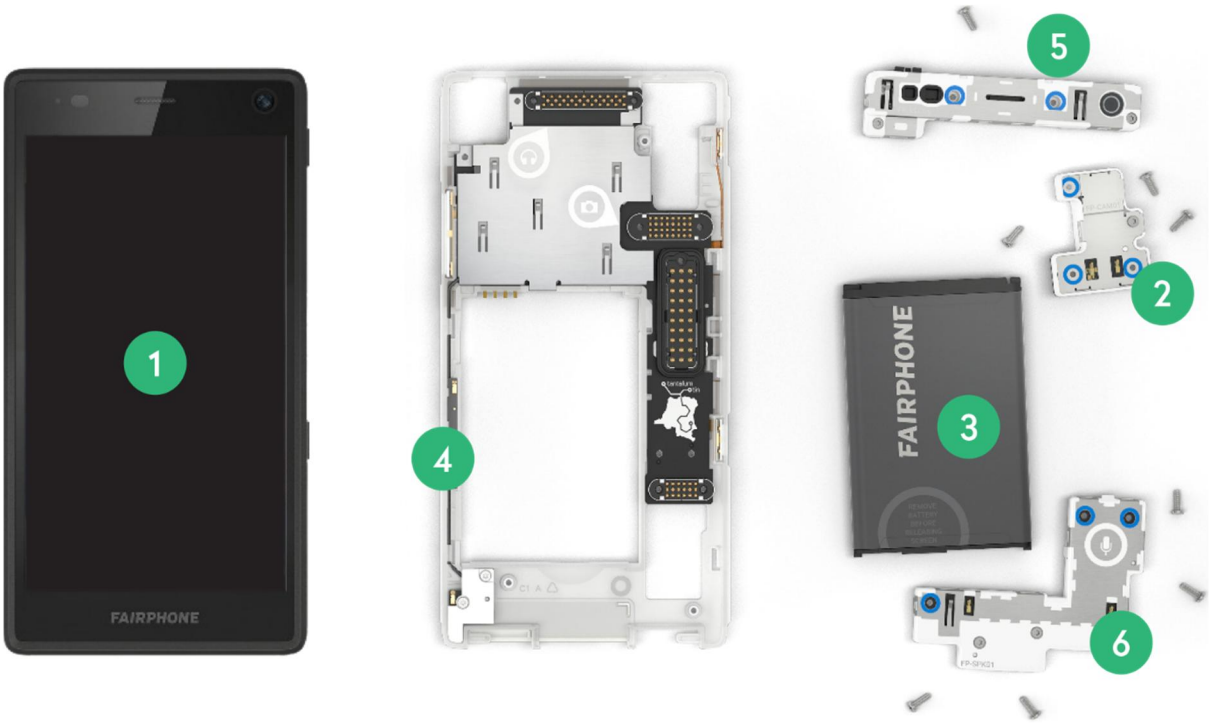

Figure 13: Disintegration of Fairphone 2 parts (Fairphone, 2017b).

3.2.3 Fairphone 2 configurations in detail and teardown discussion

Some of the latest smartphone batteries are non-removable, additionally it encompasses the bracket-covered press connector design, while the fair phone 2 has spring contacts design which were seen in older smartphone way back in 2005 (ifixit, 2015).

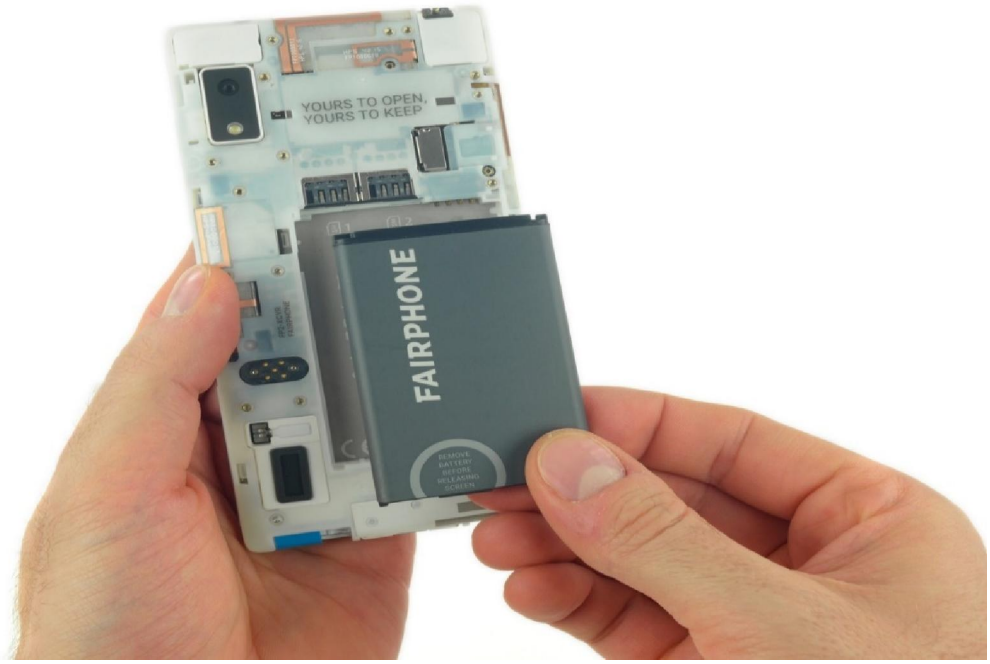

Figure 14: The battery compartment (ifixit, 2015).

Once the back cover of the phone is detached, two switches are flipped and the sliding the panel outwardly results in dismantling of display assembly.

Figure 15: Sliding mechanism for separation of display from mainframe (ifixit, 2015).

After separating display from mainframe, the collection of pogo pins can be noticed and this is plugged into counterpart present in the main frame. The following images are related to the above description.

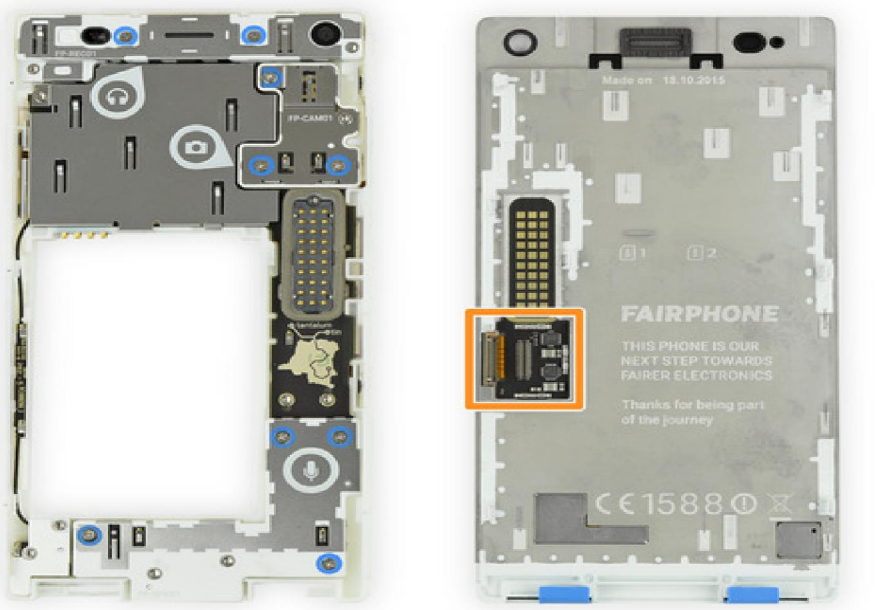

Figure 16: Pogo pins that interconnect display and main frame (ifixit, 2015).

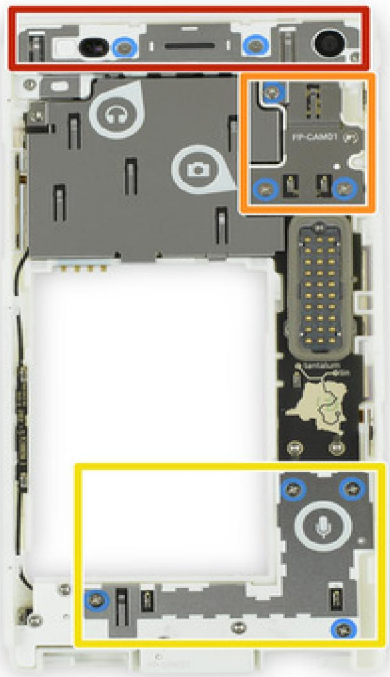

Figure 17: Earpiece speaker, headphone jack, front and rear facing camera unit (ifixit, 2015).

The above figure (Figure 17), depicts the various components of the phone such as earpiece speaker, headphone jack and front facing camera unit. These parts are highlighted using red mark. While, the rear facing camera module is highlighted using orange mark and finally, the microphone module in yellow mark (ifixit, 2015).

Following images indicates the module view of front camera, rear camera and microphone:

Figure 18: Front facing camera module (ifixit, 2015).

The rare camera module of the Fairphone 2

Figure 19: Rear camera module (Fairphone, 2017a).

In the following page, the Fairphone 2 microphone module is observable:

Figure 20: Microphone module (ifixit, 2015).

RF cable which transmits the radio signal along the frame corner into main antenna. It could be observed in the following images:

Figure 21: RF cable transmitting signals onto the main antenna connection (ifixit, 2015).

After dismantling each component, plastic frame incorporating all the embedded antennas and buttons having spring contacts thereby enabling connection to the mother board. The USB 2.0 device interface is designed in terms of five pogo pins, power input is required and this enables users to upgrade with other features such as NFC (Near Field Communication) being used for the transaction payments by tapping mobile instead of cards (ifixit, 2015).

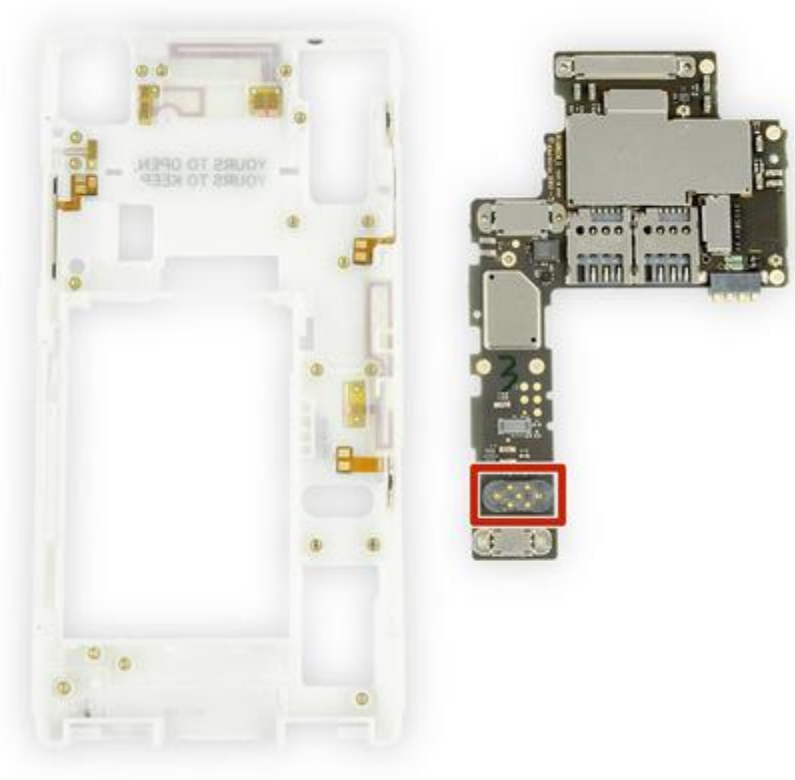

Figure 22: Fairphone 2 frame and main PCB (ifixit, 2015).

Coming to the main hardware such as ROM and Bluetooth module, Samsung KLMBG4WEBC 32GB eMMC NAND Flash (Red marked) and Qualcomm WCN3680B Wi-Fi 802.11 ac Bluetooth combo (orange marked) as per inputs from Fairphone team. While coming to Accelerometer + Gyroscope, ST Microelectronics LSM330DLC 6-Axis (yellow marked) has been incorporated (ifixit, 2015). The following image depicts the above description:

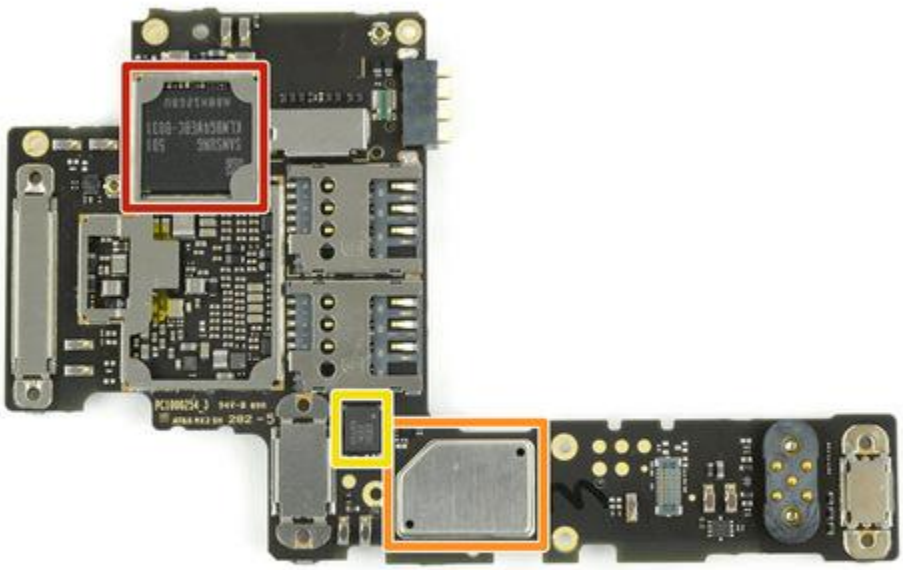

Figure 23: ROM, Bluetooth module, Accelerometer + Gyroscope (ifixit, 2015).

Ultimately, on the back of the board lies the RAM Samsung K3QF2F20EM 2 GB LPDDR3 RAM, layered on top of the Qualcomm snapdragon 801 MSM8974AB (red marked), the RF receiver used here is Qualcomm WTR1625L (Orange marked) identical to one used in iPhone 6. Audio codec used here is Qualcomm WCD9320 (Purple marked) also RF Micro Device RF7389EU Multimode Multiband Power Amplifier Module (yellow marked) has been accommodated. On the other hand, Qualcomm QFE1100 Envelope Tracking Power Management (green marked) has been used and ultimately, Qualcomm PM8841 PMIC (blue marked) is incorporated (ifixit, 2015). The above description related image can be observed below:

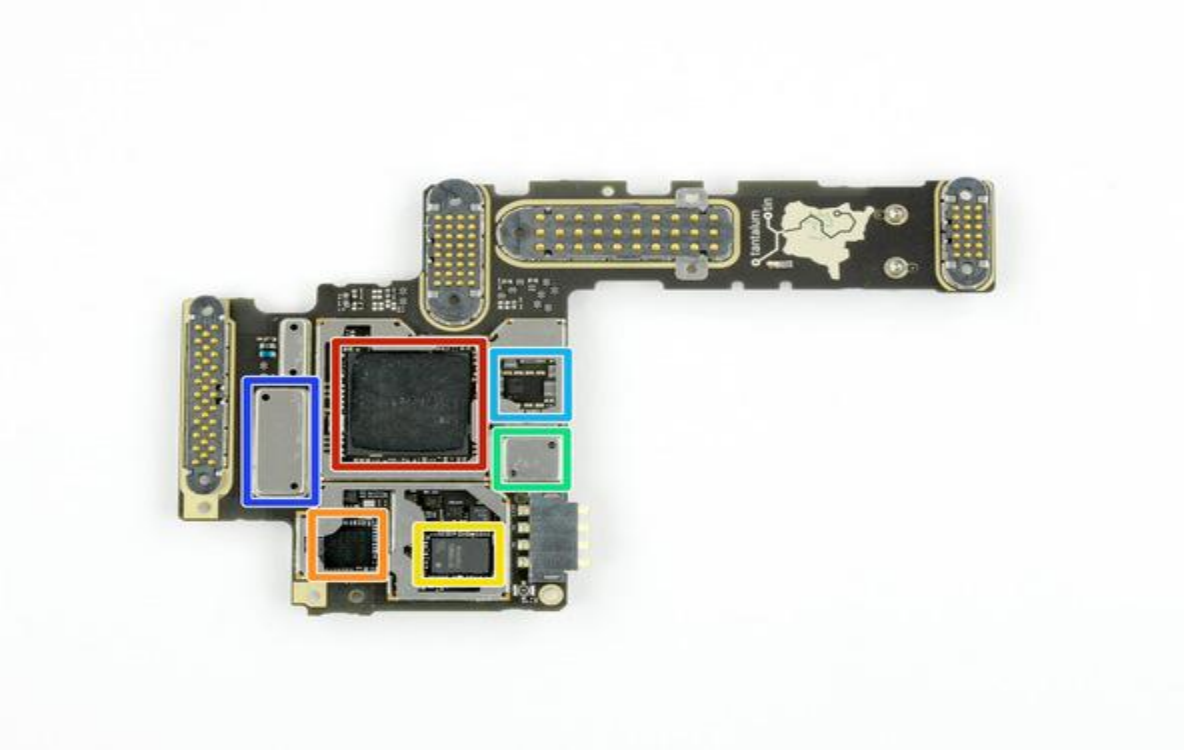

Figure 24: RAM, RF receiver, Audio codec and Envelope Tracking Power Management module (ifixit, 2015).

This marks the end of the detailed teardown of Fairphone 2 as this is the primary requirement for further developments to be carried out in considering the modular phone as platform in designing the concept of secured smartphone. Even though the detail hardware specification of the Fairphone 2 was available through this teardown, also from the above image (Figure 24), the main PCB of the Fairphone 2 is observable. But, the internal connection that exists between cellular radio and CPU and even other main components is not available as the company has not made it public. Even the company was approached, to obtain this information, but it was not ready to reveal on the grounds of the company policy. So, at this stage, inclusion of Fairphone 2 as platform for designing secure smartphone is ruled out.

3.3 Security Problems with smartphones

In current technological trend, the mobile user's community is rapidly increasing, also security risk is growing in proportional. As reported by, Mary Meeker's 'detailed statistics about internet usage, earlier this year the mobile usage was outpacing desktop or laptop'(Bradbury, 2015). Also according to her, mobile phone users spent an average of 2.8 hours a day, while the laptop or desktop users accounted to only 2.4 hours a day (Bradbury, 2015).

In the current scenario, mobile devices are acting as a storage device for plenty of personal and corporate data and the mobile companies are taking responsibility of encryption. Most of the

mobile companies include antivirus software to restrict the unauthorised access to the personal data. Even, with these precautionary measures there lies some threats.

Dean Weinert, head of mobile for security firm ThreatMetrix, claims that, third party application stores which hosts number of third party applications is main security threat to the smartphone as it is the unauthorised version of the statutory application. This has affected the official application store including Apple even though it has name for providing high end encryption (Bradbury, 2015).

On the other hand, Google's play store had provided platform malignant application which paved way to break Google's automated antivirus system. One such application was Bouncer which performs scan for malware with respect to new application, but in the background, premium SMS services is made to activate for the user (Bradbury, 2015).

As per Symantec experimentation, to detect malware and privacy concern, scanning of Android apps were carried out and the results revealed that one third of the applications disclosed SIM card details having access to call log, address book details and mobile PIN numbers. Also, with the application scanned, without user knowledge, the mobile phone number has been collected. The free application available in the store is a major malware, where in the user is promoted as a product says, Johnathan Kuskos manager of EMEA threat research centre at WhiteHat Security. One example to suspect an application as malicious is flashlight application as it is only used to switch on the phone's camera flash as torch. If that is the case, there is no requirement for it to access user camera, microphone, photo or media, if it tries to access these, the user should have a suspicious eye on them says, kuskos (Bradbury, 2015).

3.3.1 Cellular Radio Back-doors

Firstly, let us have quick look on cellular radio system. It is basically a telephone transmission system which employs radio frequencies in full duplex mode with signal being either analogue or digital. Here powerful transmitter covers respective region, while coming to cellular radio system, it is replaced by smaller areas or cells as this enables the employment of less powerful transmitters. Centralized Mobile Telephone Switching Office (MTSO) controls network, which is basically the linkage of cells. The main function of MTSO is, once the mobile phone exit or enters within a specific range of a cell, the call is transferred to neighbouring cell (Oxford, 2017).

Also, the frequency reuse technique serves in cellular radio system to accomplish high capacity mobile radio system. The installation of this system in many countries has resulted as one of

the most rapidly growing and major demanded telecom application so far. The cellular radio adapts bounded frequency spectrum accessible for mobile radio by re-using same frequencies repeatedly and this is mainly achieved by isolating a large geographical area into number of minute nominal hexagonal areas and is termed as cells over entire country. Cluster arrangement is employed with respect to cells and the bandwidth allocated are isolated between the cells in each cluster (Rappaport, 1996).

Now moving onto the cellular radio backdoors, it is observed that smartphones equipped with mobile communication facility usually 3G or 4G LTE basically runs on two operating systems but not one. Normally, mobile phones have either Android or iOS operating system, apart from this end-user operating system, an operating system that controls radio related functions is running behind and is highly dependent on time resulting in requirement for Real Time Operating System (RTOS). The operating system controlling radio related function is the major problem resulting in cellular radio backdoor.

The Replicant developers, which is a pure free-software version of Android has potentially discovered security loop hole in some of the Samsung Galaxy phones and tablets, such that it is more vulnerable as device file system could be hacked and this is possible with devices such as Nexus S, Galaxy Note2, Galaxy Note, Galaxy Tab2, Galaxy SIII and Galaxy S2. As viewed by one of the Replicant project's developer Paul Kocialkowski, major issue lies in software that allows Android OS and cell radio to communicate each other (McAllister, 2014). This software allows modem to read, write and delete files on device thereby allowing to manipulate the major section of the device.

3.3.2 Samsung Galaxy S2 overview and its cellular radio backdoors issue discussion

The revolution in the field of mobile technology is taking place rapidly while at the same time, cybercrime has evolved and suspects in this field are termed as hacker. This type of crime has sidelined the traditional crime such as bank robbery. Now the personal devices are the main target that includes smartphone and tablets (Rondeau, 2014). Presently, user look for more ease of operation of device, portability, global connectivity so that time could be saved and all these advantages can be gained through smartphone only. But the issue arises here, reliance on smartphone blindly without verifying security features leads to leakage of personal information without being aware of this happening.

As reported by the developers of the Replicant software, which is basically a mobile OS for Android platform has discovered that one of the application provided in few Samsung galaxy

devices enables the permission to access personal files of user remotely. It was noticed by Replicant developer Paul Kocialkowski that, the issue mainly arises due to proprietary library that is responsible for Android OS to communicate with firmware running on cellular radio. Due to this software in some Samsung Galaxy devices allows the modem to control read, write and delete phone's personal storage files (Constantin, 2014).

Some of the devices that are vulnerable due to this problem includes Nexus S (I902x), Galaxy S (I9000), Galaxy S2 (I9100), Galaxy Note (N7000) etc. According to Kocialkowski, 'to overcome this backdoor issue, it is better to design a device that separates modem from rest of the components thereby avoiding the clutter with main processor, camera or GPS (Constantin, 2014).

3.4 Cellular modules

In the present market scenario, cellular connection is ubiquitous ranging from machines to smartphones and it is still undergoing massive expansion. Even though a lot of advancement has taken place in the recent years, cellular connection overpowers the Machine to Machine connection as the later accounts only 2% of the former one. The report by "Machina Research points claims, "the cellular technology will reach 2.6 billion growth rate by the end of 2022 (Arrow, 2015).

Presently, 2G is the basic cellular option employed with majority of M2M applications globally and will reach 22% by 2022. The current scenario is revolving around 3G and 4G LTE (Long Term Evolution) network and it is expected to reach 90% by 2022. Currently, several cellular modems are available to be employed for Code Division Multiple Access (CDMA) and Global system for Mobile Communications. There are four choices to choose for a cellular module solution and can be chosen based on the requirement. The four varieties are Chipset, Module, Embedded Module and Box Product (Arrow, 2015).

A quick overview on all the four types of cellular module is discussed in this section. Beginning with the Chipset cellular modem, which is basically designed for high volume applications involving Estimated Annual Usage (EAU) reaching 300K. Compared to other three types, the chipset is advantageous as it delivers smallest footprint solution and lowest Bill of Materials (BOM) cost. But, there are some downside to this type which includes, expensive compliance test and Non-Recurring Engineering (NRE) cost. Furthermore, it poses great design risks and requires long term project schedule (Arrow, 2015). Due to these limitations, the Chipset is not considered for the MEGAphone design.

Moving on to the Module, this a ubiquitous approach to include the cellular connectivity feature and one should ensure the certification of the module. Considering the certified module for the design ensures small footprint solution, standard foot print such as miniPCIe, low Bill of Materials (BOM) cost. Above all, this type fetches minimal Non-recurring Engineering (NRE) and compliance testing cost (Arrow, 2015).

The third type, Embedded module is ideal for incorporation in embedded products to enable the cellular connectivity. This type delivers cellular solution by meeting full compliance and even includes antenna for the embedded solutions. Price of this type of module is quite expensive when compared to module since, the design risk compliance and carrier certifications are fully tested by the vendor itself. The advantage of this type is basically it provides standard footprint with further option for the user to select between CDMA or GSM. Furthermore, the design risk is minimal and even a type to consider when targeting to release a product in the market in a very short period (Arrow, 2015). From the MEGAphone perspective, due to budget constraint, this type is not considered.

Ultimately, compared to all the above three types, Box product ensures the quickest time to market for cellular solution but, it is the most expensive compared to all other three solutions. Even though there are some advantages of this type such as, minimal design risk and additionally, it provides benefit for further development with respect to legacy hardware but replacing this is expensive in certain fields. There are numerous manufacturers for the present 4G cellular module for GSM such as Telit, SIMCom, Quectel, Sierra wireless to name a few (Arrow, 2015).

So far, the detailed discussion of all four major types of cellular module has been overviewed and at this stage, it is clearly evident that Module type stands out better compared to the remaining three. Added to these comparison, during the design process local vendor were very supportive to supply with miniPCIe module which will be discussed in detail in the later section. Considering Module type even ensures that the design is fundamentally independent of the cellular module, through the modular design which further allows the designer to simply select the one that is convenient and acceptable, because it can be replaced later.

3.5 FPGAs

Since, the Fairphone 2 as platform to design simple and secured smartphone has been ruled out, as per the plan Artix7 FPGA is substituting the design. A basic overview on the FPGA and its manufacturing companies and market share are reviewed in this section.

The Field-Programmable Gate Array (FPGA) is basically a silicon chip which accommodates configurable logic blocks (CLBs) in an orderly manner. The major advantage of FPGA is that it can be reprogrammed many times thereby enables to perform different function in just over a period of microseconds. But, the Application Specific Integrated Circuit (ASIC) enables to perform only one function for entire duration. FPGA should be guided through programming as it will be just blank and unable to communicate to its surrounding devices. This feature of FPGA is both advantageous and disadvantageous as it ensures flexibility while increasing the complexity of programming. (Wain et al., 2006).

FPGA should be guided through programming as it will be just blank and unable to communicate to its surrounding devices. This feature of FPGA is both advantageous and disadvantageous as it ensures flexibility while increasing the complexity of programming. There are several FPGA manufacturing companies such as Xilinx, Altera, Actel, Vantis, Lattice, Lucent, QuickLogic, Cypress. Among all, Xilinx and Altera has maximum market share. The below bar graph shows market share of all the manufacturers as of 2010 (Staff Writer, 2013).

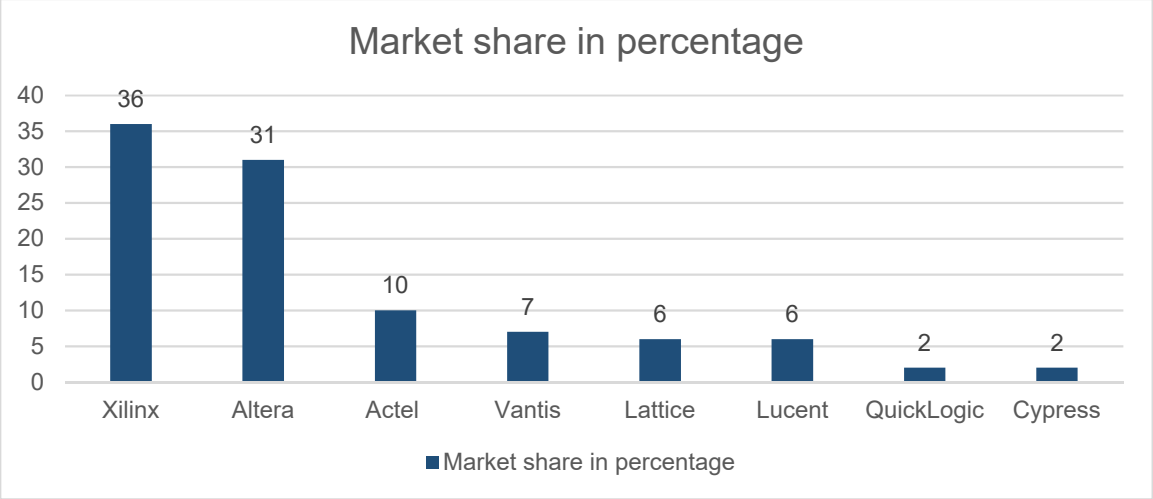

Figure 25: Market Share of FPGA Vendors, 2010 (Staff Writer, 2013).

Xilinx and Altera alone conquers the market by 90% approximate with former having a share of 47% and latter with 41% as of 2012. While in 2010 it was around 36% and 31%, and can observe exponential increase in growth within a span of two years. (Staff Writer, 2013). The Nexys4 DDR with Artix7 FPGA from Xilinx is the most popular FPGA as it has most of the functionalities on board that are required for the smartphone design. Furthermore, these boards are quite common in most of educational institution, as well as for practical analysis by developers. Further discussion regarding the specific FPGA is carried out in the later Chapter.

4. MIPI ALLIANCE

This Chapter overviews the organisation that is responsible for assigning the interface specifications to various functional modules in the Smartphone.

Mobile Industry Processor Interface (MIPI) Alliance is a non-profit global organisation which facilitates open membership. The main agenda of this organisation is to develop interface specification for mobile ecosystem also covering mobile oriented industries. The alliance originated in the year 2003 with prime members such as ARM, Intel, Nokia, Samsung, STMicroelectronics and Texas Instruments. Apart from these elite group of companies, globally the alliance has over 250 companies as member with 12 active working groups. In a decade, it has rolled out over 45 specifications entitled to mobile ecosystem only. Presently, the traditional mobile ecosystem has no barrier and has spread to even tablets and laptops. Due to this, MIPI alliance specification are not bounded to only mobile phones and thereby, these specifications are incorporated in tablets, cameras, industrial electronics, PCs, automotive, medical technologies and augmented reality (Boyce, 2008).

Diverse field has been merged under MIPI alliance to ease the mobile manufacturing and this includes handset manufacturers, device OEMs, software providers, application processor developers, semiconductor companies, application processor developers, test and equipment companies, also camera, tablet and laptop companies (Peter Lefkin and Wietfeldt, 2014).

In course of defining general mobile-interface specification, MIPI Alliance Working Groups has been established and it includes over 15 working groups that manages the responsibility of the entire mobile device design. Currently following working groups are active such as Analog Control Interface, Battery Interface (MIPI BIF), Camera (Camera Serial Interface), Debug, DigRF, Display (Display Serial Interface), High Speed Synchronous Interface, Low Latency Interface, Low Speed Multipoint Link (SLIMbus), Marketing, PHY, Reduced Input/output Working Group (RIO), RF Front-End Working Group (RFFE), Sensor Work Group (I3C), Software Investigation Group, Technical Steering Group, Test Working Group, UniPro even M-PHY, used by Mobile PCIe (Peter Lefkin and Wietfeldt, 2014).The MIPI specifications has paved the way for design process simplification, minimise design cost, affordable price. Most importantly, time span for components, features and services for market arrival has been reduced. Ultimately, MIPI specifications delivers on the basis of industry needs for a successful mobile design which mainly revolves around three characteristics such as power optimisation, high-performance operations and minimal EMI (Electro Magnetic Interference) (Boyce, 2008).

4.1 MEGA65 computer

MEGA65 is lot more than a retro computer and this design is implemented to continue the legacy of C65 heritage in 21st century. The MEGA65 is basically an 8-bit computer with computational speed being 50 times faster than a Commodore64 (C64) which was launched into the market during the year 1982 (Detlef Hastik et al., n.d.).

A quick overview on MEGA65 features as it includes, HD output, SD card support, Ethernet, Extended memory and lot more. Even with the inclusion of all these features, 8-bit feel is retained and adds up lot more fun. Furthermore, the MEGA65 is an open-source oriented with both, hardware and software designs are made available for free. With the design being open source, anyone can create prototype by dedicating substantial amount of time, effort and money (Detlef Hastik et al., n.d.).

In the process of deriving the MEGAphone design, MEGA65 design is considered as the foundation, as it is, easily interpretable and delivers high level security through simplicity. The entire schematic design of MEGA65 are available within the telecommunication laboratory. Some of the features included in the MEGAphone, are derived by considering MEGA65 schematic.

The hardware and software configuration of MEGA65 that includes the information regarding CPU, Speed, Direct Memory Access (DMA), Video controller, Sound, Media, Outputs, Inputs, Operating system, Form factor and Development options are made available through mega65.org web page (Detlef Hastik et al., n.d.).

5. DEVELOPMENT OF PROTOTYPE CONCEPT

The main intention of this project is to derive a Smartphone based on the MEGA65 project that is, MEGAphone which delivers design simplicity along with security. The features to be included in the MEGAphone, are identical to any phone like object, including tablets and phablets. But, there are some additional features that are included to ensure the security as per the requirement for the MEGAphone design other than normal smart-phone features and this is explained, under the respective functional blocks.

Ultimately, the end prototype is expected to be identical to a phone in terms of physical dimension. Working in that way, the dimension for each component selection are closely looked through. This can be noted in the upcoming chapters involving the component selection All the possible functional requirements of the MEGAphone are drawn and classified into two main categories namely, Critical components and Project application specific components. The two categories with their corresponding functionalities are listed below:

5.1 Critical components

- Single-cell LiFePO4 battery
- Micro-USB connector and charger
- Controlled output from Single-cell LiFePO4 battery
- Disabling the power supply to 4G LTE module
- Disabling the power supply to FPGA and dependent components via GPIO line of FPGA
- Enabling the 3.3V power supply to FPGA and dependent components by employing momentary switch
- Enabling the 3.3V power supply to FPGA and dependent components by an interrupt signal from 4G module
- Enabling the 3.3V power supply to FPGA and dependent components by an alarm signal from a Real-Time Clock
- Disabling the 3.3V supply to the Wi-Fi module via a signal from the FPGA board
- 3.3V supply to the 4G module controlled via signal from the FPGA, but only if physical switch is set to allow 4G module to be powered
- 3.3V supply to both the Wi-Fi module and the 4G module can be disabled via a physical switch labelled “Airplane mode”
- Real-time clock IC to maintain time and date when switched off, and to set alarms

- Power Indication LED for 4G LTE module
- Power indication LED for FPGA board
- Power Indication LED for Wi-Fi module
- Four RGB LEDs
- VGA connector providing video output with at least 4-bits colour depth per channel
- LCD panel connected via digital VGA interface with at least 6 bits colour depth per channel
- LCD capacitive touch digitiser via I2C/SPI to FPGA board
- Accelerometer connected via I2C to FPGA board
- PWM or similar adjustable backlight controller for LCD panel
- Micro SD card slot to be connected to FPGA board
- Speaker, ideally stereo, for audio output
- Microphone
- Headphone jack
- Audio output to speaker and headphone jack can be independently controlled
- Microphone input from headphone and internal microphone can be physically disabled with a switch
- Wi-Fi module interconnection with the FPGA via UART or SPI interface
- UART, I2C, input and output PCM audio interfaces and ADC interface between 4G module and FPGA
- Ambient light sensor
- Proximity sensor for blanking screen during calls

5.2 Project application specific components

- 25-pin DSUB connector for SX-64 keyboard
- 2 x 9-pin C64 Joystick Ports
- Four momentary - action user buttons
- Wireless co-existence interface between Wi-Fi and 4G modules
- Analogue battery voltage input
- 4 SIM card sockets connected to 4G module via SIM MUX ICs
- Commodore 64 disk drive interface

6. CANDIDATE FPGA MODULES FOR MEGAPHONE DESIGN

In Chapter 5, the various functional requirement that are necessary for the development of the MEGAphone functional design has been listed out. The FPGA module being the core in this design implementation as it drives various modules, it is necessary to analyse the FPGA features that satisfies the MEGAphone design requirement. During the process of analysis, the interface option, peripherals, input/ output pins and ports availability are taken into consideration. Furthermore, the dimension of the FPGA is one of the key thing to be considered to derive final prototype dimension close to phablet size (5.3 inch approximately). Consequently, with above framework as reference, the following section describes various FPGA possibilities to derive the MEGAphone design.

6.1 Nexys4 DDR FPGA by Digilent

The Nexys4 DDR board are ubiquitous and are employed in many electronic prototype designs. It is basically a digital circuit development platform based on Artix – 7™ Field Programmable Gate Array (FPGA) manufactured by Xilinx®. This FPGA incorporates certain unique features such as ample external memory and hence it is identified as high-capacity FPGA (Digilent, 2016). The peripheral and ports that are included in a Nexys4 DDR board are identified and depicted in the below image:

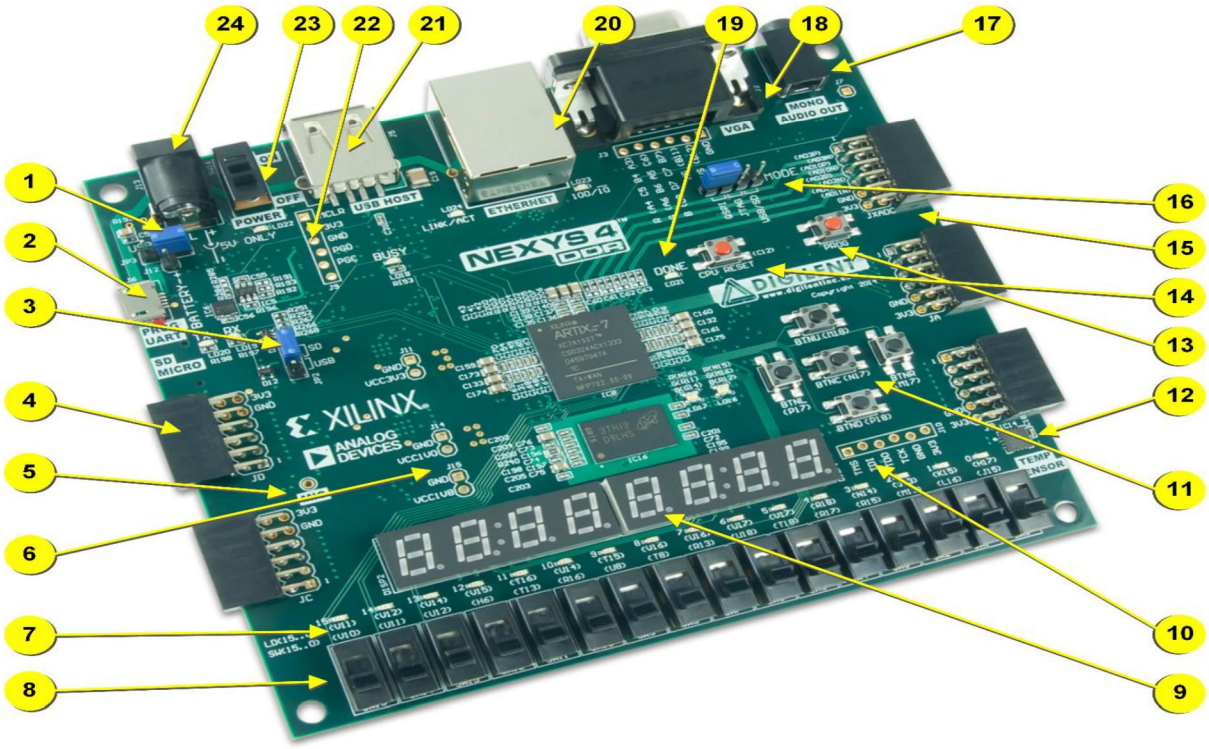

Figure 26: Nexys4 DDR features (Digilent, 2016).

The ports that are identified and numbered in the above image are described in the below table:

1	Power select jumper and battery header	**13**	FPGA configuration reset button
2	Shared UART/ JTAG USB port	**14**	CPU reset button (for soft cores)
3	External configuration jumper (SD/ USB)	**15**	Analog signal PMOD port (XADC)
4	PMOD port(s)	**16**	Programming mode jumper
5	Microphone	**17**	Audio connector
6	Power supply test point(s)	**18**	VGA connector
7	LEDs (16)	**19**	FPGA programming done LED
8	Slide switches	**20**	Ethernet connector
9	Eight digit 7-seg display	**21**	USB host connector
10	JTAG port for (optional) external cable	**22**	PIC24 programming port (factory use)
11	Five push buttons	**23**	Power switch
12	Temperature sensor	**24**	Power jack

Table 2: Ports and peripherals of Nexys4 DDR board. Data source (Digilent, 2016)

Due to this extensive range and features, it has the capability to host design, scaling from primary combinational circuit to robust embedded processors.

A quick overview on Nexys4 DDR board ports and peripherals has been completed. From the MEGAphone perspective for utilising the essential ports and peripherals that would result in implementing certain functional blocks of the MEGAphone includes, consideration of the audio connector for headphone jack feature implementation, VGA connector feature, microphone, micro SD card inclusion. All these feature implementation on the Nexys4 DDR board is simple and straight forward and the since schematic is open sourced, it would be helpful for considering this implementation as reference. But, there are many other functional blocks that are involved in the MEGAphone implementation and Nexys4 DDR board cannot cater all of them.

Furthermore, as mentioned earlier, the minimal dimension of the board is necessary to achieve MEGAphone prototype equivalent to the phone dimension and Nexys4 DDR board is unable to satisfy this criterion. But, feature that are implementable on this board as discussed are still considered for referencing in the final implementation of MEGAphone.

6.2 Artix-7 200T-2C Micro-module with XC7A200T-2C or TE0712-02 TRM FPGA

During the process of finding the FPGA board that ensures the implementation of maximum functional blocks of the MEGAphone along with the minimum dimension criteria satisfaction, the Trenz electronics, TE0712-02 TRM was noticed during the research.

This FPGA board includes a key feature that aids in implementing most of the functional blocks of MEGAphone and this possible because, it provides 158 FPGA I/O's (Input/ Outputs) through on board-to-board connectors. This is available through connecting plug-on module with 2 x 100 pin and 1 x 60 pin high speed hermaphroditic strips (Trenz Electronic, 2017b). These I/O's can be configured to any required interface protocol that are required for MEGAphone design and thereby the design process eases with reduced complication. The other feature of this board that would benefit if considered for the MEGAphone design are, dimension as this FPGA board measures around 4x5cm and this helps in deriving MEGAphone prototype identical to phone dimension. Also, supply voltage required for this FPGA module is 3.3 V which would be ideal to consider, as MEGAphone is planned to be powered by constant 3.3 V supply via single cell battery which will be discussed in the later section (Trenz Electronic, 2017b).

Figure 27: TE0712-02 TRM FPGA board (Trenz Electronic, 2017b).

The entire features included in this module can referred in the product datasheet (Trenz Electronic, 2017b). The module assembles multiple essential features on a tiny footprint even smaller than a credit card dimension and priced around 255 Euros, available through the official website.

As mentioned earlier, in the means of obtaining 158 FPGA I/O's (Input/Outputs) from TE0712-2 TRM FPGA board, plug-on board with 2 x 100 pin connector and 1 x 60 pins connector are necessary (Trenz Electronic, 2017b).

The Trenz electronic provides compatible 4 x 5cm plug on board for TE0712-02 TRM FPGA board and this module is named as TE0703 TRM. The TE0703 TRM plug on board has 2 x 100 pin plug in slot and 1 x 60 pin high speed hermaphroditic slot that is necessary for TE0712-02 TRM FPGA board to be plugged in. The TE0712-02 plug in board can be observed in the below image:

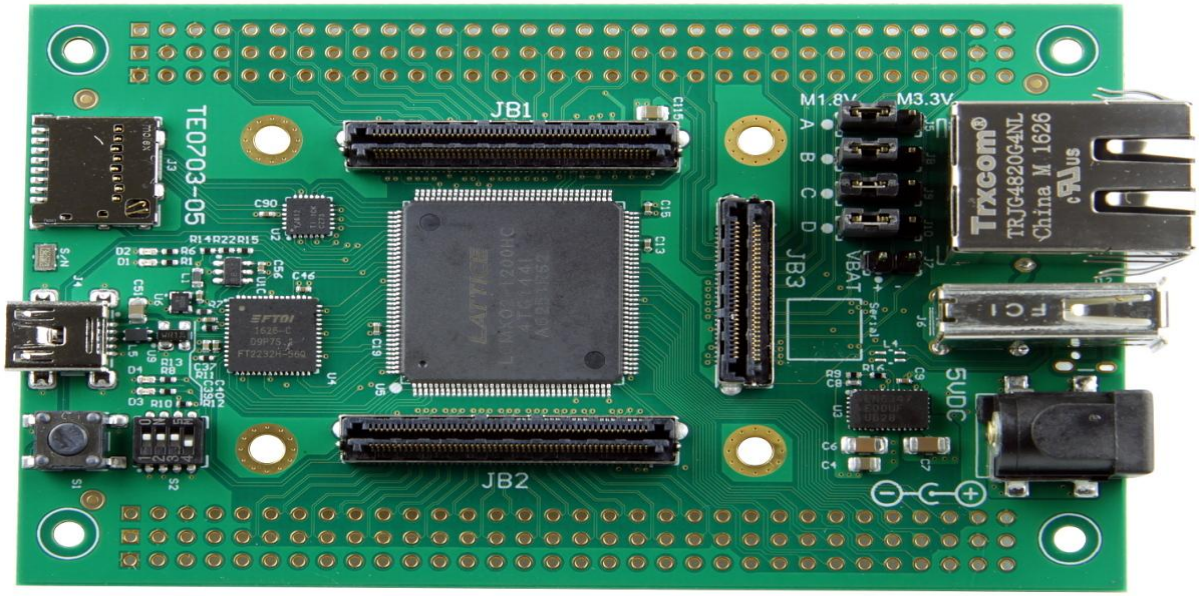

Figure 28: TE0703 TRM plug in board. (Trenz Electronic, 2017a).

Now, viewing from the MEGAphone perspective, to implement all the functional blocks derived in Chapter 5.1, a rough estimate of number of pins necessary for MEGAphone functional design implementation is around 95. Therefore, 100 pin external connector that are enabled to configure to any of the interface protocol are necessary and this board has ample number of those external connector pins than the required number and this can be observed in the Figure 28, with top and bottom corner of the board depicting the external connector slot and this should be plugged with suitable header pin to utilise. The TE0703 TRM plug in board cost around 99 Euros.

Incorporating both TE0712-02 TRM FPGA board and TE0703 TRM plug in board for the MEGAphone design would result in the bulkier prototype. Furthermore, the total price for both the modules will be 354 Euros approximately which is not economical as the total budget is limited and it would not be possible to purchase other functional modules required for the MEGAphone design. Consequently, this FPGA and plug in board is ruled out from the MEGAphone design.

6.3 Artix-7 100T, optical transceiver, 2x50 Pin, 2.54 mm pitch or TE0725-03 TRM FPGA

This FPGA module is manufactured by Trenz Electronic with part number TE0725-03-100-2CF. Unlike TE0712-02 TRM FPGA board discussed earlier, the TE0725 TRM FPGA board does not require plug in board as the external connectors and FPGA are housed on single board. The module is economical and have minimum dimension (73 x 35 mm) and almost identical to phone dimension. (Trenz Electronic, 2017c). With the above advantages taken into consideration, the TE0725-03 TRM FPGA module is considered for the MEGAphone design.

The entire features included with TE0725-03 TRM FPGA can be referred from the datasheet (Trenz Electronic, 2017c). The external connector slots are provided with 2 x 50 pin header (Trenz Electronic, 2016), has maximum spacing of 2.54mm. As mentioned by the company, the operating temperature depends on the applications it is being incorporated. But, all the parts assembled on FPGA board are bounded to commercial temperature range of 0° to 70°C which is satisfactory. The FPGA board is powered by 3.3 V single supply and are equipped with on board voltage regulators. The total number of input/output pins available through this FPGA board external connectors is 84, that is, 42 with connector J1 and remaining 42 with connector J2. This FPGA board has provision for JTAG and UART connector. The TE0725-03 TRM FPGA costs around 149 Euros and available through company official webpage (Trenz Electronic, 2017c).

Figure 29: TE0725-03 TRM FPGA board.

The above image depicts the TE0725-03 TRM FPGA board along with the POF (Plastic Optical Fibre) transceiver adapter being attached to the board and observable on the left side of the image. For the MEGAphone design, POF transceiver is not necessary.

Since there is no USB connectivity enabled in the TE0725-03 TRM FPGA, it is not possible to establish the serial communication with the FPGA board. But, this is very essential from MEGAphone design point of view. Fortunately, the TE0725-03 TRM FPGA board has provision for JTAG connector where, JTAG adapter is connectable. The information pertaining to JTAG connector can be referred under JTAG interface section. Here, the JTAG connector with Xilinx compatibility is essential as TE0725-03 TRM FPGA board runs on Xilinx's Vivado HL Web pack edition (Trenz Electronic, 2017c).

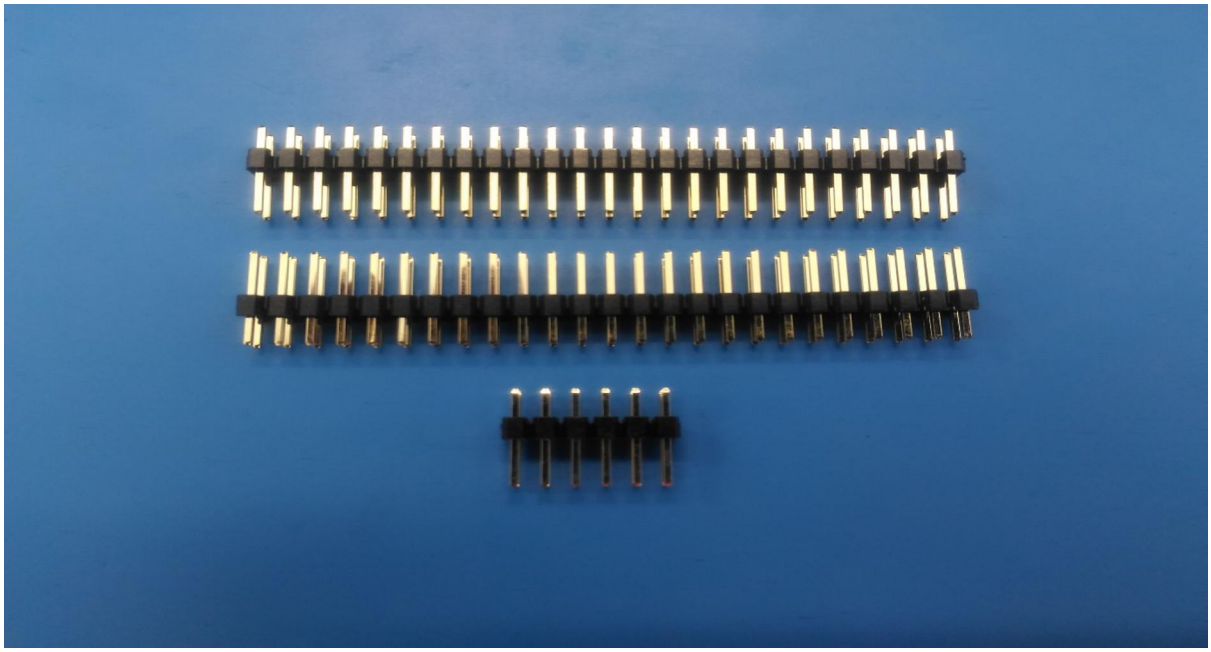

Figure 30: 2 x 50 Pin header for external connector slot and a 6-pin header for JTAG connector slot

Ultimately, the suitable adapter was found in terms of XMOD FTDI JTAG adapter along with Xilinx compatibility. Basically, this adapter is designed to function as a universal USB adapter and named as XMOD-USB-X. The XMOD-USB-X (TE0790-02) is assembled with two channels based on FTDI FT2232H USB2 HS interface chip and by default, the Port A is configured as JTAG and Port B as serial interface. The XMOD-USB-X module dimension measures around 20 x 25 mm (Trenz Electronic, 2017c).

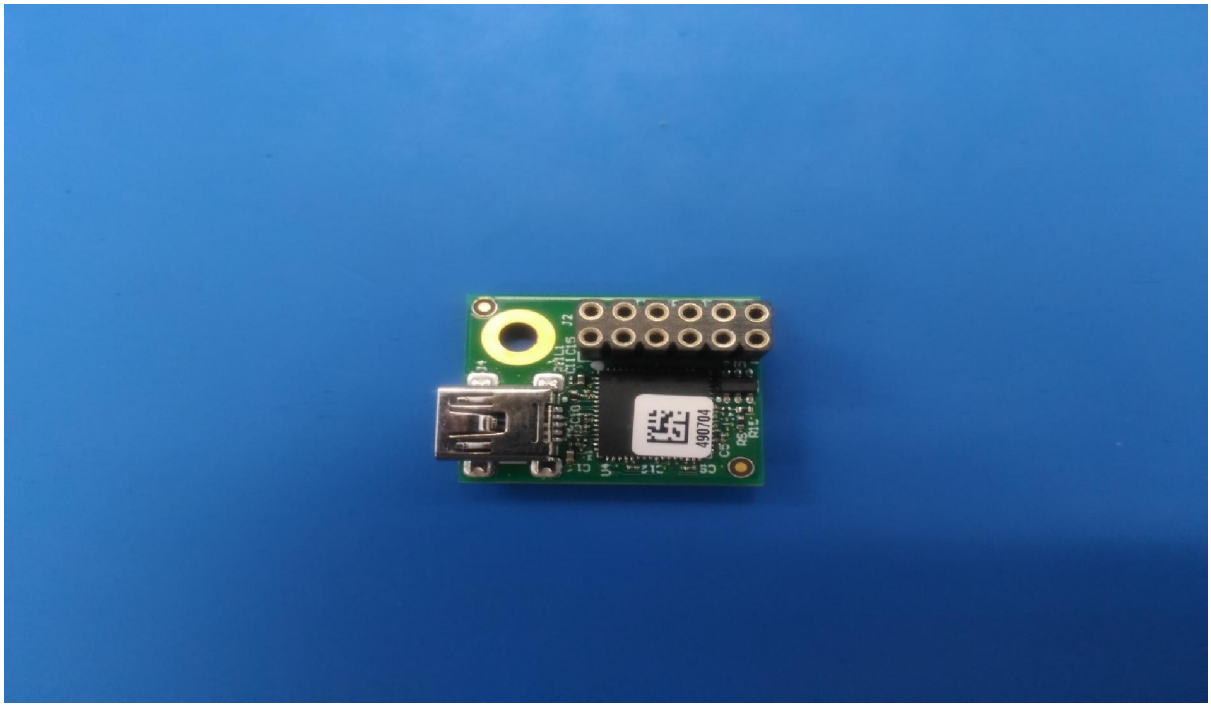

Figure 31: XMOD-USB-X (TE0790-02) JTAG adapter.

Finalising the FPGA for the MEGAphone design

The table has been constructed with various parameters necessary for the design as below:

Parameters	TE0712-02 TRM FPGA	TE0725-03 TRM FPGA
Dimension	50 mm x 40 mm	73 mm x 35 mm
Thickness	2.5 mm excluding attachment board	2.54 mm including header pin
Flash Memory	32 Megabyte QSPI	32 Megabyte
Weight (Plain module)	16 – 27 grams	8.5 grams
Number of IO (Input/ Output) pins	158 pins available via board-to-board connectors	87 pins available via header
Price	255 Euros	149 Euros

Table 3: Comparison between the TE0712-02 TRM and TE0725-03 TRM FPGA's

From the above table, it is evident that most of the characteristics between the two FPGA's varies. Initiating the discussion with dimension, the TE0712-02 TRM FPGA dimension is equivalent to square geometric shape, while the TE0725-03 TRM FPGA dimension is equivalent to rectangle geometrical shape (smartphone dimension) and this is more convenient when considering the 5-inch display.

The thickness of the TE0712-02 TRM FPGA is 2.5 mm excluding the attachment board. But, to obtain the 158 IO pins, the attachment board needs to be connected, which further increases the total thickness. On the other hand, the TE0725-03 TRM FPGA thickness is 2.54 mm including the header pins and even the attachment board is not necessary since, the header pins itself provides 87 IO pins which is sufficient for the MEGAphone design.

The plain module weight is minimum with respect to, the TE0725-03 TRM FPGA when compared to TE0712-02 TRM FPGA and this contributes in minimising the weight of MEGAphone design considerably.

The flash memory is updated with respect to TE0712-02 TRM FPGA as it embeds QSPI (Quad SPI flash), this speeds-up the operation considerably but it is, not necessary at this stage of MEGAphone design. Finally, the price difference is huge between the two FPGA's. The TE0725-03 TRM FPGA is more economic compared to the TE0712-02 TRM FPGA. Furthermore, the cost increases with respect to the TE0712-02 TRM FPGA as it requires the attachment board as discussed in section 6.2 earlier. Consequently, by analysis, TE0725-03 TRM FGA is considered for the MEGAphone design.

7. WIRELESS MODULES SELECTION FOR MEGAPHONE DESIGN

7.1 Wi-Fi modules

This era belongs to the complete evolution of smartphone and its advancement. As discussed in the earlier section regarding the various module integration that leads to the evolution of smartphone. In this section one of the most essential module embedded in the smartphone for internet connectivity that is, Wi-Fi module exploration is carried out in the means of selecting the appropriate one that meets the design specification. Before moving on to the module selection process, a quick overview on the evolution of Wi-Fi and it standards are described below.

The Wi-Fi was discovered by NCR Corporation/AT&T in Netherlands, during 1991. Basically, Wi-Fi is a non-technical term and it generally refers to 802.11 standards which originated in the year 1997 through IEEE. With gradual development, this IEEE standard has supported numerous application over a period of 13 years. Wi-Fi alliance was formed in the year 1999 with an intention to foster Wi-Fi advancements and certification to measure the success (Lemstra et al., 2010).

There are many Wi-Fi standards on which the modules are based on and it suits various application. The very first standard that is 802.11/Wi-Fi employed unlicensed radio spectrum and the data rate delivered by this standard was only 2 Mbps, also this standard is currently out of the market. The 802.11b was introduced in place of 802.11 with an improved data rate of up to 11 Mbps. Moreover, the 802.11b employs license-free ISM (Industrial, scientific and Medical) frequency band around 2.4 GHz (Lemstra et al., 2010).

The 802.11a standard was established during the same period of 802.11b but the market adoption happened much later than 802.11b. Even, 802.11a employs unlicensed ISM frequency band with higher frequency compared to former one as the frequency here is 5.8GHz with data rate of up to 54 Mbps. There are both advantages and disadvantages with this frequency band, as the interference is minimal with this frequency band being least employed. But, the reduction in RF signal range occurs as the frequency is maximum and moreover, the components are not economical compared to 802.11b (Lemstra et al., 2010).

There were many other standards that were established by IEEE over time to time with the combining advantages of the former versions along with the gradual improvement in data rates in each standard to suit different application and this includes 802.11g and 802.11n.

Collectively, 802.11a, 802.11b, 802.11g and 802.11n are the most adopted standards and are popularly known as Network bearer standards (Gupta, 2013).

It is unnecessary to go through all of them as the design requirements are very specific, two most widely accepted IEEE standards presently in the market are considered in the Wi-Fi module selection and they are 802.11a/b/g/n and 802.11b/g/n (Lemstra et al., 2010).

The selection process is carried out mainly due to, the innumerable modules available in the market by various manufacturers. Generally, the manufacturers will list the specific set of parameters that are incorporated in the module and this includes data rate, frequency range, RF band, certification and packaging type (Tektronix, 2014). Basically, with the aid of these parameters, the selection process of the module eases considerably.

The detail discussion regarding the various parameters consideration for the selection of Wi-Fi module is carried out in this section. The operating frequency band for 802.11 a/b/g/n standard is dual band, that is, it enables operation in 2.4 and 5 GHz frequency band. While, the 802.11b/g/n enables single band operation, that is, 2.4 GHz. To obtain the maximum data rate and far distance transmission, high output power is necessary. But, that fetches a lot of battery energy (Tektronix, 2014) , which is not required for the proposed design, since the design focus is on minimal power consumption.

The transmitting range of a module varies depending on the frequency band employed, standard protocol assigned and transmitting power of the module. It should be noted that, the 2.4 GHz band, over performs by delivering better transmitting range compared to 5 GHz frequency band. The data rate is also one of the factor to be considered for Wi-Fi module selection and this will be analysed for each individual module in the later section.

The antenna and connector type is another criterion that is considered for the Wi-Fi module selection. The Wi-Fi antennas are broadly classified as Omni directional and Directional, with former providing 360° coverage, while the later one direction specific and consequently bounded to a short range. Omni directional antennas are preferred for the proposed design. Moving on to the antenna connectors, on-board and external connector are the two types. The U.FL connectors serves the external option (Tektronix, 2014). With respect to this criterion, the selection is open for both the types.

Ultimately, other criteria such as operating temperature range, interface options, module size are discussed in this section. The operating temperature range differs for various modules and

one of the ideal operating temperature to be considered ranges from -40°C to 85°C (Tektronix, 2014). The interface option considered in the proposed design is, UART (Universal asynchronous receiver transmitter) and is one of the basic serial communication protocol that eases interfacing process. The proposed design is limited to the size and this is analysed in detail for each individual module.

The criteria for the selection of the module were framed and this included considering the module with minimal dimension, wide operating temperature range, targeting the module with supply voltage requirement in the range of 3.3 V to 3.8 V, serial interface protocol (specifically UART), cost effectiveness, antenna option and the frequency band operation were left open.

The following section involves the analysis of various Wi-Fi module explored that would possibly fit into the proposed design and of are as follows:

Type 1HD

Figure 32: Type 1 HD module (Murata, n.d.-c).

The following data table depicts the configuration of this module:

Frequency	**2.4 GHz**
Chipset	**Cypress(CYW43438) & STM32 (ARM Cortex-M4)**
Processor	**STM32 ARM Cortex-M4**
Antenna	**On-board**
Operating Temperature	**-20 to +70°C**
Dimension	**21.0 x 17.5 x 2.3 mm**
Supply Voltage (V_{dc})	**3.3 V**
Host Interface	**UART/SPI**
Host Interface Other	**GPIO/I2C/JTAG**
Interface Voltage (V_{dc} for V_{IO})	**3.3 V**
I/O Interface	**GPIO**

Table 4: Type 1HD features (Murata, n.d.-c).

This module is manufactured by one of the leading Wi-Fi module manufacturers, Murata. The Type 1HD module is designed by amalgamating Network bearer standards, that is, 802.11b/g/n. As each IEEE standard has various data rate individually such as 11 Mbps, 54 Mbps and 65 Mbps for 802.11b, 802.11g and 802.11n correspondingly with all standards operating under licence free ISM frequency band, that is, 2.4 GHz. Consequently, transmitting power for the data rates 11 Mbps, 54 Mbps and 65 Mbps are +17 dBm, +13 dBm and +12 dBm respectively. (Murata, n.d.-c). The operating temperature is satisfactory but, the dimension is quite large as the size constraint is one of the vital criteria in the selection of the module to the design. Regarding unit price for this module, the request for the quotation was raised and the company replied with some specific question which was unanswerable as it was based on employee and employer perspective. Thus, the price of the unit was unavailable.

Type 1GC-Imp005

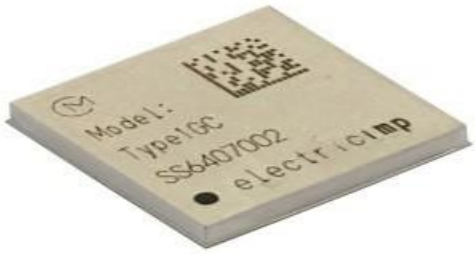

Figure 33: Type 1GC Imp005 module (Murata, 2016).

The following data table depicts the configuration of this module:

Frequency	**2.4 GHz and 5 GHz**
Chipset	**Cypress(CYW43907)**
Processor	**ARM Cortex-R4**
Antenna	**External**
Operating Temperature	**-30 to +85°C**
Dimension	**10.0 x 10.0 x 1.2 mm**
Supply Voltage (V_{dc})	**3.3 V**
Host Interface	**UART/SPI/USB**
Host Interface Other	**GPIO/I2C/Ethernet (RMII)**
Interface Voltage (V_{dc} for V_{IO})	**3.3 V**
I/O Interface	**GPIO**

Table 5: Type 1GC Imp005 features (Murata, 2016).

This module is manufactured by one of the leading Wi-Fi module manufacturers, Murata. The Type 1GC-Imp005 module is designed by amalgamating Network bearer standards, that is 802.11a/b/g/n. As each IEEE standard has various data rate individually such as 11 Mbps, 54 Mbps and 65 Mbps for 802.11b, 802.11g, 802.11a and 802.11n correspondingly. Consequently, transmitting power for the data rates 11 Mbps, 54 Mbps and 65 Mbps are +17 dBm, +13 dBm and +12 dBm respectively. In this module, the data rate for both 802.11a and 802.11g standards remains identical with 54 Mbps. But the frequency support varies as 802.11a operates in 5GHz ISM band while, the 802.11g operates in 2.4 GHz ISM band with both bands being licence free. On the other hand, the IEEE 802.11b and 802.11n standards have data rate of 11 Mbps and 65 Mbps respectively and supports identical licence-free ISM frequency band of 2.4 GHz.

The maximum operating temperature range has increased while minimum operating temperature range has decreased compared to Type 1HD module, the dimension aspect is meeting the criteria as design requires minimal size. The single, Type 1GC-Imp005 module costs around $24.50 and is available through Mouser electronics. The manufacturer part number for this module is LBWA1UZ1GC-901.

Type 1GC

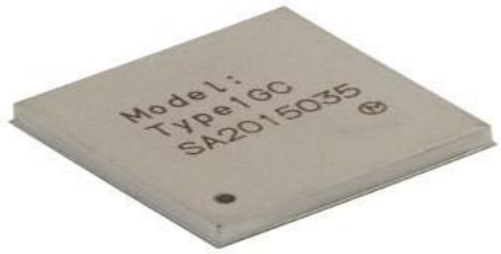

Figure 34: Type 1GC module. Image source. (Murata, n.d.-b)

The following data table depicts the configuration of this module:

Frequency	**2.4 GHz and 5 GHz**
Chipset	**Cypress(CYW43907)**
Processor	**ARM Cortex-R4**
Antenna	**External**
Operating Temperature	**-30 to +85°C**
Dimension	**10.0 x 10.0 x 1.2 mm**
Supply Voltage (V_{dc})	**3.3 V**

Host Interface	UART/SPI/USB
Host Interface Other	GPIO/I2C/Ethernet (RMII)
Interface Voltage (V_{dc} for V_{IO})	3.3 V
I/O Interface	GPIO

Table 6: Type 1GC features (Murata, n.d.-b).

This Wi-Fi module is manufactured by Murata and it delivers top notch services in terms of quality and most importantly, it is user friendly. This module is based on Cypress Semiconductor corporation. The key feature of this module is cost effectiveness thereby providing the solution to wireless connectivity. This module has data rate of all four IEEE standards and they are 11 Mbps, 54 Mbps and 65 Mbps and thereby data rate varies from minimum to maximum which covers extensive range. This module is RoHS compliant. It is noticeable that, only the chipset varies between the Type 1GC Imp-005 and Type 1GC with rest of the features remains identical. The unit price for this module is unavailable.

Telit WE866A1-P

Figure 35: Telit WE866A1-P module (Telit, 2017b).

The following data table depicts the configuration of this module:

Frequency	2.4 GHz, channel 1-13*(2.412 GHz – 2.472*)*Standalone value
Chipset	xE866 Telit FF
Antenna	External
Operating Temperature	-40 to +85°C
Dimension	15 x 19 x 2.2 mm
Supply Voltage (V_{dc})	3.1 - 4.5 V
Host Interface	4-wire UART
Host Interface Other	SPI
Interface Voltage (V_{dc} for V_{IO})	3.8 V

Table 7: Telit WE866A1-P features (Telit, 2017b).

This module has some identical features such as, Powerful Crypto Engine for fast and secure Wi-Fi. This module has considerably higher data rate compared to other modules which is about 72.2 Mbps. The operating temperature for this module is quite satisfactory. This module has many approvals such as CE, FCC/IC certified and Wi-Fi certified and additionally, the IEEE 802.11b/g/n approved as it meets the specifications for implementing wireless local area network (WLAN). The IEEE 802.11 b/g/n basically supports the bandwidth of up to 54 Mbps and to function for a wider range, the module employs 2.4 GHz frequency. This module provides a high-end security features. The module design is based on the combination of Network bearer standards, that is, 802.11b/g/n. As per the data obtained from R0ound Solutions website, the unit price of Telit W866A1-P is around 17.80€ and the Australian dollar equivalent price is around $26.70.

Telit GS2101MIP

Figure 36: Telit GS2101MIP module (Telit, 2017a).

The following data table depicts the configuration of this module:

Frequency	**2.4 GHz – 2.495 GHz**
Antenna	**External (U. FL connector) or On-board PCB trace antenna**
Operating Temperature	**-40 to +85°C**
Dimension	**18 x 25 x 2.7 mm (shield)**
Host Interface	**UART, SPI, SDIO**
Operating Voltage	**2.7 - 3.6 V**
I/O Voltage	**2.7 - 3.6 V**
I/O Interface	**SPI, UART, SDIO, I2C, I2S, GPIO, ADC (16 bit), ADC (12 bit), JTAG**

Table 8: Telit GS2101MIP (Telit, 2017a).

The GS2101MIP is manufactured by Telit communications S.p.A. This module has some exciting features and advantages such as, supporting Host-less mode that is with no external MCU (Microcontroller), running full Wi-Fi and TCP/IP networking stack. While coming to Host mode, it has most detailed AT command library connecting to 8/16/32 – bit host microcontroller using UART, SPI or SDIO interfaces. It delivers high speed secure Wi-Fi and Internet connectivity to any device incorporating a microcontroller and serial host interface. It also includes dynamic power management modes resulting in delivering ultra-low-power consumption. Additionally, it facilitates Wi-Fi Protected Set-up (WPS). The Telit GS2101MIP module design is based on the combination of Network bearer standards that is 802.11b/g/n. The information about the price of this module was obtained through Round Solutions and it cost around 19.80€ per unit. The equivalent price in Australian dollars is around $29.70.

Finalising a Wi-Fi module from the candidate list for the MEGAphone design

Now, among all the probable components discussed so far, the best one is selected by analysing its various features and that satisfies specified design criteria drawn to select the Wi-Fi module in a best possible way. A table is constructed to carry out the comparison between each other:

Module	Dimension	Operating temperature	Input/ Output Interface	Operating Voltage	Price
Type 1HD	21.0 x 17.5 x 2.3 mm	-20 to +70°C	UART, SPI	3.3 V	NA
Type 1GC-Imp005	**10.0 x 10.0 x 1.2 mm**	-30 to +85° C	UART, SPI, USB	3.3 V	$24.50
Type 1GC	**10.0 x 10.0 x 1.2 mm**	-30 to +85°C	UART, SPI, USB	3.3 V	NA
Telit WE866A1-P	15 x 19 x 2.2 mm	**-40 to +85°C**	4-wire UART, SPI	3.1 - 4.5 V	$26.70
Telit GS2101MIP	18 x 25 x 2.7 mm	**-40 to +85°C**	**SPI, UART, I2C**	**2.7 - 3.6 V**	$29.70

Table 9: Wi-Fi module comparison

In the above table, the highlighting feature of each module are bold faced. The frequency of operation is not identical for all the Wi-Fi modules discussed so far. Some of them operates in single frequency band that is 2.4 GHz and the module that fall under this category includes

Type1 HD, Telit WE866A1-P, Telit GS2101MIP. While, the dual frequency operation enabled modules has the capability to operate in both frequency band such as 2.4 GHz and 5 GHz. The module under this category includes Type1GC-Imp005 and Type 1GC.

The single band operating module with IEEE standard 802.11 b/g/n has some disadvantage compared to dual frequency band module with IEEE standard 802.11 a/b/g/n. The 2.4 GHz frequency has been adopted since long time and are ubiquitous. But, this has raised some serious issues such as, interference and the network jam. To overcome this, 5 GHz along with 2.4 GHz frequency band was introduced and is slowly gaining the market. The dual band operation eliminates the interference issue by switching to 5 GHz frequency band. Furthermore, with dual band operation enabled, the module can switch over to either 2.4 GHz or 5 GHz range depending on the source router frequency. This switch over also helps in overcoming the issues caused by 5 GHz frequency range such as poor penetration through the solid objects and less area coverage which can be improved by switching to 2.4 GHz. So, it is better to select one of the module with IEEE standard a/b/g/n. Adding this filter, only two module remains for selection and that includes Type 1GC-Imp005 and Type 1GC modules manufactured by Murata.

The size constraint, is one of the criteria in selecting the best module. Now, with Type 1GC-Imp005 and Type 1GC, the dimension variation needs to be observed. But here, both module dimension is measuring around 10.0 x 10.0 x 1.2 mm. Thus, both the module satisfies the size constraint criteria.

The operating temperature is required to be wide ranged and both Type 1GC-Imp005 and Type 1GC modules operates at temperature ranging from minimum of -30°C and maximum of up to 85°C. Again, both the module has identical operating temperature and satisfies the criteria of wide operating temperature range. Thus, both module can be considered.

Ultimately, the price difference is figured out between Type 1GC-Imp005 and Type 1GC. Since, the unit price for Type 1GC is unavailable and moreover, the datasheet is not available. Consequently, the Type 1GC-Imp005 is considerable to be employed for the proposed design with single module priced around $24.50 and is available through Mouser electronics.

7.2 Bluetooth modules

The minimal distance wireless-communication is achievable through a sophisticated technology known as Bluetooth. The operating frequency ranges between 2.400 GHz to 2.4835 GHz and belongs to 2.4 GHz ISM frequency band (Bluetooth).

In the present mobile world, there are ample number of module manufactures with plenty of options for selection which is good for the smartphone manufactures to select the best and sets the new target for each module manufacturing companies. Flip side of it is that, it also challenges the designer to pick the best. Consequently, various parameters are framed, so that it meets the required design specification.

Generally, differentiating each manufacturer module is carried out by following parameters such as transmission distance, transmission rate, certification, frequency band, operating temperature, cost effectiveness, power consumption dimension and possible interfaces. One more aspect that plays a vital role in selection of the Bluetooth module is the application that is being targeted that is various Bluetooth profile are present for different applications. Some of the leading Bluetooth profile that are ubiquitous includes headset profile (HSP), which is basically relates to hands-free Bluetooth headset. The human interface device (HID), is basically a profile incorporated to enable the input devices that are user controlled such as, keyboard, mice and joysticks. So, to establish the connection between Bluetooth devices, the profile of both should be identical. The design is targeted to the assemble Bluetooth module that is having UART interfaces, which is basically serial communication. The serial communication interface replacement is possible through (SPP) serial port profile (DeCuir, 2014).

As mentioned earlier, various parameters that are employed by manufacturers to distinguish are even considered as criteria here in the selection of Bluetooth module for the MEGAphone design. The transmission rate varies depending on the power class of the Bluetooth module to which it belongs to. In general, the transmission rate or the range is interrelated to the power class it is designated to. The overview of various power classes of Bluetooth module is depicted in the table below:

Class	Maximum Output power in dBm	Maximum Output power in mW	Maximum Range
Class 1	20 dBm	100 mW	100 m
Class 2	4 dBm	2.5 mW	10 m
Class 3	0 dBm	1 mW	10 cm

Table 10: Power classes of Bluetooth module (DeCuir, 2014).

Currently trending Bluetooth technology are mainly classified into two types such as, classic and low-energy (LE). These two types are distinguished based on the transmission rate with classic Bluetooth offering higher transmission rate and thus suitable for the application such as Bluetooth headset for top notch music output (Bluetooth).

The classic Bluetooth is further classified as basic rate (BR) and enhanced data rate (EDR). Moving onto the low-energy (LE) Bluetooth, the transmission rate is considerably low as this type of Bluetooth mainly focuses on durability of electronics for long time and thereby delivers the information transmission at elementary level. The low-energy Bluetooth module cannot be considered for the bulk data transmission at high speed (Bluetooth).

The Bluetooth low-energy (LE) modules are preferred for the selection process due to its minimal power consumption and moreover, the proposed design does not target higher transmission rate.

The operating frequency band of Bluetooth, lies in the range of 2.4 to 2.4835 GHz with classic Bluetooth accommodating 79 channels in this range having frequency interval set to 1 MHz. Contrary to this, the low-energy Bluetooth accommodates 40 channels in the same range with frequency interval upgraded to 2 MHz. The target of low-energy Bluetooth module is to minimise the power consumption and cost (Bluetooth).

There lies some confusion even in the selection of Bluetooth low-energy (LE) module and to overcome this, the Bluetooth SIG (Special Interest Group) has assigned 2 types of certification marks such as Bluetooth Smart and Bluetooth Smart Ready (Bluetooth). The Bluetooth SIG, basically manages the Bluetooth standards and are responsible for issuing license for various Bluetooth technologies and trademarks for the manufacturers (Haartsen et al., 1998).

The Bluetooth module selection is carried out by considering all the above criteria as base for each individual modules of different manufacturers. Also, a refined set of criteria for the MEGAphone design is framed and this includes, wide operating temperature range, minimum

cost, minimal dimension of the module, wide operating voltage range, minimal power consumption module (Bluetooth Low Energy), serial interface protocol (UART, I2C, SPI) and the data rate consideration is non-specific. The following section depicts the information regarding the researched Bluetooth module for the MEGAphone design.

Type 1BX

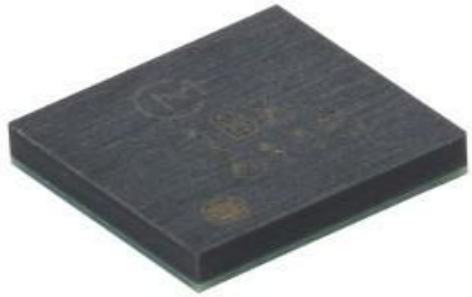

Figure 37: Type 1BX module (Murata, n.d.-a).

The following data table depicts the configuration of this module:

Frequency	**2.4 GHz**
Chipset	**CSR8811**
Processor	**No**
Antenna	**External**
Operating Temperature	**-30 to +85°C**
Dimension	**5.0 x 4.5 x 1.0 mm**
Supply Voltage (V_{dc})	**1.20 to 3.60 V**
Host Interface BT	**UART/PCM/I2S**
Interface Voltage (V_{dc} for V_{IO})	**1.2 to 3.6 V**
Bluetooth	**v4.0 BR/EDR/LE**

Table 11: Type 1BX features (Murata, n.d.-a).

The above module is compact in size, the operating frequency range is from 2402 MHz – 2480 MHz. The interface that is focussed in this research for Bluetooth module is UART and is present in the above module. With respect to cost, details were not available from official website. The main drawback of this module is that, the antenna lies externally. This module power class is confined to both class 1 and class 2 and its maximum output power is 13 dBm. This Bluetooth module is version 4.0 based and the highlighting feature of this version is low energy that is Bluetooth Low Energy (BLE). With the BLE mode active, the range is

suppressed considerably, including data flow, so that the minimal power is utilised in this process. This feature is mainly targeted to battery operated devices.

This module has both Basic Rate (BR) and Enhanced Data Rate (EDR). It has to be noted that, the data rate varies between these two types with former one having approximately half the data rate compared to the latter one (DeCuir, 2014). With regards to compliance, this module is RoHS compliant.

Type ZY

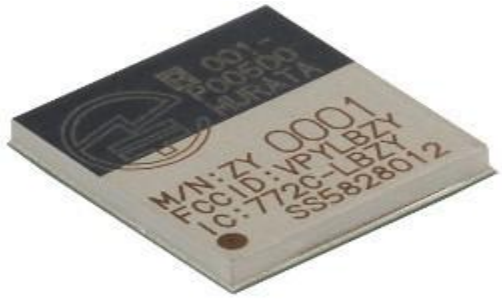

Figure 38: Type ZY module (Murata, 2015).

The following data table depicts the configuration of this module:

Frequency	**2.4 GHz**
Chipset	**DA14580**
Processor	**ARM Cortex-M0**
Antenna	**On-board**
Operating Temperature	**-40 to +85°C**
Dimension	**7.4 x 7.0 x 1.0 mm**
Supply Voltage (V_{dc})	**2.35 to 3.3 V**
Host Interface BT	**UART/SPI/I2C**
Interface Voltage (V_{dc} for V_{IO})	**2.35 to 3.3 V**
Bluetooth	**v4.1 LE**

Table 12: Type ZY features (Murata, 2015).

The Type ZY module is manufactured by Murata, it has data rate of 1 Mbps. This module is RoHS compliant and the dimension is considerably small. The antenna is assembled to the module and operating temperature is wide ranged. The maximum output power delivered by this module is 0 dBm and thus, the power class of this module is class 3 and this analysis is carried out with table 10, as reference. The unit price of this module is around $14.45. This module is available through Mouser Electronics.

Microchip Technology BM70BLES1FC2-0002AA

Figure 39: BM70BLES1FC2-0002AA module (Microchip, 2015a).

The following data table depicts the configuration of this module:

Frequency	**2.4 GHz**
Processor	**No**
Antenna	**On-board**
Operating Temperature	**-20 to 70°C**
Dimension	**20.0 x 13.0 x 2.4 mm**
Supply Voltage (V_{dc})	**3.3V**
Host Interface BT	**UART/SPI/I^2C**
Interface Voltage (V_{dc} for V_{IO})	**1.9 to 3.6 V**
Bluetooth	**v4.1**

Table 13: BM70BLES1FC2-0002AA features (Microchip, 2015a).

The BM70 Bluetooth module has many unique feature of low energy consumption and thus, it is termed as Bluetooth Low Energy (BLE) Module (Microchip, 2015a). Additionally, the dimension of this module is minimum and essentially satisfies the size constraints criteria. The module is surface mountable.

The power management in this module is organised very well through two low-power modes enabling. During the sleep mode, the module is activated through GPIO or internal timer, thereby it saves a lot of power from module being inactive when there is no necessity for it to function. The maximum output power delivered by this module is 2 dBm and it is equivalent to 1.6 mW and this conversion is obtained through dBm to milli-watts converter. The power class of this module is not mentioned. But, according to the maximum output power data, it can be predicted that it closely belongs to class 2. The module is RoHS compliant. The price for single unit is around $9.94.

Telit BlueMod+S42

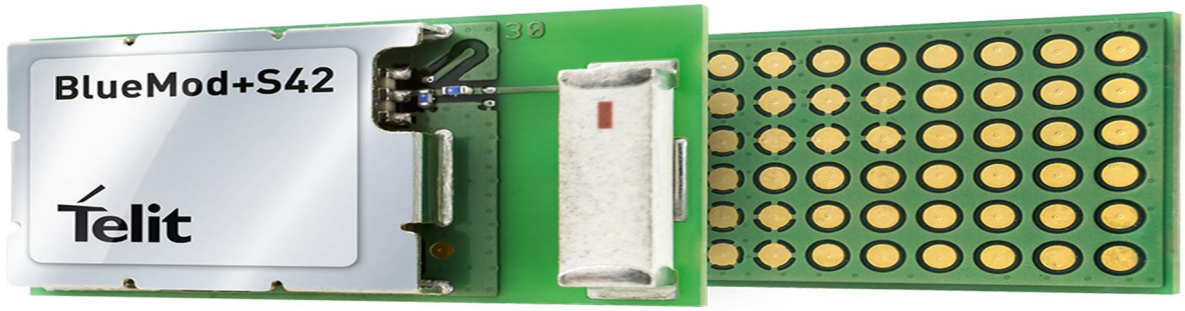

Figure 40: Telit BlueMod+S42 module (Telit, 2016).

The following data table depicts the configuration of this module:

Frequency	**2.4 GHz**
Chipset	**Based on the nRF52 Nordic**
Processor	**No**
Antenna	**On-board (Ceramic antenna)**
Operating Temperature	**-40 to +85°C**
Dimension	**17 x 10 x 2.6 mm**
Supply Voltage (V_{dc})	**3.3 V**
Host Interface BT	**UART: 9600 bps - 921600 bps (asynchronous)**
Other Interfaces	**SPI, PWM, ADC, I^2C**
Interface Voltage (V_{dc} for V_{IO})	**1.8 to 3.6 V**
Bluetooth	**v4.2 qualified module**

Table 14: Telit BlueMod+S42 features (Telit, 2016).

The BlueMod+S42 is basically future generation(Telit, 2016) Bluetooth single mode module with its design based on nRF52 Nordic chipset. This module supports NFC (Near Field Communication) functionality and is identical to the one present in Nordic nRF52 chip. This NFC handover eases device pairing and establishment of connection. This module is ideally designed for smartphone connectivity.

This module is low power consumption enabled and is designed in such a way that it eliminates cable incorporation. The unit price for this module as obtained through Digi-Key website is 11.70$ (USD) and the equivalent price in the Australian dollar is approximately $15.40.

This module is not based on the serial port profile (SPP) and it includes terminal I/O profile and this function is identical to SPP. The terminal I/O profile delivers point-to-point connection

also provides flow control over-the-air and this favours the application that involves minimal data rate and open data exchange.

This module is authorised by AT command interface and incorporates Bluetooth Low Energy (BLE) feature. This module is single mode enabled, that is the classic Bluetooth operation is absent and supports only BLE. The power class of this module is class 2 and this is drawn by comparing with data in table 10, as the maximum transmitting power is 4 dBm for this module. Ultimately, the module is RoHS compliant.

All the Bluetooth modules discussed above so far has multiple interfacing options along with UART. Since the target interface options that is required in the design is UART, narrowing the research for the Bluetooth module that are confined only to UART interface are discussed below:

Type VZ

Figure 41: Type VZ module (Murata, n.d.-d).

The following data table depicts the configuration of this module:

Frequency	**2.4 GHz**
Chipset	**TI CC2541**
Processor	**No**
Antenna	**On-board**
Operating Temperature	**-10 to +60°C**
Dimension	**20.0 x 13.0 x 2.4 mm**
Supply Voltage (V_{dc})	**3.3 V**
Host Interface BT	**UART**
Interface Voltage (V_{dc} for V_{IO})	**2.1 to 3.6 V**
Bluetooth	**v4.0 LE**

Table 15: Type VZ features (Murata, n.d.-d).

The Type VZ module is a SMART Bluetooth module and it has some unique feature of plug-in device and this basically enables Bluetooth v4.0 low energy standard. The highlighting feature of this module is data rate and it is close to 1 Mbps. The module operates normally at a very minimum temperature of -10℃ and maximum temperature is quite satisfactory. Furthermore, the size constraint criteria are not met, as the dimension is large compared to Type 1BX. Finally, the price is not mentioned in the official website as the single unit purchasing option is unavailable. This module also has the Bluetooth Low Energy (BLE) feature. The power class to which this module belongs to is, class 2. The module is not RoHS compliant.

BGM121

The BGM121 Blue Gecko Bluetooth SIP module is manufactured by Silicon Lab's. This module features transmission power of +8 dBm. One of the selection criteria in this design for the Bluetooth module being size constraint and this module satisfies, as this is designed for applications that requires ultra-small size. This module also delivers high performance RF and above all it consumes less power.

The following data table depicts the configuration of this module:

Frequency	**2.4 GHz**
Chipset	**32-bit 38.4 MHz ARM Cortex-M4**
Processor	**No**
Antenna	**Integrated, high performance enabled**
Operating Temperature	**-40 to +85°C**
Dimension	**6.5 x 6.5 x 1.4 mm**
Supply Voltage (V_{dc})	**1.85 to 3.8V single power supply, 2.4 to 3.8 in DC-DC mode**
Host Interface BT	**UART**
Other Interfaces	**SPI, Smartcard (ISO 7816), IrDA, I^2S, I^2C**
Bluetooth	**v4.2 qualified module**

Table 16: BGM 121 features (Silicon Labs, n.d.).

The BGM121 module is RoHS compliant. This module is available through Mouser Electronics with single unit priced around $9.21. Since the maximum output power or transmit power for BGM121 is 8 dBm, this module belongs to class 1, when analysed with table 10 as reference added with Bluetooth smart.

PAN1316

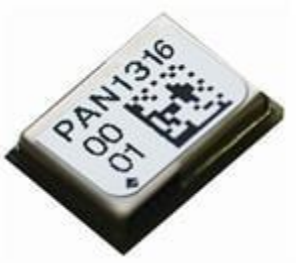

Figure 42: Panasonic 1316 module (Panasonic, 2017).

The following data table depicts the configuration of this module:

Frequency	**2.4 GHz**
Chipset	**No**
Processor	**No**
Antenna	**On-board**
Operating Temperature	**-20 to +70°C**
Dimension	**9.5 x 9.0 x 1.8 mm**
Supply Voltage (V_{dc})	**2.2 to 4.8 V**
Host Interface BT	**UART**
Bluetooth	**V4.0**

Table 17: Panasonic 1316 features (Panasonic, 2017).

This module is manufactured by Panasonic with part number ENW89823C2JF. The version of this module is based on version 4.0 that is, Bluetooth Low Energy enabled. Due to BLE feature, this module supports the sleep mode and is activated only when an event occurs. The maximum output power or transmission power delivered by this module is 10 dBm and it belongs to class1, class2 with Bluetooth smart. This module provides data rate of up to 2.1 Mb/s. Furthermore, dual mode option is available with Bluetooth Low Energy (BLE) and Classic Bluetooth function ensembled on a single module. Furthermore, this module is designed for minimum range operation. Ultimately, the module is RoHS compliant with priced around $18.26 available through Mouser electronics.

Finalising a Bluetooth module from the candidate list for the MEGAphone design

Module	Dimension	Operating temperature	Input/ Output Interface	Operating Voltage	Price
Type 1BX	**5.0 x 4.5 x 1.0 mm**	**-30 to +85°C**	**UART/PCM/I2S**	**1.2 – 3.6 V**	NA
Type ZY	**7.4 x 7.0 x 1.0 mm**	**-40 to +85°C**	**SPI, UART, I2C**	2.35 - 3.3 V	$14.45
BM70BLES1FC2-0002AA	20.0 x 13.0 x 2.4 mm	-20 to +70°C	UART, SPI, USB	3.3 V	**$9.94**
Telit 53346-02	17 x 10 x 2.6 mm	**-40 to +85°C**	UART	3.3 V	$15.40
Type VZ	20.0 x 13.0 x 2.4 mm	-10 to +60°C	UART	3.3 V	NA
BGM121	**6.5 x 6.5 x 1.4 mm**	**-40 to +85°C**	UART	**1.85 – 3.8 V**	**$9.21**
PAN1316	9.5 x 9.0 x 1.8 mm	-20 to +70°C	UART	**2.2V - 4.8 V**	$18.26

Table 18: Bluetooth module comparison

The above table depicts the comparison of various parameters of individual Bluetooth module that are considered for selection with highlighting feature of each module being bold faced. Each module over performs other in certain areas and those are highlighted and discussed below along with drawbacks and then concluded with final selection.

The dimension comparison discussion is included in this section, the Type 1BX has the minimum module dimension compared to all other modules. The next modules that are in line with minimum dimension includes, Type ZY, BGM121 and PAN1316.

Moving on to the operating temperature range comparison, here again Type 1BX over performs besides other modules. The other modules such as Type ZY, Telit 53346-02 and BGM121 has identical operating temperature range that falls in second place in delivering ideal operating range.

Now overviewing the interface options available in various modules, Type 1BX, Type ZY and BM70BLES1FC2-0002AA delivers multiple interface. The rest of the modules including Telit 53346-02, Type VZ, BGM121 and PAN1316 are restricted to UART interfaces only.

The operating voltage range is wide ranged (1.2 – 3.6 V) in Type 1BX compared to all other modules. The next best in this area is BGM121 (1.85 – 3.8 V).

The least priced module includes BGM121 and BM70BLES1FC2-0002AA with former priced around $9.21 and later costs around $9.94.

In the process of comparison so far, the Type 1BX and BGM 121 is satisfactory in all the areas with Type 1BX being even better compared to BGM121. Besides these comparisons, the other factors that results in finalising the module includes Bluetooth version, antenna type, transmission power/ output power. Comparing these factors for Type 1BX and BGM 121 is carried out in the following section.

The Bluetooth version of Type 1BX is version 4.0 with Basic Rate/ Enhanced Data Rate and Low Energy enabled. While, the BGM 121 features upgraded version compared to Type 1BX module, that is, Version 4.2. There are many advantages when it comes to version 4.2 according to claims made by Bluetooth Special Interest Group (SIG) such as, best power optimisation, advanced privacy feature leads to elimination of eavesdropping and even direct internet access enabled (Haartsen et al., 1998).

The Type 1BX module has external antenna, while the BGM 121 has integrated type antenna along with high performance enabled. So, for Type 1BX module, the additional process of investigating compatible antenna and interconnection process needs to be accomplished which is not the case with BGM 121 module.

The transmission power/ Output power is maximum in Type 1BX and it delivers 13 dBm. Contrary to this, BGM 121 delivers 8 dBm transmission power.

Ultimately, with all the comparison done so far, BGM 121 is considered for the Bluetooth module in the design as pricing of Type 1BX is unavailable.

7.3 4G LTE modules

The LTE (Long Term Evolution) network is disassembled, as the frequency band for it to be operational differs from one carrier to the other also, from country to country. The former networks such as 2G/3G/CDMA all together employs only five bands of frequency. But, LTE network alone operates on 44 frequency bands. Moreover, the LTE comes in two types and hence it employs two different technologies such as Time-Division Duplex (TDD) and Frequency-Division Duplex (FDD). Consequently, the complexity piles up and it also indicates that, the global compatible module is unavailable at this moment (Gupta, 2013)

Due to this limitation, the selection of the 4G LTE module for the MEGAphone design is focussed on maximum region compatibility along with Australian region as one of the criteria for selection of 4G LTE module. The other criteria considered for the selection of 4G LTE module includes, minimum module dimension, operating temperature, interfacing options such as UART, I2C, ADC and PCM input/ output audio, minimum power consumption and operating voltage.

To cater the global network, the smartphone manufacturers release the single product in multiple variant so that, it solves the problem of supporting specific carrier and country cellular module and even the antenna range (Gupta, 2013). In the following section, discussion regarding the candidate 4G LTE modules are carried out.

Altair ALT1160

Altair's ALT1160 sports similar chipset found in ALT1210 that is CAT-M1 ioT. This module has higher downlink speed of up to 10 Mbps and uplink speed of up to 5 Mbps. This module also has extremely low power consumption. This chipset incorporates ALT1160 baseband chip along with RF-CMOS transceiver IC, the ALT6401. The ALT1160 has sophisticated design as it assembles advanced power management unit (PMU), DDR memory, low-power CPU subsystem. Furthermore, this chipset incorporates secured framework for customer developed applications (Altair, 2017).

The combination of ALT6401 RF-CMOS transceiver facilitates the evolution of low cost devices with minimum external component count. The bands that are supported by this module are LTE-FDD (450 MHz), TDD (699-960 MHz) and HFDD - Half Duplex FDD (1500-2700 MHz). This module enables the following interfaces such as USB2.0, UART, SPI, I2S/PCM, Auxiliary PWM and ADC, Camera, USIM. This module assembles VoLTE, IMS, OTA-DM

with HD voice functionality. The special feature of this chipset is noise cancellation through its proprietary Interference Cancellation (INCA™) (Altair, 2017).

TELIT LE910 Series

Telit is one of the leading manufacturer of LTE module at present. The LE910 series is one of the best variant till date. The LE910 is basically described as next generation of Telit LTE modules. The main reason behind such claims is, the integration of two high-speed cellular modules in one. The key feature of this module is, it enables simple integration with peripherals and actuators via USB 2.0 HS, UART and GPIOs defined by the user. Data rate provided by this module under LTE network is, uplink of up to 50 Mbps and downlink of up to 100 Mbps (Telit, 2014).

It incorporates 10 I/O ports including multifunctional I/O's. The structural design of this module is such that, the dimensions are 28.2 x 28.2 x 2.2 mm and its operatable temperature ranges from -40°C to +85°C. This module is certified by REACH and RoHS compliant. The REACH is a European Union which manages Registration, Evaluation and Restriction of Chemicals (SA and TRUSTEE, 1999). The supply voltage required for this module is 3.8 VDC under Nominal and the range is from 3.3 – 4.2 VDC. The TELIT LE910 Series has five different variants to be cater various market specification such as North America, Europe, Korea and Australia thereby covering multiple band configurations including sets of 4G and 3G bands. The Australian and European LTE network compatible LTE module in LE910 series is LE910-EUG. The frequency band range of LE910-EUG for LTE compatibility is 800 (B20) / 1800 (B3) / 2600 (B7). The module supports 1.8V/ 3V SIM card interface (Telit, 2014).

In the pursuit of investigation for the compatible 4G LTE modem for the MEGAphone design, certain advanced modems that are very new in the market were noticed and are discussed below,

Intel XMM 7480

This modem is basically Intel's fourth generation LTE modem and delivers cellular ecosystem with a homogeneous solution for next wave of LTE-Advanced services and devices. This modem incorporates many exciting features such as high-speed LTE-Advanced and this basically enables the user to experience high-quality voice calls, video streaming, virtual reality, multi-player gaming and many more. The transceiver employed in this module is Intel SMARTi™ 6T and this enables the support to the maximum number of bands in a single SKU. Consequently, mobile devices can be built with global coverage option. This is the first modem

to support 4 carrier aggregation (4CA) and this feature helps the Original Equipment Manufacturers (OEMs) and operators to alleviate the spectrum fragmentation challenge present in the global market (Intel, 2017b).

The modem is ideally designed for the worldwide compatibility and thus it supports more than 33 LTE bands with all being Industry-leading band density. To cover global market, 5-mode operation is incorporated that includes LTE-FDD, LTE-TDD, TD-SCDMA, legacy 2G and 3G. While coming to the speed provided by this modem, it delivers speeds up to 600 Mbps while downloading and 150 Mbps while uploading. The other unique feature of this modem is power consumption where in it consumes 15% less power compared to Intel's previous generation LTE Advanced modem. Ultimately, to deliver the better spectrum efficiency and higher data rate, 256QAM downlink and 64QAM uplink modulation schemes are included (Intel, 2017b).

Intel XMM 7560

This modem is basically Intel's fifth generation LTE modem. There are many highlighting features as modem delivers very high speed, low latency and revolutionary in radio thereby introduces the user to the gigabits speed in a single, global SKU (Stock Keeping Unit). The output from this modem is incredible as it provides high-speed LTE-advanced connectivity for quality voice calls and intensive data applications. Unveiling about the speeds of this modem, the blazing downlink speed results in delivering speed exceeding 1 Gbps and uplink speed is around 225 Mbps. The band density supported by this module is very wide and it leads by synchronising more than 35 LTE bands (Intel, 2017a).

This module is designed on Intel's 14 nm process and its power consumption is minimal compared to Intel's previous generation LTE Advanced modem. With intention to cater global market operation, module assembles 6-mode operation and this includes LTE-FDD, LTE-TDD, TD-SCDMA, GSM/EDGE, UMTS/WCDMA and CDMA/EVDO. The transceiver employed in this module is Intel SMARTi™ 7. Finally, it supports more than 35 LTE bands simultaneously of either 3.5 GHz or 5 GHz (Intel, 2017a).

As mentioned earlier, these modems are new in the market. Consequently, the data sheets are not made available to public and this lead to the non-availability of detailed information regarding data interfaces that these modules support as this is, the basic criteria to incorporate into the candidate design. Ultimately, the above two modems are potentially interested and may be incorporated in the future design.

Quectel EC25 Mini PCIe

The selection criteria we had for 4G LTE module were discussed with a local cellular vendor here in Adelaide, as they came to support this project and all this was possible through my supervisor on 18th July 2017. We had a meeting in the laboratory with one of the field application engineer from AVNET, an Electronic marketing company based in Mawson lakes here in Adelaide. Along with field application engineer, we had other marketing representative on call. We had a detailed interaction regarding 4G LTE module specification required for the MEGAphone design. Consequently, the Quectel, a leading GSM/GPRS module manufacturer based in Shanghai, had the precise configuration that matched the design criteria. The module that was finalised for the purchase based on the identical features are discussed in detail.

The EC25 is basically, LTE-FDD/LTE-TDD/WCDMA/GSM wireless connectivity module manufactured by Quectel with series of module to cater the specific requirements involved in the various design. This module series assembles receive diversity and thereby enables the various data connectivity on network such as, LTE-FDD, LTE-TDD, DC-HSPA+, HSPA+, HSDPA, HSUPA, WCDMA, EDGE and GPRS (Quectel, 2017).

In EC25 series, EC25AU is available in three variants but, EC25AUFATEA-512-STD is the ideal module as it meets the module selection criteria of Australian region compatibility for 4G LTE modem in this design. The various criterion for 4G LTE module selection in the design is overviewed with respect to this module as below.

As discussed earlier in the introduction to 4G LTE modules, the UART interface is one of the key requirement when it comes to the interface option in this design. Pertaining to the UART interface of this module, it offers two UART interfaces namely, the main UART interface and the debug UART interface.

As per the information obtained through Quectel data sheet for EC25 Mini PCIe, the main UART interface endorses various baud rates such as 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600 and 3000000 bps. The default baud rate for this interface is, 115200bps (Quectel, 2017).

Another feature of this interface is its support for data transmission and AT (Attention) command communication. The AT (Attention) command communication eases the communication. Consequently, the main UART interface is enabled for this design.

The other type of UART interface in this module, that is, the debug UART interface aids a baud rate of 115200 bps. This interface is targeted for Linux console and log output. Coming to the supply voltage requirement, the module requires voltage in the range of 3.3 V – 4.3 V with typical voltage being 3.8 V (Quectel, 2017).

The below image included is of Quectel EC25-AU module:

Figure 43: The EC25AUFA-512-STD (4G LTE) module by Quectel

Some of the other features to consider Quectel EC25 Mini PCIe module as one of the candidate for the MEGAphone design includes physical characteristics with dimension measuring around 32±0.15 x 29.0±0.15 x 2.4±0.2 mm and weighing around 4.9 gram approximately, operating temperature ranging from -35°C to 75°C. Furthermore, the Quectel EC25 Mini PCIe module has EU RoHS compliance. Also, the module supports 1.8 V/ 3 V USIM/SIM card interface (Quectel, 2017).

Ultimately, the Quectel EC25 Mini PCIe modules uplink and downlink speed are tabulated as below:

Technology	Uplink Speed	Downlink Speed
Frequency Division Duplex	50 Mbps	150 Mbps
Time Division Duplex	35 Mbps	130 Mbps

Table 19: Uplink and downlink speed of Quectel EC25 Mini PCIe module (Quectel, 2017).

Finalising a 4G LTE module from the candidate list for the MEGAphone design

Each candidate 4G LTE module discussed so far has its own limitations and advantages and this section summarises those aspects. Consequently, this approach would lead to derive a suitable 4G LTE module for the MEGAphone design.

As mentioned earlier, the Intel XMM 7480 and Intel XMM 7560 datasheet are not available yet. But, it may be considered for future enhancement in the 4G LTE functional block of the MEGAphone design. So, excluding these two modules, the other three modules such as Altair ALT1160, TELIT LE910 series and Quectel EC25 Mini PCIe module are considered for the comparison.

Initiating the discussion by considering operating voltage requirement for all the three modules, Altair ALT1160 has no reference regarding the voltage requirement in the product brochure. So, it is better not to consider for further comparison. Now comparing the TELIT LE910 series and Quectel EC25 Mini PCIe module on various category through table constructed as below:

Parameters	TELIT LE910 module	Quectel EC25 Mini PCIe
Supply voltage range	3.3V – 4.2 V	3.3V - 4.3 V
Typical voltage	3.8 V	3.8 V
Interface	USB 2.0 HS (High – Speed), UART, user definable GPIOs	**PCM, USB2.0, two UART modes, SGMII (Serial Gigabit Media Independent Interface), USIM interface.**
Dimension (mm)	**28.2 x 28.2 x 2.2**	29.0±0.15 x 2.4±0.2
SIM interface	1.8V/ 3V SIM card	**1.8V/ 3V USIM/ SIM card**
Price	$426.48	**$56.09**
RoHS compliance	Yes	EU RoHS directive

Table 20: TELIT910 series and Quectel EC25 Mini PCIe module comparison

Analysing the above comparison table, the TELIT LE910 series module supply voltage requirement is in the range of 3.3 V – 4.2 V with nominal voltage being 3.8V. On the other hand, Quectel EC25 Mini PCIe module requires 3.3 V – 4.3 V with typical voltage being 3.8V. So, both TELIT LE910 series and Quectel EC25 module have identical supply voltage requirement.

Moving on to the interface availability comparison, the TELIT LE910 series module delivers USB 2.0 HS (High – Speed), UART and user definable GPIOs (General Purpose Input/ Outputs). While, the Quectel EC25 module has ample interface options such as, PCM, USB2.0, two UART modes, SGMII (Serial Gigabit Media Independent Interface), USIM interface. Consequently, in this category, the Quectel EC25 Mini PCIe module over performs the TELIT LE910 series module.

The module dimension comparison is discussed in this step, the TELIT LE910 series module measures around 28.2 x 28.2 x 2.2 mm and Quectel EC25 Mini PCIe module measures around 32±0.15 x 29.0±0.15 x 2.4±0.2 mm. The TELIT LE910 series module has better dimension comparatively.

Both the module supports 1.8 V/ 3 V SIM card interface. But the, Quectel EC25 Mini PCIe module even provides USIM card interface.

The price of the TELIT LE910 series module is very expensive compared to Quectel EC25 Mini PCIe module. So, there is no point in considering the module that has huge price difference as the end the product (MEGAphone) price will be way more expensive if, TELIT LE910 series module is considered.

Apart from this above comparison table data, the uplink speed in both the modules are identical (50 Mbps) for both the modules. But the downlink speed is better in Quectel EC25 Mini PCIe module as it provides 150 Mbps compared to TELIT LE910 series speed of, 100 Mbps. But there is no clear information regarding technology (TDD or FDD) that is rendering this speed with respect to TELIT LE910 series 4G LTE module. In contrast to this, the Quectel EC25 module has clear mentioning regarding this.

Ultimately, with all the above various comparison, the Quectel EC25 Mini PCIe 4G LTE module is considered for the MEGAphone design.

8. SCREENS

The screen, is one of the prime component in any smartphone design, as it is the main source for user interaction with the device. The detailed discussion regarding various types of screen available in the market have been discussed earlier under Chapter 3.1.4. The process of incorporating an ideal touchscreen for the MEGAphone is discussed in this section.

8.1 Fairphone2 Screen

Initially, the Plan A was to design and perform rudimentary functional testing thereby, replacing main board for the Fairphone 2 handset, that uses an FPGA, small external memory and cellular radio on a PCB that can take the place of the existing main PCB in the FairPhone2. This plan has been dropped out on the grounds of various reason that has been discussed earlier in Chapter 3.2.3.

But, to retain the core idea, Plan B was laid out to derive the MEGAphone that involves the entire design to begin from scratch and attempt to reverse engineer the Fairphone2 screen to assemble with MEGAphone design by the analysing its pin configuration by performing the continuity test using the Multi-meter. Through the official website of the Fairphone, the screen was available and in the meantime alternatives to get Fairphone 2 screen were investigated such as, looking for a broken screen availability. Fortunately, my supervisor arranged me to get few of the Fairphone 2 broken screens and the continuity test was carried out to determine the interconnection. All the data recorded during the testing process are included in Appendix A.

Again, after the tedious process of testing the Fairphone 2 screen pin configuration, few IC's (Integrated Chip) embedded in the screen panel were unable to figure out as, nowhere the information were available even with IC number. Ultimately, due to all these setbacks, even the integration of Fairphone2 screen was dropped out from the MEGAphone design.

Alternatively, normal smartphone LCD screen with a reasonable size and resolution is considered for the MEGAphone design. Again, it is evident that, there are ample amount of option for screens. So, in the means of selecting the appropriate one, following set of criteria are drawn that benefits the MEGAphone design.

Firstly, the design requires an LCD capacitive touch screen with the resolution being 800x480. The interface type target for this design is to have a 24 bit RGB interface. The main reason for having a 24 bit RGB interface is the reference design availability for the screen interface of

MEGA65 computer and it is having VGA interface for video display. Consequently, it is easier to employ RGB interface type, as it is identical to VGA.

Ultimately, the above criteria for screen selection has been satisfied by a screen manufacturer named Fanscoo Electronic Technology Co.Ltd. The product number and features are discussed below.

8.2 X050DTLN-55 LCD Display

The X050DTLN-55 is 5.0-inch silicon TFT-LCD module manufactured by Fanscoo Electronic Technology Co, Ltd. The specifications of this module are overviewed as follows.

The module outline is 120.7(H)*76.3(V)*3.25(T) mm. The required criteria for interface type is satisfied as this module is RGB interface enabled. The module provides all viewing direction as it is designed under O-FILM technology. The power supply requirement for this module is around 3.3V. The 16 Chip-White LEDs is employed for backlighting the screen. The dot number and dot size for this module are 800*3(RGB)*480 and 0.135(H)*0.135(V) mm.

The display colour provided by this module is 262K. The operating temperature of this module is a highlighting feature with wide range enabled, that is, from -20 to 70°C. The interface is enabled through FPC 0.5mm_Pitch 40 pin. The distance of separation between the consecutive pins is 0.5mm and it is described as Pitch. This touch panel incorporates 40 interface pins to establish the connection (Fanscoo Electronic Techology Co., n.d.).

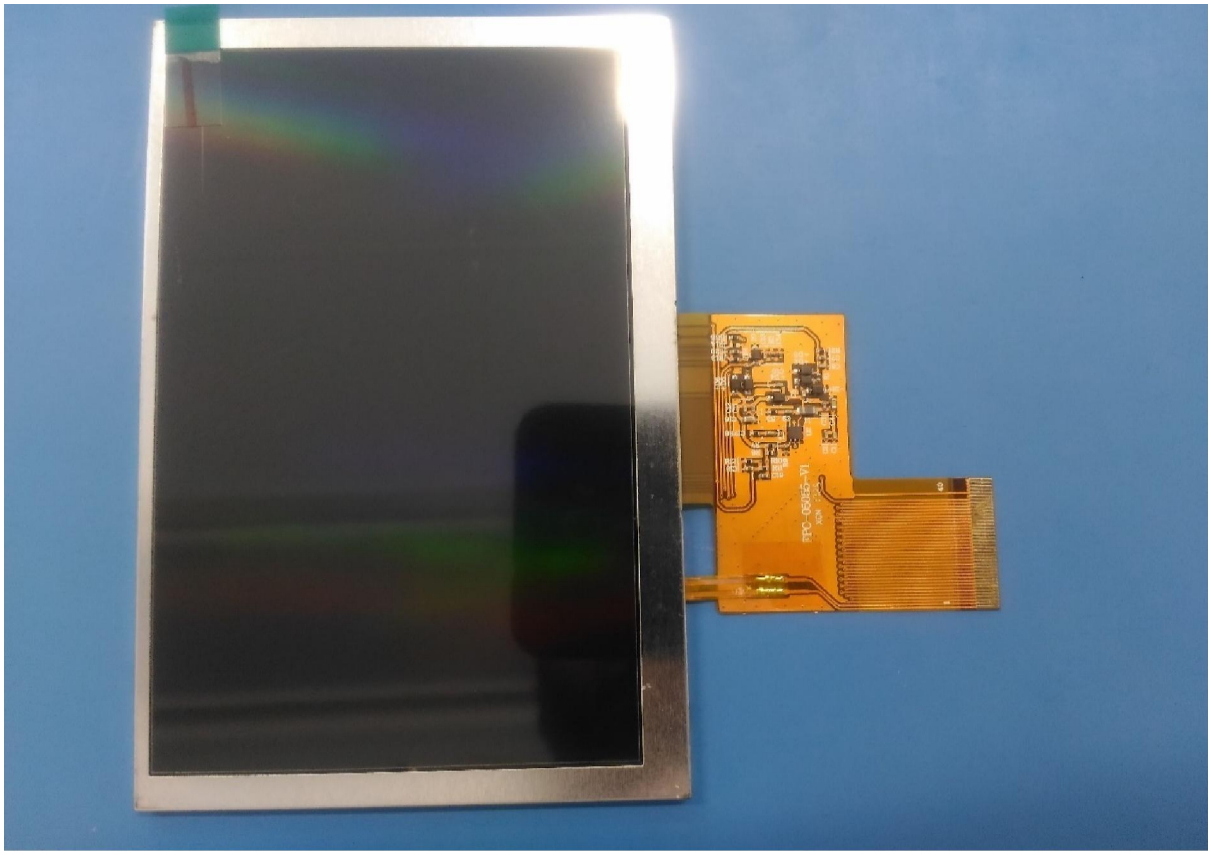

Figure 44: X050DTLN-55 Touch panel

Figure 45: Comparing the dimension of LCD panel with LiFePO4 battery

The corresponding digitiser for the above LCD touch panel can be observed in the below image:

Figure 46: The FT6336U touch digitiser.

Figure 47: FT6336U Touch digitiser dimension comparison with selected single cell 3.2V LiFePO4 battery.

9. DETAIL DISCUSSION REGARDING THE LIST OF PORTS AND MODULES INCLUDED IN DERIVING A FUNCTIONAL MEGAPHONE

9.1 Single-cell LiFePO4 battery

The proposed MEGAphone design is expected to be powered by a Single-cell LiFePO4 battery. The LiFePO4 battery, the Lithium Iron Phosphate also termed as “LFP” (Lithium Ferro Phosphate) belongs to rechargeable battery category. This is basically, a cathode material infused in the lithium-ion battery (Stream, 2016). The LiFePO4 cell is observed as revolutionary in the battery world with some of its unique features such as long-term durability, affordability and the minimal charging time requirement has enabled it to be included in most of the design implementation.

A single cell LiFePO4 battery is capable of delivering 3.3 V supply output with nominal voltage being 3.2 V and peak voltage being 3.65 V (Stream, 2016). For the functional design to be operatable, 3.3 V constant power supply is required, but nominal voltage being 3.2 V, it is necessary to employ a 3.3 V battery regulator to obtain the regulated power supply. The compatible battery regulator selection discussion is added in the later section.

Quick overview on some of the unique features of LiFePO4 batteries are described in this section. The LiFePO4 batteries has comparatively greater tolerance with voltage ranging from 0.7V to 3.5 V. Also, the overcharging is hazardous free up to 4.2 V and anything beyond this voltage level results in break-down of organic electrolytes. The nominal voltage of 3.2 V is provided even during discharging and thus making LiFePO4 cell a non-aqueous system. As mentioned regarding the long-term durability earlier, the LiFePO4 cell provides additional cycle life of up to 2000 cycles when compared to other chemical composition Lithium ion batteries (Stream, 2016).

To avoid the damaging, the battery voltage should not be allowed to discharge below 2.0 V. By being cautious about this voltage level, it is possible to extend the battery life (Hua and Syue, 2010).

The single cell LiFePO4 battery to be included in this functional design is captured in the below screen grab:

Figure 48: Single cell LiFePO4 cell

Figure 49: Comparing battery dimension with smartphone (Fairphone 2) as reference

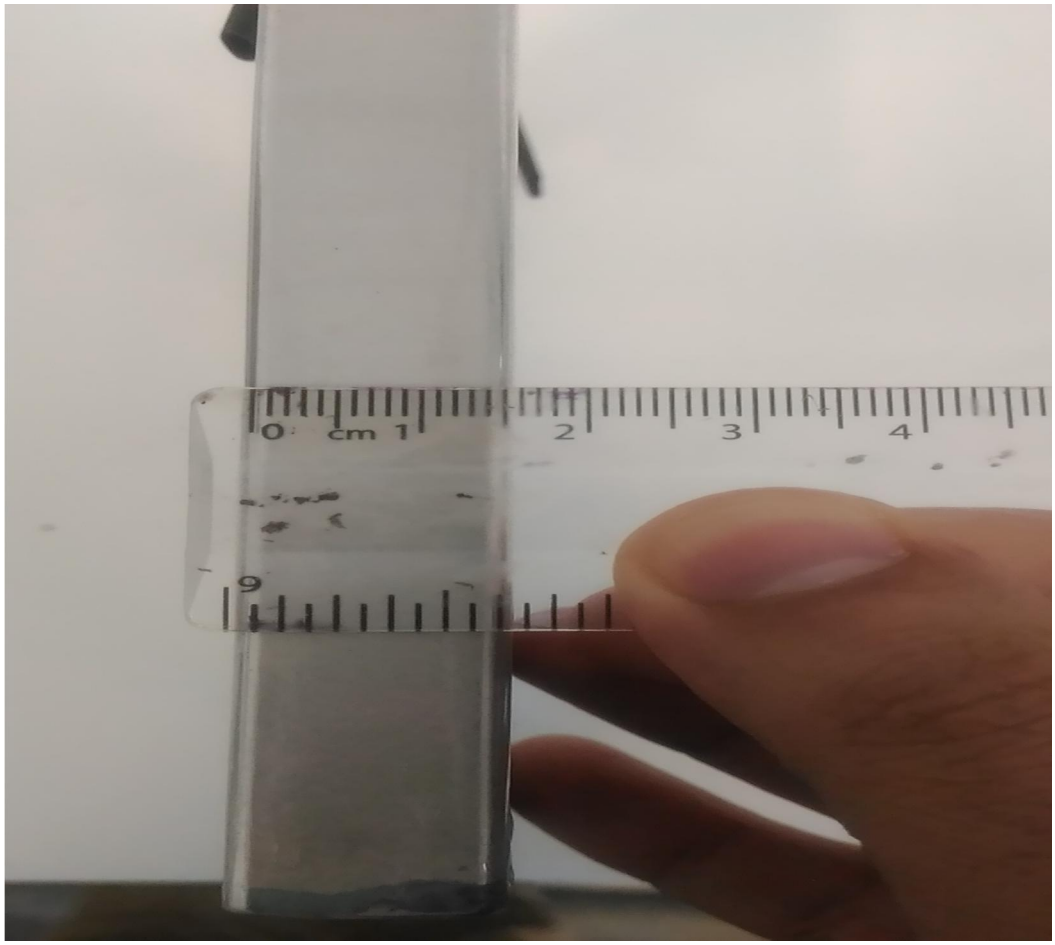

Figure 50: Depth of the LK-1690135 (LiFePO4) battery

From Figure 48, the battery model, voltage and current information are noticeable. The battery model number is, LK-1690135 and nominal voltage is 3.2 V. The current rating of this battery is, 12 Ah (ampere-hour). The battery weighs 200 grams (approximately) with dimension measuring around 130 millimetre/ 13 Centimetre.

The Figure 49 depicts the dimension comparison of battery with a 5-inch screen smartphone (Fairphone 2). The vertical dimension (height) of the battery is almost identical to the smartphone dimension. While, the horizontal dimension (width) is slightly greater than smartphone dimension. With increased horizontal dimension of the battery, the final functional design may fall in to the Phablet size (5.5-inch) category.

Ultimately, the depth of the LiFePO4 battery is measured and is observable from Figure 50. The depth of the battery measures around 1.4 cm and most of the online listing mentions the depth as 16 mm which is basically incorrect.

9.2 Micro-USB connector and charger

Currently, most of the handheld devices battery are charged either by employing Micro-USB connector or the USB type-c connector. The USB type-c connector has been recently introduced and is slowly gaining the market. But, the most popular and ubiquitous charging connector is the Micro-USB.

The Micro-USB connectors were introduced by USB-IF in the year 2007 on 4th of January. There are two types of Micro-USB connectors namely, Micro-A connector and Micro-B connector (Wang and Stavrou, 2010).

Figure 51: Micro-USB A plug (Wikipedia, n.d.-b).

Figure 52: Micro-USB B plug (Wikipedia, n.d.-b).

The Micro-USB B is the most widely used connector in the handheld device charging. The proposed design involves the inclusion of Micro-USB B charge connector to charge single cell LiFePO4 battery.

The suitable charger that would serve the purpose is, LT3652HV manufactured by Linear Technology. The LT3652HV is basically a monolithic step-down battery charger with operating input voltage ranging from 4.95 V to 34 V. This charger has some exciting features

like capability of delivering programmable charge rate of up to 2 A. The charge termination feature terminates charging when charge current drops below 1/10 compared to programmed maximum that is C/10. Once the charging is terminated, the minimum current, typically 85 micro-ampere standby mode is activated. Additionally, when the battery voltage drops 2.5% down the programmed float voltage, the auto-recharge feature is activated with the initiation of new charging cycle (Linear Technology, 2010).

Furthermore, the LT3652HV equips a programmable safety timer and is responsible for activating charge termination after required time is clocked. Ultimately, this charger incorporates 3.3 V float voltage feedback reference and this enables to configure battery float voltage of up to 18 V via resistor divider. This charger is ideal for portable handheld devices (Linear Technology, 2010).

9.3 Controlled output from Single-cell LiFePO4 battery

To obtain a 3.3 V regulated power supply from single cell LiFePO4 battery. The compatible battery regulator was investigated and finally that suited the requirement was, TPS6128xA.

The TPS6128xA is basically a low and wide-voltage battery front-end DC to DC converter suitable for single cell LiFePO4 battery. This regulator ideally serves portable handheld devices assembled with single cell battery by optimising its voltage range.

The battery durability extension as well as current and voltage limitation of powered system can be sorted out by employing TPS6128xA as it has the capability to function as high-power pre-regulator. The TPS6128xA delivers a simple input/output logic interface thereby eases the interfacing process. In the extreme scenario, the TPS6128xA ensures the safety for the battery by activating thermal shutdown, also protects from overload hazards (Texas Instruments, 2016).

The TPS6128xA has some unique features such as, it delivers DC to DC boost or bypass threshold of 3.15 V with $V_{SEL} = \text{Low}$. Likewise, with $V_{SEL} = \text{High}$, the DC to DC boost or bypass threshold delivered is 3.35 V. One of the unique feature of TPS6128xA is its ability to deliver valley inductor current of 3 A which is required for the functioning of the 4G LTE module employed in this design and is discussed in the further section. The nominal body size of TPS6128xA measures around 1.66 mm x 1.66 mm with 16 pins in total (Texas Instruments, 2016). The part number of this module selected for the MEGAphone design is TPS61281A as it has simple logic control interface.

9.4 Disabling the power supply to 4G LTE module

The 4G LTE module equipped in this design is Quectel EC25 Mini PCIe. The detail discussion about this module features and functioning has been discussed under 4G LTE module selection section.

Generally, the 4G LTE module consume lot of power. Consequently, the battery drains rapidly. Furthermore, the other components in the design is affected for its smooth functioning. It should be noted that, the ample amount of power consumption is due to the Radio Frequency exchange by the 4G LTE module and this remains as sole reason.

To overcome this issue, the continuous 3.3 V power supply for Quectel EC25 Mini PCIe module is disabled during unnecessary situation. This process of disabling power supply is possible by pulling down (to low-level) W-DISABLE# pin present in the Quectel EC25 Mini PCIe module which will be pulled up by default. Ultimately, the Quectel EC25 Mini PCIe module enters Airplane mode. During this state, Radio Frequency functioning is halted. Moreover, access to the all AT commands correlative with Radio Frequency function is prohibited (Quectel, 2017).

9.5 Disabling the power supply to FPGA and dependent components via GPIO line of FPGA

The FPGA module employed in this design is, TE0725-03 TRM FPGA. The detail discussion regarding this module has been carried out in the FPGA selection section. This FPGA board runs on 3.3 V input power supply. As it is not required to keep FPGA active all the time, it is better to cut the supply when there is no necessity of running it.

Generally, FPGA have plenty of pins and to interpret easily, the FPGA pins can be divided into two categories. The two categories are namely, Dedicated Pins and User Pins. The dedicated pins are assigned to carry out specific function and are prevented from configuring by the user. This is generally termed as, hard-coded. While, the user pins also called as, IOs or I/O’s or user IOs are basically input/output pins. These input/output pins are user configure enabled. The user will have total control over these pins and can be configured either as input, output or even as bi-directional (fpga4fun, n.d).

In context to the above, the TE0725-03 TRM FPGA has 6 I/O’s called as I/O banks and they are tabulated as below:

Bank	VCCIO	B2B I/O	Notes
0	3.3 V	0	JTAG
14	3.3 V	0(3)	3 I/O in XMOD-JTAG- for use as UART
15	1.8 V	0	Used for optional hyper RAM
16	2.5 V	0	Used for optional fibre transceiver
34	User select	42	0R resistor to select 3.3 V
35	User select	42	0R resistor to select 3.3 V

Table 21: I/O Banks (Trenz Electronic, 2017c).

So, disabling the 3.3 V power supply to the FPGA board and dependent component is possible by sending signal via I/O, Bank 34 or Bank 35 of the FPGA board.

9.6 Enabling the 3.3 V power supply to FPGA and dependent components by employing momentary switch

In the previous step, the FPGA and the dependent components has been disabled from the power supply. Again, during the situation when the FPGA and the dependent component needs to be functional, the power supply is enabled by employing a momentary action switch. The dependent components with respect to FPGA are discussed in the later section. The momentary action switch is held for 2 seconds and this gives the power supply back.

The momentary switch that can be employed in this design is, single pole single throw type (SPST) as there is only a single source of power supply included for the MEGAphone functioning.

9.7 Enabling the 3.3 V power supply to FPGA and dependent components by an interrupt signal from 4G module

As discussed in the previous step for re-activating the power supply to FPGA and the dependent components via momentary switch. In this step, the other means of re-activating FPGA is discussed, that is via sending an interrupt signal from Quectel EC25 Mini PCIe module to TE0725-03 TRM FPGA and the dependent component.

This process is implementable by interfacing one of the General-purpose Input/ Output (GPIO) pin of the Quectel EC25 Mini PCIe module to TE0725-03 TRM FPGA. Basically, there are three GPIO's in Quectel EC25 Mini PCIe module and the one that is required in this process is WAKEUP_IN, that is pin number 1 (Quectel, 2017). The WAKEUP_IN is a digital input type

and sliding it to the low level sends the wake-up signal to TE0725-03 TRM FPGA. Consequently, the FPGA and dependent components will be reactivated.

9.8 Enabling the 3.3 V power supply to FPGA and dependent components by an alarm signal from a Real-Time Clock

One more way of re-activation of 3.3 V power supply to TE0725-03 TRM FPGA and the dependent components is possible by the integration of Real-Time Clock (RTC) module.

The TE0725-03 TRM FPGA needs to be interfaced with an RTC module via I2C connection. So, an RTC module with I2C enabled interfacing option needs to be investigated. Furthermore, the RTC module should be able to produce an interrupt signal. In other words, an alarming signal, needs to be generated from the RTC module. Once the alarming signal is generated, the 3.3 V power supply to FPGA and dependent components are enabled via alarming signal.

The ideal RTC module to implement this procedure is, PCF8563 RTC module manufactured by NXP semiconductors. The module is available in five variants, module with type number PCF8563TS/5 is the suitable for this functional design. The PCF8563TS/5 module is identified by the name TSSOP8. The reason behind choosing this variant specifically are, it's minimal dimension and leads availability. The PCF8563TS/5 measures a body width of 3mm and provides 8 leads. (Texas Instruments, 2016).

The pin configuration is as tabulated below:

Symbol	Pin	Description
OSCI	1	Oscillator input
OSCO	2	Oscillator output
$\overline{INT}$	3	Interrupt output (open-drain; active LOW)
V_{SS}	4	Ground
SDA	5	Serial data input and output
SCL	6	Serial clock input
CLKOUT	7	Clock output, open-drain
V_{DD}	8	Supply voltage

Table 22: Pin configuration of PCF8563 (Texas Instruments, 2016).

The PCF8563 is equipped with a sixteen 8-bit registers and features address auto-increment feature for registers. The module has an on-chip oscillator with a frequency of 32.768 kHz and along with this, a capacitor is added. The source clock and calendar feature for this RTC module

is provided by a frequency divider unit. The module also incorporates a timer, a programmable clock output, a voltage low detector and finally an, I2C-bus interface of 400 kHz.

Overviewing the register design of this module, the assembled 16 registers are addressable 8-bit parallel registers with some of the bits left unimplemented. The initial two registers with memory location 00h and 01h basically meant for controlling and are called as control and/or status register. The consecutive memory location from 02h until 08h are employed as counter which facilitates clock functioning. The clock functioning includes from seconds to year. The alarm registers are allocated with the memory location starting from 09h through 0Ch and this indicates the alarm state (Texas Instruments, 2016).

The control and/or status register with address location 01h, is the register that needs to be observed for the activation of the interrupt signal which leads to enabling of 3.3 V power supply to FPGA and dependent components. The PCF8563 datasheet, provides the information about 8-bit allocation of the control and/or status register with memory location 01h can be observed. This table serves as foundation to analyse the interrupt signal activation.

Activating the interrupt mode is discussed in this section. As mentioned earlier, the PCF8563TS/5 has 16, 8-bit register. Out of 16 registers, 4 registers are allocated for alarm and are assigned with the memory location 09h. The 4 Alarm registers are as follows,

- Register Minute_alarm
- Register Hour_alarm
- Register Day_alarm
- Register Weekday_alarm

The above four alarm registers bit allocation serves as the base for the explanation carried out in the below section (Texas Instruments, 2016).

Initially, the alarm enable bit (AE_x) with bit number 7 of more than one register of the recently overviewed alarm register needs to be cleared. Consequently, the alarm condition activates. During alarming, the Alarm Flag (AF) is set to logic high. To generate the interrupt, the asserted AF can be employed. Interface helps in clearing the AF.

In this section, the interrupt generation via alarm function is explained precisely. The bit that is controlling this process is, Alarm Interrupt Enable (AIE) bit. During the situation when AIE is enabled, $\overline{\text{INT}}$ pin varies according to the condition of AF bit. The AF bit will be in the set condition until it is interfaced. Once the AF bit is interfaced, it reaches the clear state and

remains in this state until time increments in order to match the alarm condition which leads in transition to set state again (Texas Instruments, 2016).

PCF8563TS/5 RTC module is available on Mouser electronics through its website au.mouser.com with single module priced around $1.52. The PCF8563TS/5 RTC module is RoHS compliant.

9.9 Disabling the 3.3 V supply to the Wi-Fi module via a signal from the FPGA board.

Provided, the Airplane Mode physical switch is not set to prevent powering the Wi-Fi module, the FPGA must be able to control the supply of power to the Wi-Fi module, and if the Wi-Fi module requires it, instruct the Wi-Fi module to power up or power down. Basically, this functional block of the MEGAphone will work in such a way that, it should be capable of, disabling the Wi-Fi interface when it is necessary. This is necessary to ensure that, it cannot exfiltrate information or make the device traceable, when the user desires to be offline and untraceable. Therefore, just as for the 4G LTE module, it is necessary to have a mechanism to disable the Wi-Fi module by disabling its power. So, with respect to the component selected for the MEGAphone, the TE0725-03 TRM FPGA needs to control the power supply line of the Type 1GC-Imp005 Wi-Fi module to implement this functional block.

9.10 3.3 V supply to the 4G module controlled via signal from the FPGA, but only if physical switch is set to allow 4G module to be powered

In a situation where the Airplane mode in Quectel EC Mini PCIe is not activated via W-DISABLE# pin (Pin 4) to prevent powering to the module. Then, TE0725-03 TRM FPGA must be able to control the supply of power to the Quectel EC25 Mini PCIe module, and if the Quectel EC25 Mini PCIe module requires it, instruct the Quectel EC25 Mini PCIe module to power up or power down. The Quectel EC25 Mini PCIe module has a PWRKEY pin (Pin 21) that generates signal required to control 4G module to power up after it has been supplied with power.

The Quectel EC25 Mini PCIe module data sheet indicates that power should not be removed from the EC25 before the PWRKEY signal or the appropriate AT command has been issued to shut down the module internally. This requirement can be met by having the FPGA program issuing the AT command before depriving the module of power (Quectel, 2017).

9.11 3.3 V supply to both the Wi-Fi module and the 4G module can be disabled via a physical switch labelled “Airplane mode”

Ideally this would be the same switch as airplane mode, in the form of a 3-position switch, where the centre position is only Wi-Fi is powered, and one end disables both, and the other end enables both. That is, one end is full wireless connectivity, and the other end is no wireless connectivity.

The switch should ideally be de-bounced in some way, so that power is cut to the appropriate module is disabled only after 1 second, so momentary discontinuity, e.g., due to a dirty switch, does not cause the modules to rapidly power cycle.

The Quectel EC25 Mini PCIe module data sheet indicates that power should not be summarily removed without using the PWRKEY input line or issuing the appropriate AT command. Therefore, it is desirable to have the airplane mode switch circuitry sustain provision of power to the 4G module for a short period of time, also pull the PWRKEY low for > 650ms during that time (Quectel, 2017).

The total time required for safe shutdown in the manner is very long (>29.5 seconds), which is unacceptably long. The module also features a RESET line (Quectel, 2017). By pulling the RESET line low, it will presumably cause the EC25 to cease writing to flash memory, and it should be safe to remove power after a short period of time, presumably less than a second, allowing only enough time for any pending flash memory write to complete.

Therefore, the airplane mode circuit requires edge detection for the 4G-disable function, which should then feed a timer circuit that pulls RESET line low for at least 150ms + time to complete flash memory writing (perhaps approximately 400ms total), and sustains power the 4G module for a flexible period, before disabling power to the 4G module. Experimentation will be required to confirm that this is adequate, but it seems a reasonable starting point, since 29.5 second shutdown time is unacceptably long.

If a MOSFET circuit is used to gate power to the 4G module, this edge detection and short sustain function could be implemented by coupling the enable signal to the MOSFET with a pull-up capacitor and pull-down resistor, so that the MOSFET remains ON for a short period after the gate signal ceases to drive. The 4G power LED should remain on until power is deprived, from the 4G module.

9.12 Real-time clock IC to maintain time and date when switched off, and to set alarms

In the Chapter 9.8, discussion with regards to the enabling of 3.3 V power supply to FPGA and dependent components by an alarm signal through RTC (Real-Time Clock) has been added. Also, the suitable RTC that needs to be incorporated for the respective functional design has been overviewed, that is PCF8563TS/5 RTC module. Now, again considering the same RTC module, time and date needs to be maintained during switch-off scenario. Even, the alarm setting scenario needs to be added.

During a situation when power source of MEGAphone, that is, single cell LiFePO4 cell is not charged and cell charge is getting drained up with functional design being operational. To avoid the damaging of LiFePO4 cell, it is necessary to avoid over-discharging.

It has to be noted that, single cell LiFePO4 cell voltage is around 3.3 V and in order to avoid damaging by over-discharge, the cell should not be allowed to discharge below 2.0 V (Cycle9, 2011). In the means of ensuring this, operation of the entire functional design is not possible when charge drops below a typical operational voltage of 3.3 V. At this point of time, only key modules in the functional design that fetches minimum amount of power remains operational. One such module that should remain operational is the real-time clock.

The PCF8563TS/5 real-time clock module is required to restore the date, time and alarm setting with the rest of modules of functional design are deprived from power supply. For PCF8563TS/5 fetches very low back-up current, typical 0.25μA at $V_{DD} = 3.0$ V (NXP, 2015).

This minimal current can be drawn from single-cell LiFePO4 cell until it reaches 2.0V and discharge rate is quite satisfactory in LiFePO4 cell and thus it can run the PCF8563TS/5 for long period. Ultimately, it is possible to implement this functional step.

Additionally, it was noticed that, PCF8563TS/5 is capable of delivering signal output of 32.768 kHz, 1.024 kHz, 32 Hz and 1 Hz (NXP, 2015). This signal output can be made available for TE0725-03 TRM FPGA so that, the FPGA can run in the low power mode whenever necessary and this helps in optimising the power consumption of the FPGA module.

9.13 Power Indication LED for 4G LTE module

The 4G LTE module to be employed in the design is Quectel EC25 Mini PCIe. To indicate the power status of the 4G LTE module, the LED needs to be assembled along with 4G LTE module. Analysis of the data sheet of Quectel EC25 Mini PCIe for pin configuration of the

module to assemble LED was carried out. Consequently, it was noticed that, module has pins dedicated for power ON and OFF operation of the module. The PWRKEY (power key) pin is assigned with pin number 21. The DC characteristics of this pin are as follows, $V_{IH}max = 2.1$ V, $V_{IH}min = 1.3$ V, $V_{IL}max = 0.5$ V (Quectel, 2017).

The $V_{IH}max$ indicates, Maximum Input High Level Voltage Value, $V_{IH}min$ indicates Minimum Input High Level Voltage Value and $V_{IL}max$ indicate Maximum Input Low Level Voltage Value.

Initially, the Quectel EC25 Mini PCIe module is set to power down mode. The process of turn on can be implemented by manipulating the PWRKEY, through button. In order to avoid the electrostatic strike that may occur during button press via finger, essential Transition Voltage Suppression (TVS) diode needs to be employed near the button to avoid Electro Static Discharge (ESD) (Quectel, 2017).

A basic LED circuit can be interconnected to PWRKEY pin and thus serves the required purpose. The RGB LED from Yetda Industry Ltd available through SparkFun with model number 5060000BRG4 is considered for LED (Yetda Industry Ltd, n.d.). The feature should be enabled in such a way that, during the time when power is supplied to the EC25 module, the green LED should turn ON. To turn ON, green LED, suitable value of current limiting resistor needs to be investigated.

9.14 Power indication LED for FPGA board

The power domains are different for individual functional units in this design. The TE0725-03 TRM FPGA does not have the LED to indicate the power status of the module. So, it is necessary to have an external LED circuit basically consisting of current limiting resistor and Light Emitting Diode (LED) between supply terminal, V_{cc} and ground (GND) terminal. As mentioned earlier, the nominal voltage supply that a single LiFePO4 cell can deliver is, 3.2 V and thus 3.3 V regulated power supply is obtained by employing TPS6128xA (battery regulator) as it is necessary for powering up the TE0725-03 TRM FPGA.

Both the 50-pin header included with TE0725-03 TRM FPGA, Optical transceiver has the supply terminal V_{cc} and ground(GND), with pin number 5 being V_{cc} (3.3 V supply) and pin 1 being assigned as ground(GND). So, it would be ideal to include basic LED circuit between these two pins to monitor power status of the module. Consequently, the LED turns ON/OFF in proportional to the power supply to the TE0725-03 TRM FPGA. The basic LED circuit is

driven by supply voltage with current limiting resistor in series with an LED. The series connection of current limiting resistor stabilises current through LED.

Surface mount technology (SMT) LED is considered for the design. The RGB LED from Yetda Industry Ltd available through SparkFun with model number 5060000BRG4 is considered (Yetda Industry Ltd, n.d.). The feature should be enabled in such a way that, during the time when power is supplied to the TE0725-03 TRM FPGA, the green LED should turn ON. To turn ON, green light of the LED, suitable value of current limiting resistor needs to be investigated.

The calculation of suitable current limiting resistor requires the following data of the LED, such as forward voltage and forward current along with supply voltage provided (a1ronzo, 2010). The forward voltage varies for different colours in an RGB LED, but the forward current is identical. In perspective to 5060000BRG4 RGB LED, the forward voltage for green light is 3.1 V, the forward current being 30mA (Yetda Industry Ltd, n.d.) and the supply voltage provided for the TE0725-03 TRM FPGA is, 3.3 V. Now determining the required current limiting resistor (a1ronzo, 2010) with all the above data as follows,

$$R = \frac{V_s - V_f}{i}$$

$$= \frac{3.3 - 3.1}{30 * 10^{-3}} = 6.66\ \Omega$$

Since, the obtained current limiting resistor of 6.66 Ω is not a standard value, rounding up to a standard value is desirable. Consequently, the value of 6.8 Ω would be an ideal consideration for the design to stabilise the current through 5060000BRG4 RGB LED module during the event of green LED turn ON/OFF operation to indicate the power status of TE0725-03 TRM FPGA.

9.15 Power indication LED for Wi-Fi module

The power status indication of the Wi-Fi module needs to be implemented via LED. The Wi-Fi module considered for the MEGAphone design is Murata's Type 1GC-Imp005. There are two ways to implement this step.

The first way of implementation is considering Type 1GC-Imp005 module's LED drive to enable the functioning of red/green status LEDs. The module provides a dedicated pin for red

and green LEDs with former assigned with pin named, B35 and later assigned with pin named, B36. Both the LEDs are configured as output (Murata, 2016).

The LED's are usually available in two configurations, either common anode or common cathode. The Type 1GC-Imp005 has the ability, to auto-detect LED configuration and this feature can be enabled by observing the direction of idling at boot with respect to red LED pin (B35). The proper functioning of this process requires a 10 kiloohm resistor in parallel with red LED. The common anode and common cathode circuit implementation can be referred in (Murata, 2016).

To notify the power status of the Type 1GC-Imp005 Wi-Fi module, the green LED drive pin (B36) needs to be programmed for two scenarios. In the scenario 1, the green LED should turn ON to indicate the module being powered. On the other hand, during the scenario 2, the green LED should turn OFF as soon as the Wi-Fi module is deprived of power. The power sequence for Type 1GC-Imp005 Wi-Fi module is tabulated as below,

Power supply Status	Green LED status
Power supplied	ON
Power deprived	OFF

Table 23: Power status indication for Wi-Fi module by configuring LED drive.

So far, the LED sequence for power status indication of the Type 1GC-Imp005 Wi-Fi module has been discussed. When it comes to the employment of the suitable LED for the operation, the company recommends certain bi-colour LED and information about this can be referred in datasheet (Murata, 2016) . The current limiting resistor needs to be calculated once the specific bi-colour LED is chosen from the recommended list.

The second way to indicate the power status of the Wi-Fi module is possible by reconsidering the basic LED drive circuit mentioned in the earlier section of power indication LED for FPGA module and this is arguably a very simplified version thus making it easy for the interpretation. This method involves including the suitable green LED along with the current limiting resistor to Type 1GC-Imp005 Wi-Fi module between the main power supply terminal and the ground. The Type 1GC-Imp005 Wi-Fi module requires a 3.3V regulated supply and to ensure this, 3.3V battery regulator TPS6128xA has been employed and discussed in the previous section. There are various power supply terminals available in Type 1GC-Imp005 Wi-Fi module. The Type 1GC-Imp005 Wi-Fi module main power input terminal is A43 (VDD) and ground terminal considered here is A40 (GND) (Murata, n.d.-b).

Particularly surface mount technology (SMT) oriented green LED module is considered to implement this step and the Avago Technologies, ASMT-UGB5-NV702 matches the required specification. Considering the forward voltage, forward current of ASMT-UGB5-NV702 LED module which is 3.2 V and 20 mA(milli-ampere) (Avago Technologies, 2011), calculation of current limiting resistor (a1ronzo, 2010) is as follows,

$$R = \frac{V_s - V_f}{i}$$

$$= \frac{3.3 - 3.2}{20 * 10^{-3}} = 5\ \Omega$$

The obtained current limiting resistor of 5 ohm is basically a non-standard value. Considering a standard value for the design is ideal and in that case, the obtained value is rounded up to 5.6 Ohm. Ultimately, 5.6 Ohm current limiting resistor is required to stabilise the current through the ASMT-UGB5-NV702 LED in a basic LED drive circuit and this completes the second method of implementation, for power indication of Wi-Fi module through an LED.

9.16 Four RGB LEDs

The RGB LEDs are included in the MEGAphone design to facilitate LED blinking to notify incoming messages, missed call, low/full battery indication, charging status and so on. This is identical to the normal smartphone feature. Most of the smartphones blinks red LED for low battery indication, green LED for incoming messages, missed calls and even full charge indication. While, the orange LED for charging status indication (indicating charger being plugged). Ample amount of RGB LEDs and breakout boards are available currently in the market. In the process of delivering the optimised design, it would be ideal to consider SMD (Surface Mount Device) LEDs rather than breakout boards.

The SparkFun has ample number of SMD LEDs to consider, Triple Output LED RGB – SMD module available on the product website of SparkFun is employable (SparkFun, n.d.). Before delving deep into this SMD LED module, a quick overview on RGB LED design is necessary.

RGB LEDs basically consists of three LEDs (Red-Green-Blue) that are assembled into one. Apart from these three colours, it is possible to obtain different colours by fusing these three colours in various combination. Normally, the RGB LEDs consists of four pins, with three colours accommodating three individual pins accounting to three pins in total. While the remaining one pin is basically common pin and this would be either Anode or Cathode (Schubert et al., 2005).

Coming back again to RGB LED module selected, the Triple Output LED RGB – SMD module's common pin is configured as Anode. The typical forward voltage required to drive the various colour in this LED module are tabulated below:

LED colour	Typical Forward Voltage
Red	2 V
Green	3.5 V
Blue	3.5 V

Table 24: Typical forward voltage required for driving LEDs (SparkFun, n.d.).

Since it is proposed to assemble four RGB LEDs, and this would fetch total of 16 pins. As it is required to interface with TE0725-03 TRM FPGA, during the integrated design, external slots usage needs to be optimised to include all the functional blocks of the MEGAphone, at that point of time, allocating 16 pins is quite difficult. As a result, suitable I2C (Inter Integrated Circuit) IO (Input/ output) expander needs to be employed. There are many other functional blocks that require I2C IO expander. So, it would be ideal to discuss regarding this by collectively considering all the functional blocks.

9.17 VGA connector providing video output with at least 4-bits colour depth per channel

According to the data obtained from the Nexys4 DDR board reference manual, it requires 14 FPGA signals for VGA port implementation and delivers 4-bits colour depth per channel. Out of 14 FPGA signals, 12 signal lines with 4 bits each are dedicated for Red, Green and Blue colour respectively. Ultimately, remaining 2 signals are assigned for standard sync signals such as Horizontal Sync (HS) and Vertical Sync (VS) (Digilent, 2016).

Having this Nexys4 DDR board VGA port as reference, it is essential to derive the identical model using TE0725-03 FPGA to provide video output with 4-bits colour depth per channel. Furthermore, along with the VGA connector it is also required to drive LCD panel (X050DTLN-55) with 4-bits colour depth per channel and in doing so, the suitable buffer needs to be investigated. The main aim behind the buffer employment is to enable the driving of both, VGA connector and LCD panel (X050DTLN-55) from same physical lines of TE0725-03 TRM FPGA.

The logical buffer amplifiers are enabled to drive the multiple displays simultaneously and thus serves the purpose of driving displays through same physical lines of FPGA.

The Octal buffer is employed in the MEGAphone design and this has eight individual buffer amplifiers. This is capable of delivering 4-bits colour depth per channel. Again, these Octal buffers are available in TTL (Transistor-Transistor Logic) and CMOS (Complementary Metal Oxide Semiconductor) Logic. The entire functional design is powered up by a single LiFePO4 cell and it is necessary to optimise the power consumption of the octal buffer.

In general, TTL chips draws lot of power in the idle state compared to CMOS buffer and this, ruins the goal of power optimisation. In contrast to TTL buffer, the CMOS chip power drawing is proportional to the clock rate and as the clock rate value increases, the power consumption increases and vice versa. The only area where the CMOS chips lags compared to TTL chip is in manipulating the electrostatic discharge and thus it is more prone to damage (Ashida et al., 1982).

One of the important factor that decides in finalising the appropriate buffer for the functional design is the required minimum supply voltage. The octal buffers that requires this comparison is 74HC244 and 74HCT244 manufactured by Nexperia. The 74HC244 is a CMOS level octal buffer with supply voltage requirement ranging from minimum of 2 V to a maximum of 6 V. While, the 74HCT244 is a TTL level octal buffer with supply voltage requirement ranging from minimum of 4.5V to a maximum of 5.5 V(Nexperia, 2016). The TE0725-03 TRM FPGA employed in this functional design requires single power supply of 3.3V (Trenz Electronic, 2017c). Since the octal buffer is driven by the TE0725-03 TRM FPGA lines, the minimum supply voltage of TE0725-03 TRM FPGA is compatible with 74HC244, CMOS level octal buffer and can be included in the functional design. Consequently, the 74HCT244, TTL level octal buffer is not considered due to greater minimum supply voltage requirement (Nexperia, 2016).

9.18 LCD screen connected via digital VGA interface with at least 6 bits colour depth per channel

In Chapter 8, the LCD screen selection process for the MEGAphone design has been discussed and ultimately, X050DTLN-55 LCD screen was selected. With the selected LCD screen, it is required to implement the functional block which involves interconnecting LCD screen to the TE0725-03 TRM FPGA through VGA interface with a minimum of six bits colour depth per channel. This basically involves dedicating at least 6 bits for RGB colour (Red/Green/Blue) channels. Furthermore, additional 3 lines for HSYNC, VSYNC and PIXELCLOCK and this sums up to requirement of 21 FPGA lines in total.

Before implementing this step, initially the power supply requirement for the LCD screen operation should be considered. The supply voltage required to drive the LCD screen lies in the range of 3 V – 3.6 V, with typical voltage being 3.3V (Fanscoo Electronic Techology Co., n.d.). On the other hand, the TE0725-03 TRM FPGA can deliver 3.3 V output power. Consequently, there is no necessity of bringing down the voltage level for this functional implementation.

However, the number of pins required is 21, there is a possibility to reduce this pin numbers by considering the power supply to X050DTLN-55 LCD screen just above the minimum voltage, that is, around 3.1 V. At this voltage level, the logic level converter with MOSFET (Metal Oxide Field Effect Transistor) circuit needs to be employed between the TE0725-03 TRM FPGA and X050DTLN LCD screen to match the voltage level. As a result, the TE0725-03 FPGA outputs are buffered for producing the Analog VGA signal from same lines on the FPGA, thereby the pin number count can be brought down. The reason behind choosing the MOSFET circuit is that, it can transform voltage level in either way, that is high to low and low to high.

9.19 LCD capacitive touch digitiser via I2C/SPI to FPGA board

The capacitive LCD touch digitiser interfacing to TE0725-03 TRM FPGA board needs to be implemented. Again, the I2C or SPI interfacing standards are considered for implementation. The capacitive touch digitiser employed for this functional block implementation is FT6336.

In the process of exploring the possible interface standards for implementation of this part of the functional design, the Adafruit capacitive touch screen, FT6206 interfaced with Arduino board with I2C communication protocol enabled was noticed. The entire communication establishment of Adafruit capacitive touch screen with Arduino board C++ code is available through GitHub. This implementation provides the foundation for developing the I2C interface for capacitive touch screen employed in this functional design, FT6336U with TE0725-03 TRM FPGA board. With the datasheet of FT6336U touch digitiser and taking the reference of the C++ code mentioned above, it is possible to implement this functional block with the necessary information available.

9.20 Accelerometer connected via I2C to FPGA board

The accelerometer is also one of the functional requirement in deriving the MEGAphone design. Generally, the accelerometer is quite commonly assembled sensor that, aids in detecting tilt, motion and orientation of smartphone. Additional feature includes shake detection (Lau

and David, 2010). Once, the tilt or motion is detected, the LCD adjusts the viewing direction accordingly.

A simple and high performance oriented accelerometer is employed in this design and it is delivered by LIS3DH. The LIS3DH is manufactured by ST microelectronics and available through Adafruit website and is basically, one of the most popular triple-axis accelerometer with low power consumption feature in the "Nano" family category. Some of the exciting features of the LIS3DH accelerometer are listed as follows,

- Supply voltage range is from 1.71 V to 3.6 V
- Minimum power consumption in Ultra low-power mode with just 2 μA.
- Provides I2C or SPI digital output interface
- Capable of detecting motion and free-fall
- Integrated temperature sensor
- Free-fall and motion detection via 2 independent programmable interrupt generators
- The output data rates from 1 Hz to 5 kHz is measurable as it provides dynamically user selectable full scale of, $\pm 2g/\pm 4g/\pm 8g/\pm 16$ g.
- Capable of detecting 6D/4D orientation
- The operating temperature ranges from -40°C to +85°C
- The module is RoHS compliant

The LIS3DH accelerometer has 16 pins in total. The pin description can be referred in datasheet (ST, 2016).

The functional description of this module is overviewed in this section. Basically, LIS3DH delivers two operating modes namely, normal mode and low power mode. Both the modes are unique with former one delivers high resolution, while the latter one minimizes the current consumption compared to former one. The selection of the operating mode can be referred in in LIS3DH accelerometer datasheet. To interpret this, the control register description is necessary and this can be referred in LIS3DH accelerometer datasheet. Referring these two table gives the precise information regarding LPen (Low power mode enable) bit of control register 1 and HR (High resolution output mode) bit of control register 4 (ST, 2016).

So far, the features, pin configuration and functional description has been overviewed. Now it is essential to discuss the connection of LIS3DH accelerometer to TE0725-03 TRM FPGA. This proposed interconnection is carried out via I2C interface, as both accelerometer and FPGA provides I2C compatibility.

As per the data obtained from the datasheet of LIS3DH, the pin number 8 that is CS, has the capability of enabling either SPI or I2C interface and thus, provides either one mode for selection depending on the requirement (ST, 2016).
Since, the target interface is I2C, the I2C mode needs to be enabled. During the activation of I2C interface mode in LIS3DH, the CS line must be set to high. In general, the CS pin needs to be connected to pin number 1, that is, Vdd_IO.
Basically, the registers present in the LIS3DH can be accessed via I2C serial interface. The other pins that are essential for I2C serial interface establishment are as follows:

Pin number	Pin name	Pin description
4	SCL	I2C serial clock
6	SDA	I2C serial data
7	SA0	I2C less significant bit of device address
8	CS	I2C mode selection (1: I2C mode)

Table 25: Pin description of I2C interface (ST, 2016).

Basically, the accelerometer LIS3DH is a slave bus and the I2C interface is responsible for writing the data into the register and enables the content to be read back. The various terminology pertaining to I2C interface can be referred in LIS3DH accelerometer datasheet (ST, 2016).

Overviewing the signal involved in I2C bus and this includes Serial Clock Line (SCL) and Serial Data Line (SDL). The SDL is responsible for both sending and receiving the data to/from the interface and hence it is termed as bidirectional line. The external pull up resistor needs to be employed to interconnect these data lines to Vdd_IO pin. The scenario of both lines being high occurs only when bus is free. The I2C interface manages to work in both fast mode and the normal mode (ST, 2016).

9.21 Four SIM card sockets connected to 4G module via SIM MUX ICs

The idea behind the employment of multiple SIM slot is to switch between the various network operators. Also, this quad SIM slot eliminates the need of swapping the SIM cards during the period of multiple countries travel. According to my observation with respect to the telecommunication laboratory engineers within the university, they travel to a minimum of 3

to 4 countries on regular basis is not particularly uncommon. Furthermore, given the large size of the device, there is plenty of room to accommodate the quad SIM feature.

In this functional design, four SIM card slots are incorporated. It should be noted that, direct interconnection of SIM card slots to the 4G module is not possible and hence, SIM MUX ICs are employed to connect the four SIM card slots. The SIM MUX ICs that needs to be employed in this functional design is TXS02324.

The TXS02324 SIM MUX ICs is manufactured by Texas instruments and has dual-supply standby capability. The TXS02324 enables the interfacing between a wireless baseband processor and two individual SIM subscriber cards thereby allowing to save the data for mobile handset applications. This custom designed TXS02324 is capable of interfacing two SIMs/UICCs (Subscriber Identification Module/Universal Integrated Circuit Card).

Some of the key features of TXS02324 are overviewed in this section. This module is compatible with ISO/IEC Smart-Card Interface, GSM and as well as with 3G mobile standards. Two supply voltage pins are provided by voltage-level translator. The baseband interface is enabled by VDDIO and sets the reference voltage for operation from 1.7 V to 3.3 V. The two SIM card slot VSIM1 and VSIM2 are enabled for functioning in either 1.8 V or 2.95 V. This voltage for SIM cards are delivered by an internally assembled independent Low-Dropout (LDO) regulator. The input battery voltage in the range of 2.3 V to 5.5 V is accepted by LDO (Texas Instruments, 2011).

The TXS02324 is basically a 20 pin QFN (Quad Flat No-leads) package. The module delivers a wide operating temperature ranging from as low as -40°C to as high as 85°C. The module dimension is around 3 mm x 3 mm.

The precise information regarding SIM card interfacing can be interpreted by referring the diagram depicted in figure 1 of TXS02324 datasheet (Texas Instruments, 2011).

The TXS02324 pin configuration details can be referred in Terminal function table of TXS02324 datasheet. The basic overview on the TXS02324 operation can be overviewed in the section, basic device operation of TXSO2324 datasheet. Furthermore, the procedure involved in establishing SIM interface and SIM cards transition can be interpreted by referring section, Setting-up the SIM interface and switching between SIM cards described in TXS02324 datasheet (Texas Instruments, 2011).

A single TXS02324 is capable of multiplexing two SIM card slots as per the information obtained from TXS02324 datasheet (Texas Instruments, 2011). As mentioned earlier, the functional design involves cascading of four SIM card slots and hence possibility of multiplexing all these four SIM card slots through a single TXS02324 MUX IC requires experimentation.

For the normal operation of the TXS02324 SIM MUX IC even in the situation where the TE0725-03, Artix-7 100T optical transceiver FPGA is not powered, the TXS02324 SIM MUX IC is powered through the 3.3 V supply provided to power up Quectel EC25 Mini PCIe module.

So far, the discussion regarding the features of SIM MUX IC TXS02324 and powering up the module has been completed. The SIM card slot multiplexing possibilities were explored. Now, the suitable SIM card slot that should be featured in this functional design needs to be investigated and in doing so, Molex 0473080001 is the ideal SIM card slot for this functional design. The SIM card slot with product number 473080001 is manufactured by Molex with various ratings and configuration that would be essential looking through are as below (Molex, n.d.-a):

- Voltage: $\mathrm{Vcc} = 5\ \mathrm{V} \pm 10\%,\ \mathrm{ripple} \leq 100\mathrm{mVpp}$
- Current: $10mA\ max$
- Operating temperature: -40°C to 85°C
- Durability: 5000 cycles.

9.22 PWM or similar adjustable backlight controller for the LCD panel

Normally, to backlit the LCD panel in any battery powered device including mobile phone, white LED's are employed. There are various advantages in selecting LED to drive the LCD panel such as it can deliver maximum luminous efficiency, durability and additionally, the minimal size. Generally, the LED's employed for back lighting LCD panel are approximately 0.1 W (Watt) powered (Lam, 2008).

A quick overview on white LED evolution, the Japanese manufacturer Nichia developed white LED during the year 1996. Back then, the white LED was designed by "coating GaN (gallium nitride) and InGaN (indium gallium nitride) blue LED with a yellowish phosphor compound". (Lam, 2008). There has been a lot of developments in white LED to improve its luminous efficacy. Normally, in order to drive a LCD panel, between 6 to 10 LED's are necessary (Texas Instruments, 2017a).

Generally, LED's electrical characteristics is mainly dependent on forward voltage (VF) and this varies between 2.7 – 4 V and forward current in the range of, 20 mA – 1.5 A (Lam, 2008). To drive these LED's, the suitable LED driver are necessary. These LED drivers are responsible for adjusting white LED intensity which is responsible for LCD panel brightness variation.

From the MEGAphone design perspective, the LCD panel, X050DTLN-55 is backlit enabled through a set of 16 white LED's. The forward voltage (VF) for this set LED's is in the range of 21.6 V – 24 V with forward current being 40 mA. The LED circuit diagram can be referred from X050DTLN-55 LCD screen datasheet (Fanscoo Electronic Techology Co., n.d., Texas Instruments, 2017a). Certain LCD panel are enabled with automatic back light adjustment that functions based on the ambient light (environment light), but the X050DTLN-55 LCD panel does not include such feature. The other way of back light adjustment according ambient situation is, ambient light sensor. The ambient light sensor inclusion for the MEGAphone design is discussed in later section.

Even though, both the LED driver and ambient light sensor sole purpose is to control the LCD panel brightness through the variation of white LED intensity according to the situation and thereby optimises the battery consumption. It is necessary to have both the feature in the MEGAphone design as it operates differently, with the LCD panel brightness adjustment via LED driver is not dependent on the ambient light instead, it is dependent on user touch. While, the ambient light sensor works in correspondence to ambient light level.

Narrowing the discussion to the LED driver suitable for the X050DTLN-55 LCD panel employed in the MEGAphone design. The PWM (Pulse Width Modulation) method of controlling the brightness of the LCD panel needs to be incorporated. As mentioned earlier, the X050DTLN-55 LCD panel is driven by 16 White LEDs (WLEDs) and the compatible LED driver for this is Texas instruments, LM36272 IC (Integrated Chip).

The LM36272 is basically a dual channel LCD backlight driver designed to drive LCD panel with a maximum of 16 LEDs. The chip is, PWM brightness control enabled and even I2C brightness control feature is included. The operating supply voltage is in the range of 2.7 V – 5.5 V and it is possible to provide the required supply voltage while driving from TE072-03 TRM FPGA as it delivers 3.3 V supply.

As mentioned earlier, the maximum forward voltage required for X050DTLN-55 LCD panel 16 LEDs is, 24 V with a forward current of 40mA and the LM36272 can deliver 28 V for a

string of 8 LEDs with maximum current of up to 30 mA. The detailed description of LM36272 chip can be referred in datasheet (Texas Instruments, 2017a).

The LM36272 delivers two brightness control modes namely, I2C only brightness control and I2C along with PWM brightness control. For the MEGAphone design, second mode would be ideal and the details regarding can be referred in LM36272 datasheet(Texas Instruments, 2017a) .The two strings can accommodate a total of 16 LEDs.

9.23 Micro SD card slot to be connected to FPGA board

The ideal Micro SD card connector for the functional design selected is manufactured by Molex with series number 47219.This Micro SD connector is based on hinge style. The durability of this Micro SD card slot is up to a maximum of 5000 mating cycles. The operating temperature range is from -40°C to +85°C. The termination interface style of this Micro SD card slot is surface mount (Molex, n.d.-b). The unit price of this Micro SD card connector is $1.11 and is available through Digi-Key Electronics.

The selected Micro SD card slot is interconnected to TE0725-03 TRM FPGA via SPI interface. The SPI interface can be established by overviewing the Micro SD card pins. Generally, a Micro SD card has a total of 8 pins. In order to enable the power connection to Micro SD card, pin 4 and 6 are required, with pin 4 being 3.3 V supply and pin 6 being ground (GND) (Davis, 2016). It can be noted that the functional design is powered by 3.3V supply.

The Micro SD card pinout for SPI mode enabling is depicted in the table below:

Pin number	Pin name	Signal function
1	NC	No Connect
2	/CS	Chip Select
3	DI	Master Out/Slave In(MOSI)
4	Vdd	Supply Voltage 2.7V to 3.6V
5	CLK	Clock
6	Vss	Ground
7	DO	Master In/Slave Out(MISO)
8	RSV	Reserved

Table 26: Micro SD pin configuration (Davis, 2016).

9.24 Speaker, ideally stereo, for audio output

Every smartphone is equipped with a speaker that delivers the required audio output. The audio output serves the purpose of notification which includes, the ringing for incoming calls, alarm functioning, task reminders, conversation via speaker and so on. Furthermore, one of the most ideal and popular purpose that speaker delivers is, music output. Smartphone speakers have seen lot of updates, with even capable of delivering Dolby digital audio output. Consequently, the smartphone manufacturers are showcasing audio output delivery as one of the highlighting feature to consider during the process of selecting ideal smartphone.

Shifting the focus towards the speaker that needs to be employed in the MEGAphone design and the purpose it serves, ideally between 1 to 4 Centimetre diameter, stereo speaker needs to be integrated to deliver notification sounds for incoming calls, messages, alarm functioning and call conversation.

The speaker that would be ideal for this functional design to consider according to target specification is, K 16 – 8 Ohm from the manufacturer, Visaton. This speaker module measures around 1.6centimetre and targets the application involving model construction. The technical specification of this module can be referred from datasheet (Visaton, 2015).

The impedance of this speaker is 8 Ohm and the rated power is 0.5 W (Visaton, 2015). So, driving the speaker via TE0725-03 TRM FPGA requires a suitable amplifier as the power output from FPGA is 3.3 V.

9.25 Microphone

The Microphone feature in any smartphone is one of, the most essential functional unit as it enables the voice communication. Normally, single microphone is assembled to deliver this feature.

From the perspective of inclusion of microphone feature to the MEGAphone design, the Nexys4 DDR board has on board microphone feature, considering this design as reference and thereby by analysing the entirety of the design, the MEGAphone's microphone functionality is derived.

Now analysing the Nexys4 DDR board microphone functional unit, the ADMP421 chip is employed for this feature inclusion, which is basically an Analog device, omnidirectional MEMS (Micro-electromechanical Systems) microphone (Digilent, 2016).

The ADMP421 chip comes in a small and thin, surface-mount package with dimension measuring, 3 mm x 4 mm x 1 mm. The chip has higher signal to noise ratio and sensitivity of 61 dBA (A-Weighted Decibel) and -26 dBFS (Decibels relative to full scale). Further details regarding the entire feature of this chip can be referred in ADMP421 datasheet (Analog Devices, 2011).

In the MEGAphone design, the microphone module needs to be interconnected with TE0725-03 TRM FPGA and even requires suitable amplifier that is necessary for microphone. Since, the microphone unit design of Nexys4 DDR board is open source, it would be convenient to design microphone functional block for MEGAphone by incorporating ADMP421 chip.

In doing so, the voltage supply requirement for the ADMP421 chip was investigated through its datasheet and the chip requires voltage ranging from a minimum of 1.8V to maximum of 3.3 V (Analog Devices, 2011). The TE0725 TRM FPGA is capable of driving ADMP421 chip as it delivers, 3.3 V supply. Regarding the amplifier inclusion, the ADMP421 has an inbuilt impedance converter amplifier (Analog Devices, 2011) and thereby eliminates the need for additional amplifier for the microphone functional block implementation for MEGAphone.

The ADMP421 microphone chip delivers PDM (Pulse Density Modulated) format as means for digitised audio output. The PDM format is widely employed in portable audio applications. The main advantage of the PDM format is that, it enables two channels transmission in mere two wires (Analog Devices, 2011).

9.26 Headphone jack

The MEGAphone design includes an audio jack that delivers both stereo audio output and mono microphone input. The specific requirement mentioned can be found in TRRS (Tip/Ring/Ring/Sleeve) style audio jack. Before, discussing the 3.5mm TRRS audio jack to be employed in this functional design, a quick overview on various style and standards of 3.5 mm audio jack are described in the following section.

The various style available in the headphone jack are TS, TRS and TRRS. The TS (Tip/ Sleeve) style basically has two conductors and is available in 3.5 mm. This style is suitable for establishing mono unbalanced connections with respect to microphone level and speaker level. The next style that is TRS (Tip/ Ring/ Sleeve) is based on three conductors and is available in 3.5 mm. This style ideally suits the application involving mono balanced connections. But, it

is widely assembled to support unbalanced stereo application in both microphone and speaker level (Tépper, 2015).

Now focussing on the style that needs to be employed in the MEGAphone design, that is TRRS (Tip/ Ring/ Ring/ Sleeve). The TRRS style is ubiquitous and can be noticed in all handheld device as well as personal computers and Laptops that are enabled with 3.5 mm audio and microphone function. As mentioned earlier regarding the standards, only TRRS style has two standards OMTP and CTIA/ AHJ. The confusion between these two standards are quite common and precise differentiation between these two are described below (Tépper, 2015).

It is noticeable that, both the TRRS standard comprises of four conductors. The major difference between the two standard lies in the functional assignment for four conductors. The OMTP standards assigns Tip for left audio, ring 1 as right audio and ring 2 for microphone. While, the sleeve is assigned as ground. Contrary to OMTP, the CTIA/ AHJ assignment for the four conductor varies slightly with Tip and ring 1 assignment retained as identical to OMTP. While, ring 2 and sleeve assignment is the vice versa of OMTP that is, ring 2 is assigned as ground and sleeve is assigned as microphone. The OMTP is basically an older version TRRS and was employed in Sony Ericsson in its Xperia series released during the year 2010 and 2011, Samsung chrome books released during the year 2012 and even, in Sony's play station Vita (Tépper, 2015). Currently all the handheld devices, PC's and Laptop are mostly assembled with CTIA/ AHJ standard TRRS.

AHJ stands for American Headset Jack also called as CTIA. The table comparison of OMTP and CTIA/ AHJ standard is depicted below:

Standards	Tip	Ring 1	Ring 2	Sleeve
OMTP	Left audio	Right audio	Microphone	Ground
CTIA/ AHJ	Left audio	Right audio	Ground	Microphone

Table 27: TRRS standards (Bryan, 2017).

So, far the detailed discussion regarding the various styles and standards of audio jack and even the proposal for the MEGAphone design audio jack has been discussed. Now, narrowing the focus on to the MEGAphone audio jack that is, TRRS audio jack that delivers both stereo audio output and mono microphone input needs to be investigated. During that process, one ideal module that delivers this specification was found and is available through SparkFun website. This 3.5 mm TRRS audio jack is SMD (Surface Mount Device) oriented ideal for integration to handheld device and development boards.

9.27 Audio output to speaker and headphone jack can be independently controlled

Generally, every Smartphone outputs the audio via speaker or headphone. This feature works in such a way that, at once, output is delivered from either one of the source. More precisely, audio output is obtainable through the speaker if, the headphone jack is left unconnected and vice versa. To enable this feature of audio output, switch over in Smartphone, usually a controller IC (Integrated Chip) is employed.

Viewing with respect to the MEGAphone design, it would be ideal to replicate the identical feature as discussed above recently, but with certain modification with assignment of independent audio lines for speaker and headphone jack. Here, the stereo audio output signal generated from the TE0725-03 TRM FPGA needs to be channelled through amplifier and thereby the amplified signal needs to be directed to the speaker and headphone jack. It is possible to implement this functional block either by selecting the suitable controller IC (Integrated Chip) or by replicating audio output lines.

Employing the controller IC would be ideal as these IC's, have inbuilt amplifiers and this eliminates the additional process of selecting the suitable amplifier. Furthermore, replicating audio output lines is not convenient as it would require additional pins from TE0725-03 TRM FPGA. In case if this option is considered there may be a possibility of insufficient pins available from TE0725-03 TRM FPGA for the implementation of remaining functional blocks of the MEGAphone design.

For the design convenience I2C interfaced audio controller IC has been considered for the MEGAphone design. The NCP semiconductors NCP2704 is the ideal IC. Some of the unique features of this IC are its capability of delivering high sound quality in both the speaker and headphone. Furthermore, it provides individual mixer control for speaker and headset. The supply voltage required for this IC is in the range of 2.5 – 5.5 V. So, it is possible to deliver the required supply voltage through TE0725-03 TRM FPGA as it can deliver 3.3 V supply. The entire feature and operating characteristic of the NCP2704 IC can be referred from the datasheet (ON Semiconductor, 2010).

9.28 Microphone input from headphone and internal microphone can be physically disabled via switch

In the MEGAphone design, the internal microphone employed is, the ADMP421 chip and headphone jack employed is, TRRS audio jack that has mono microphone input as discussed in the earlier sections. Since there are two microphone inputs for inputting the audio signal into MEGAphone. It is necessary to include the switch between the internal microphone and audio jack so that, when the headset is plugged into the audio jack, the microphone input is enabled to the audio jack line and internal microphone inputting is disabled by switching process and vice versa.

To implement this functional block, it is necessary to investigate the suitable switch. Since, it is required to have single switch control for both the line, DPDT (Double Pole Double Throw) switch would be ideal and thereby it is possible to physically disconnect circuit to them.

In addition to this function, the LED indication can also be included. Basically, this requires the DC bias current to flow on either one of them or possibly both, which would be sufficient enough to power an LED to indicate the isolation status.

9.29 Wi-Fi module interconnection with the FPGA via UART or SPI interface

The Type 1GC-Imp005, is the Wi-Fi module considered for the MEGAphone design. It is required to establish the communication between Type 1GC-Imp005 and TE0725-03 TRM FPGA via UART or SPI interfacing protocols. As tabulated earlier in the specification list of Type1GC-Imp005, the module is enabled with both UART and SPI interface. The UART interface protocol is considered in this design. The pin dedicated for the UART interface in Type1GC-Imp005 Wi-Fi module is tabulated as below:

Pin	Name	Type	Description
A52	UART0_RXD	Input	uart0 serial input
A53	UART0_RTS	Output	uart0 request to send
A54	UART0_CTS	Input	uart0 clear to send
A55	UART0_TXD	Output	uart0 serial output

Table 28: UART interface pin details (Murata, 2016).

The Type1GC-Imp005 Wi-Fi modules nominal operating voltage is 3.3 V. The pin dedicated for inputting main power supply to the module is, A43 (VDD) and corresponding ground pin

is A40 (GND) (Murata, 2016). On the other hand, the Artix-7 100T, optical transceiver FPGA operates with same voltage as of Type1GC-Imp005 Wi-Fi module. Even though the Artix-7 100T, optical transceiver FPGA has dedicated UART pins, but this is not considered for interfacing for the sake of maintaining design simplicity. Instead, the 50-pin header included with Artix-7 100T, optical transceiver FPGA is considered.

The voltage range required for the normal operation of Type1GC-Imp005 Wi-Fi module when supplied through A43 (VDD or VDD_VBAT) is from a minimum of 3.13 V to a maximum of 4.8 V. The typical voltage is not mentioned in the datasheet and it can be any value that falls between 3.13 V to 4.8 V. Since, the Type1GC-Imp005 Wi-Fi module is driven by Artix-7 100T, optical transceiver FPGA, the voltage available through this module is 3.3 V. So, 3.3 V is considered as typical supply voltage for Type1GC-Imp005 Wi-Fi module for the functional design (Murata, 2016).

9.30 UART, I2C, input and output PCM audio interfaces and ADC interface between 4G module and FPGA

In the means of establishing the communication between 4G LTE module and FPGA, the UART, SPI, I2C and input/ output PCM (Pulse Code Modulation) audio interfacing protocols options are considered. The multiple interfacing options are necessary, as the module is responsible for enabling the entire telephony feature for this functional design.

The 4G LTE module and the FPGA considered for the functional design is, Quectel EC25 Mini PCIe and TE0725-03 TRM FPGA respectively. The detail discussion regarding this functional block are carried out as below.

The Quectel EC25 Mini PCIe module facilitates 2 types of UART interface such as main UART and debug UART. The various baud rates are supported in the main UART interface and in this functional design, default baud rate is considered, that is 115200 bps. While, the debug UART is capable of transmitting data only in 115200 bps baud rate. In selecting between these two types of UART for the functional design, former one is capable of delivering the data transmission and AT command communication, while the latter one is suitable for Linux console and log output (Quectel, 2017). Thus, the functional design mainly involves data exchange, in that context, main UART interface is ideal.

The pin assignment for the main UART interface can be referred from Quectel EC25 Mini PCIe module datasheet. It has to be noted that, the module typical operating voltage

requirement is 3.8 V (Quectel, 2017). But the UART interface power domain is 1.8 V. With respect to the UART interface between Quectel EC25 Mini PCIe module and TE0725-03 TRM FPGA, again this power domain difference comes into picture as Artix-7 100T, optical transceiver FPGA requires single power supply with a nominal voltage of 3.3 V (Trenz Electronic, 2017c). So, in that case voltage should be reduced from 3.3 V to 1.8 V and to do so, there are many options to consider such as, voltage divider network, Low drop-out (LDO) regulator. The Quectel EC25 module datasheet suggests, considering a level translator for this process. The level translator module considered here is, Texas instruments, TXS0108EPWR. The reference circuit for establishing the interconnection with Quectel EC25 Mini PCIe module and a microcontroller can be referred in (Quectel, 2017) and this serves as base for deriving the schematic for UART interface between Quectel EC25 Mini PCIe module and TE0725-03 TRM module that is required for the functional design.

Now moving on to the PCM (Pulse Code Modulation) audio interface, single PCM interface is delivered by Quectel EC25 Mini PCIe module and offers two modes such as, Primary mode and Auxiliary mode. For the functional design, PCM audio input and output are required and the Primary mode serves the requirement as it operates in both master and slave mode and caters short frame synchronisation. While, the Auxiliary mode operates only in Master mode and caters long frame synchronisation. Narrowing the discussion to the primary mode, the data sampling operation is possible through PCM clock signal and performed on the respective falling edge. While, the rising edge of the PCM clock signal is picked up for the transmission. The MSB (Most Significant Bit) is considered with respect to falling edge of PCM data frame synchronisation signal (Quectel, 2017).

The I2C (Inter Integrated Circuit) interface between the Quectel EC25 Mini PCIe and TE0725-03 TRM FPGA can be implemented through the I2C interface dedicated pins provided by Quectel EC25 Mini PCIe module. Both, I2C serial clock and I2C serial data pin of EC25 Quectel module which is responsible for I2C interface operates in 1.8 V power domain. The, Artix-7 100T optical transceiver FPGA operates in 3.3V power domain. Consequently, voltage reduction is required by employing either voltage divider circuit or Low drop-out regulator. Since, both the I2C pins are configured as open drain, pull-up resistor needs to be employed for the operation in 1.8 V power domain. In the I2C interface operation, the Quectel EC25 Mini PCIe module functions as master device only (Quectel, 2017).

The pin configuration for both PCM and I2C interface of Quectel EC25 Mini PCIe module and also, the PCM and I2C interface with an external codec IC can be referred in Quectel EC25 mini PCIe module datasheet (Quectel, 2017). But, in this functional design, the TE0725-03 TRM FPGA itself, is considered as codec.

Finally, one of the means to monitor the LiFePO4 battery voltage employed in this design is possible through employing one of the ADC (Analog to Digital Converter) pins available in Quectel EC25 module. The Quectel EC25 module provides two dedicated pins for ADC operation and the details regarding the pin assignment and voltage characteristic can be referred from Quectel EC25 Mini PCIe module datasheet (Quectel, 2017).

9.31 25-pin DSUB connector for SX-64 keyboard

The Commodore64 computer has keyboard as one of its peripheral device and it is interconnected via a 25-pin DSUB connector. In this functional design, this 25 pin DSUB connector along with the keyboard are interfaced to TE0725-03 TRM FPGA. To accommodate all the functional requirement units, it is necessary to optimise the pin usage of the FPGA by employing suitable Input/ Output (IO) expander. There are plenty of options available for IO expanders and this functional design intends to employ I2C protocol IO expander. The reason behind employing I2C protocol is basically, it enables master device to control communication of one or more slave devices. In relation to this functional design, TE0725-03 TRM FPGA is considered as master device and SX-64 keyboard with DSUB connector is considered as slave device.

While integrating the MEGAphone functional blocks, it is necessary to employ the suitable I2C IO (Input/ Output) expander to accommodate this 25-pin DSUB connector.

The PCA9698 manufactured by NXP semiconductors will be suitable to connect this 25-pin DSUB connector. This is basically a 40 pin IO expander and requires a 5 V supply (NXP, 2010). To ensure the 5 V power supply, it is again required to include 5 V DC-DC Converter. Earlier in the design, a 3.3 V voltage regulator (TPS6128xA) has been included to provide required 3.3 V supply to most of the functional blocks. But this functional block is an exception from that as 5 V supply is required here and this is possible by considering the connection of a 5 V DC-DC converter connected to the 3.3 V regulated output obtained from TPS6128xA (Texas Instruments, 2016).

This requirement can be sorted out by the inclusion of a 5 V DC-DC converter, NCP1402 by ON semiconductor. This breakout board is capable of accepting the input voltage between 1 to 4 V and delivers 5 V output. (ON Semiconductor, 2014). Rather than considering this breakout board, it would be ideal if this included as part of the schematic design. Furthermore, this breakout board is currently retired. The other possible inclusion would be considering, Microchip's step-up DC-DC converter, MCP1640/B/C/D. This IC can deliver, both 3.3 V and 5 V supply output. This IC delivers, 3.3 V output with output current of 100 mA (Microchip, 2015b). But, this output current is too low to drive TE0725-03 TRM FPGA or Quectel EC25 Mini PCIe 4G LTE module. Thus, it is not considerable for the MEGAphone.

9.32 Two x 9-pin C64 Joystick Ports

The joystick port for the MEGAphone is also one of the design requirement with, the unit capable of serving dual purpose such as, a secure communication device as well as a, game console.

Now, moving on towards the revolution of joystick port. The 9-pin joystick port was first introduced in Atari's gaming console, Atari 2600 back in 1977. This revolutionary port introduced back then has been popularly recognised by the term, Atari joystick port. Later, this port was even assembled in the computer as one of the prime port to enable the connection for several gaming controllers (Marchand and Hennig-Thurau, 2013).

Figure 53: Atari 2600 Joystick port (Wikipedia, n.d.-a).

This port was even housed in commodore series (8-bit) computer as gaming port to run the popular games. One of the last version of Commodore series, Commodore-64 launched in the year 1982 incorporated this 9-pin connector for joystick connection.

Figure 54: Control port (9-pin) for joystick connection (C64 Wiki, 2016).

Basically, this 9-pin connector is a D-sub miniature also known as D-sub electrical connector. This term was coined due to its physical appearance as it is basically a D-shaped metal shield (Scott et al., 2013).

In perspective to the functional design requirement, this 2, 9 pin Commodore64 joystick needs to be assembled to the TE0725-03 TRM FPGA via I2C interface. But by doing so, it fetches total of 18 pins which is a huge number. Consequently, this causes the hurdle for the accommodation of other functional components. So, to resolve this issue, a suitable I2C interface compatible IO expander needs to be investigated which thereby saves the FPGA pins.

9.33 Four momentary - action user buttons

Basically, the momentary action buttons are the one which performs the assigned operation such as activation or deactivation only until, the button is pressed. As soon as the user releases the button, the operation is terminated. Normally, the smartphone is equipped with momentary action button to deliver the features such as Powering ON/ OFF and volume control. The two buttons employed mainly performs the two mentioned functions. However, there are other sub functions that are associated with these two buttons and the discussion regarding those, is not necessary with respect to MEGAphone design.

Now with respect to the MEGAphone design, the momentary action switches serve the same purpose as discussed with respect to the smartphone. Even this functional block requires I2C IO expander as this establishes the connection through FPGA and due to this to save TE0725-03 TRM FPGA pins.

9.34 Wireless co-existence interface between Wi-Fi and 4G module

The finalised Wi-Fi (Type 1GC-Imp005) module for this project does not have the provision to implement this functional block of the MEGAphone design.

Basically, this functional block of the MEGAphone design would require a Wi-Fi module that is designed to function simultaneously with the 4G LTE module which is possible through a Wi-Fi and Bluetooth combo as this would be one of the simplest way of implementation. But, by doing so, a new challenge arises as the Wi-fi module also becomes inactive if the cellular radio in the 4G LTE module is powered down. Since hardware testing is out of scope in this project, the future student needs to test the possibility of implementing this step.

From the time when MEGAphone design was initiated, the Wi-fi and Bluetooth combo inclusion in the design was not considered and this is evident as separate selection criteria sets and even the process of selection are carried out independently. But, during this functional block implementation exploration, this came in the way of one of the possible solution.

One possible module suggestion for the future students in considering Wi-Fi and Bluetooth combo is, Quectel FC20N, as it has dedicated pins for the implementation of Coexistence interface (Quectel, 2016).

Another method to implement this functional block of the MEGAphone that can be considered by the future student would be, by inclusion of Wi-Fi module only, that has some input lines which notifies them to terminate the transmission temporarily.

9.35 Ambient light sensor

Ambient light sensor functioning has been described earlier in the section 3.1.10. In this functional design, the ambient sensor light is employed to control the brightness of X050DTLN-55 TFT-LCD module.

Normally, the ambient light sensor module is based on I2C protocol and this functional considers the same. The other factors such as RoHS compliance and surface mount type (SMT) are taken into the account while selecting the ambient sensor module.

Currently, there are plenty of options available for ambient sensor light module in the market and it requires thorough analysis to sort out the best one that suits according to the functional design requirement which was ultimately found in APDS-9200 module from Broadcom.

The APDS-9200 is packed with exciting features which includes even the ultra-violet light sensing along with ambient light sensing. The power optimisation can be achieved through APDS-9200 with the module design being unique which involves matrix arrangement. This feature provides the device with best angular response for sensing of ultra-violet and ambient light. The measurable ultra-violet wavelength by this module ranges from 320nm to 400nm and this range is identified as UV-A. Another wavelength ranges from 290nm to 320nm and

named as UV-B. The module has the capability to detect extremely low light with lux rating being 0.008 (Broadcom, 2017).

The lux rating basically defines the intensity of light that is measurable. This module is enabled with I2C interfacing and it has additional feature such as, it includes interrupt pin and this aids in minimising the tasks that a microcontroller had to perform. With respect to the MEGAphone design, the interrupt pin can be utilised to serve for FPGA's task reduction. The detailed description of the module operation and pin configuration can be referred in APDS-9200 datasheet (Broadcom, 2017).

Again, to save the pins of TE0725-03 TRM FPGA, the I2C IO expander is employed for connecting APDS-9200. For the integrated design, it would be ideal to consider the suitable I2C I/O expander to reduce drawing the pins from TE0725-03 TRM FPGA.

9.36 Proximity sensor for blanking screen during calls

The detailed description regarding the proximity sensor functioning was dealt in the section 3.1.11. Now focussing on proximity sensor to be employed in the MEGAphone design, the digital proximity sensor with I2C interface enabled is considered. The module with this specific configuration has been investigated and discussed below.

The Avago Technologies, APDS-9130 is fused with Infrared LED and a proximity measurement system designed on 8-pin package and has very small dimension of 3.94 x 2.36 x 1.35 mm (L x B x H). This module is capable of, detecting the object from distance of up to, 100 mm. Also, the module features fast two I2C interface of up to 400 kHz and this eases the connection establishment with the Artix-7 100T optical transceiver FPGA employed in the design. The input/output pin configuration for this module can be referred in APDS9130 datasheet (Avago Technologies, 2015).

The communication between APDS-9130 and the Artix-7 100T is established through I2C interface. The recommended voltage for operating APDS9130 proximity sensor ranges from 2.2 – 3.6 V with typical supply voltage being 3V. Here, the Artix-7 100T provides 3.3 V supply and would be convenient to operate APDS9130 proximity sensor at 3.3 V.

Again, as discussed in the ambient light sensor earlier, it is required to incorporate the suitable I2C IO expander to optimise the pin usage of the TE0725-03 TRM FPGA.

9.37 Analogue battery voltage input

Any handheld devices that runs on battery needs to display the battery percentage so that, it would be convenient for the users to make decision during the situation when battery is fully charged. Consequently, user needs to unplug the charger. Furthermore, in a situation where the battery percentage is too low and requires charging. Resulting in alerting the user to plug in the charger. The MEGAphone design also aims at providing similar feature of charge level detection for LiFePO4 battery incorporated in the design. There are two ways to implement this feature and are mentioned below,

- Battery charge controller IC
- Employing any one of the analogue inputs of LIS3DH accelerometer

In a situation where battery charge controller IC (Integrated Chip) is not able to provide the information regarding the charge level of battery, one of the analogue inputs of LIS3DH accelerometer comes in to the support.

Before concluding this discussion regarding the various functional blocks of the MEGAphone, the I2C IO expander inclusion to the design required for the various functional blocks to save the TE0725-03 TRM FPGA which thereby eases the pin management when the integrated design needs to be overlooked. A table is constructed to account the number of pins involved in various functional blocks that requires I2C IO expander as follows:

Functional Blocks	Number of pins
Four RGB LED's	16
Two x 9 Pin C64 Joystick	18
Four momentary action switches	8
Ambient light sensor	3
Proximity sensor	6
25 pin D-sub connector	25
Total	**76**

Table 29: Pin count for various functional blocks

In Chapter 9.31, one of the I2C IO expander has been already selected, that is, NXP semiconductors PCA9698 (NXP, 2010). This is basically, a 40 pin I2C IO expander. To accommodate above 76 pins, two of the PCA9698 I2C IO expander would be sufficient. Ultimately, this resolves the pin shortage issue with respect to TE0725-03 TRM FPGA that would arise when deriving the integrated design for the MEGAphone.

10. MISCELLANEOUS MODULE INTERFACES

10.1 Commodore 64 disk drive interface

This is possible by using one of DIN Chassis socket suitable for printed circuit board. The ideal DIN connector meeting the required criteria is DIN 45322 circular connector socket manufactured by Lumberg. The DIN 45322 is basically a 6-pole right angle DIN socket.

Figure 55: DIN 45322 Pin

The physical characteristics of the DIN 45322 can be referred in the DIN 45322 data sheet. The DIN 45322 is a female pin. The general pin assignment for a DIN 45322 Connector is tabulated as below:

Pin	Name	Direction	Description
1	/SRQIN	Input	Serial SRQIN
2	GND	-	Ground
3	ATN	Input/ output	Serial ATN in/ out
4	CLK	Input/ output	Serial CLK in/ out
5	DATA	Input/ output	Serial DATA In / out
6	/RESET	-	Reset

Table 30: Pin configuration of DIN 45322 Connector (HwB, n.d.).

This feature inclusion to the MEGAphone design requires some additional arrangements with the C64 disk drive port requiring 1 KΩ pull-ups and open-collector operation. Consequently, there should be a bus driver with output enable line, that enables it to be pulled low when activated and a second pin that allows reading the pin. This all needs to operate in the 5V domain. For the smooth operation, a level converters inclusion in both the directions may be appropriate. There are five such pins in this interface, that needs to be connected in this way.

10.2 Bluetooth module functioning

The Bluetooth module has been selected for the MEGAphone design. But, the functionality with respect to the MEGAphone is not assigned yet.

10.3 Cartridge Port

The cartridge port inclusion in to the MEGAphone as one of the functional blocks has been planned. This port is basically a Commodore 64 expansion port that is normally employed for connecting cartridges. This port requires too many pins and at this point of time, at this stage it is not possible to decide whether this can be included as it all depends on the number of pins available with respect to TE0725-03 TRM FPGA after all the main functional block inclusion.

10.4 Casing or physical structure

The implementation of the key idea such as simplified and secured design Smartphone through MEGAphone design has been worked out. With all the functionalities involved in the MEGAphone as discussed in Chapter 9, the depth (thickness) and dimension can be predicted approximately. The single cell LiFePO4 cell dimension is around 13 Centimetre with depth (thickness) being 1.4 Centimetre and LCD display size is 5-inch, which corresponds to 12.7 Centimetre. It would be ideal to obtain a mould with a dimension of 5.3 inch approximately along with depth of 2.2 Centimetre approximately that would fit in all the functional modules of the MEGAphone.

The above dimension consideration for casing is just an approximation and this basically serves as the reference for the future student, resuming this project. So, at this point of stage, this falls out of the scope.

10.5 Proposed complete prototype design

At this stage of the design, the proposed complete prototype design falls out of the scope of this project. But, in the process of deriving the schematics for each hardware interface or sub-system for the MEGAphone, various design challenges came into picture. One of the main challenge was, to sort out the required power supply for various components during the process of interfacing as the power requirement for the various components was not limited to single voltage level. Consequently, the incorporation of additional components to ensure proper voltage supply was sorted out. Due to this new challenge, delay in the design process was inevitable.

As the process of sub-system design for MEGAphone fetched a lot of time than expected. The goal of the MEGAphone project to derive the entire integrated design that would have aided in proposing complete prototype design has been out of scope at this point of time.

In near future, along with the sub-system design obtained so far, remaining sub system design needs to be worked out. Consequently, it is possible to derive an entire integrated design and develop the PCB layout. Ultimately, verification of the design is required for printing the circuit board to obtain the MEGAphone.

The power switching mechanism proposal that is considerable for the integrated design is derived with respect to the three major components in the MEGAphone such as FPGA, Wi-Fi module and 4G LTE module are depicted in the table as below:

4G enable switch	4G LTE module enabling via FPGA	Power switch	**4G LTE module Power**
1	1	X	**1**
X	0	X	**0**
0	X	X	**0**

Table 31: 4G LTE module powering mechanism.

In all the three cases, the power switch has no impact on powering the 4G LTE module.

From the above table, in the first case, it is evident that, the 4G LTE module is powered up(ON) only when, 4G switch is enabled and 4G LTE module is enabled via FPGA.

While, in the second case, if 4G switch is not considered (X) and even 4G LTE module is disabled via FPGA, the 4G LTE module is powered down (OFF).

Ultimately, in third case, the 4G switch is disabled, and 4G LTE module enabling via FPGA is not considered, the 4G LTE module is powered down (OFF).

Now considering the powering mechanism for Wi-Fi module:

Wi-Fi enable switch	Wi-Fi module enable via FPGA	Power switch	**Wi-Fi module Power**
1	1	X	**1**
X	0	X	**0**
0	X	X	**0**

Table 32: Wi-Fi module powering mechanism

The Wi-Fi module powering is like the mechanism of 4G LTE module powering. Again, in all the three cases, the power switch has no impact on powering the Wi-Fi module.

Now moving on to the FPGA powering, the below table depicts corresponding mechanism:

4G interrupt signal	Power Switch	FPGA self-enable	**FPGA power**
X	1	X	**1**
X	X	1	**1**
0	0	0	**0**
1	X	X	**1**

Table 33: FPGA powering mechanism

In the first case, 4G interrupt signal is not considered (X), power switch is enabled (1) and FPGA self-enable is not considered (X). Therefore, the FPGA is powered up (ON).

In the second case, 4G interrupt signal is not considered (X), power switch is not considered (X) and FPGA is self-enabled (1). Therefore, the FPGA is powered up (ON).

In the third case, 4G interrupt signal is disabled (0), power switch is disabled (0) and FPGA is not self-enabled (0). Therefore, the FPGA is powered down (OFF).

Ultimately, in fourth case, 4G interrupt signal is enabled (1), power switch is not considered (X) and FPGA self-enable is not considered (X). Therefore, the FPGA is powered up (ON).

11. SCHEMATICS

Some of the main functional blocks of the MEGAphone schematic are derived and discussed under this Chapter.

11.1 Single Cell LiFePO4 battery charger

In Chapter 9.1, the detail discussion regarding single cell LiFePO4 battery employed for the MEGAphone as power source has been carried out. The micro USB connector and ideal charger for this single cell LiFePO4 battery was also overviewed in Chapter 9.2. The LT3652HV, 2 A charger was the one that has been included in this design. The LT36552HV charger are available in the Altium library under Linear Technology Power Management Energy Harvesting.IntLib. The schematic drawn is as below:

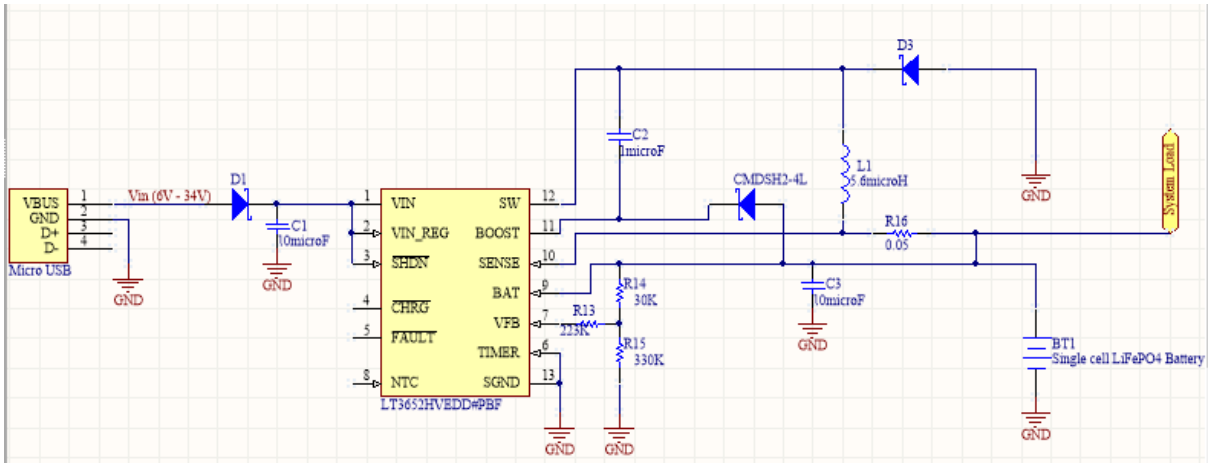

Figure 56: LT3652, 2A charger for single cell LiFePO4 battery (Linear Technology, 2017).

In the above schematic single cell battery needs to be added. But, it is not available in the miscellaneous device library of Altium designer, only dual cell battery component is available.

11.2 Controlled supply of 3.3 V from single cell LiFePO4 battery is drawn by employing DC-DC converter

To deliver the regulated supply of 3.3V from single cell LiFePO4 battery to various functional blocks of the MEGAphone, TPS61281A battery front end DC-DC converter is incorporated. The detail discussion regarding this module has carried out in Chapter 9.3. The TPS61281A provides simple logic interface and the corresponding schematic has been drawn and included below:

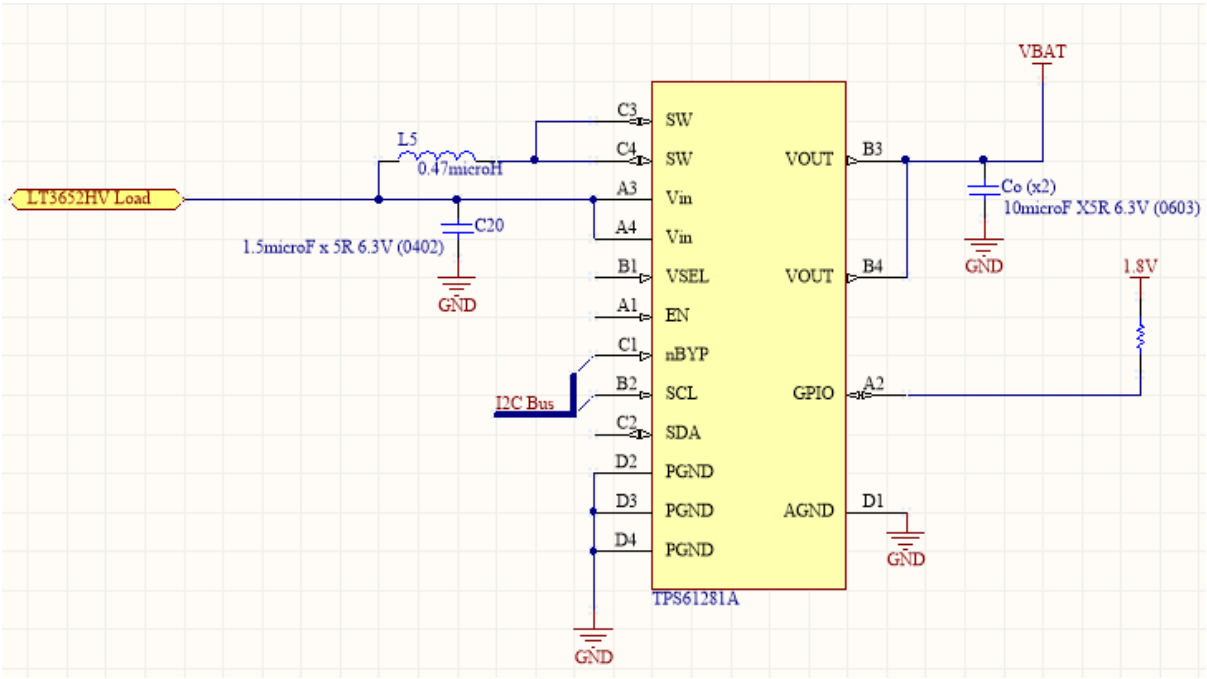

Figure 57: TPS61281A DC-DC converter for single cell LiFePO4 battery (Texas Instruments, 2016).

The LT365HV battery charger discussed earlier, corresponding output voltage is applied as load to the TPS61281A module. All the functional blocks of the MEGAphone requiring 3.3 V supply is drawn through TPS61281A VBAT pin.

11.3 Regulated 5 V Power supply required to drive some of the functional blocks of MEGAphone design via inclusion of 5 V DC-DC converter

Since the entire MEGAphone functional blocks cannot be driven by same voltage supply level. The required provision of various voltage levels is catered through inclusion of DC-DC converters. In Chapter 11.2, 3.3 V regulated supply through TPS61281A IC has been overviewed along with the schematic.

Here, in this section, selected IC (Integrated Chip), NCP1402, to obtain regulated 5V supply schematic design is overviewed which is essentially required to drive some of the functional blocks of the MEGAphone design such as, 1541 disk drive port, SX-64 keyboard and C-64 Joystick.

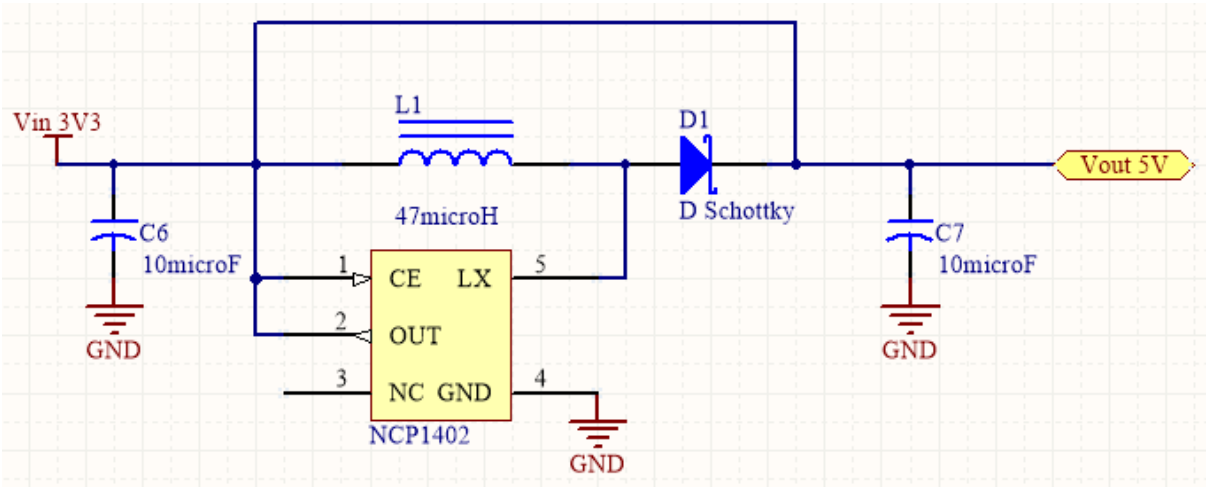

Figure 58: NCP1402 5V DC-DC converter (ON Semiconductor, 2014).

The voltage supply of 3.3 V generated via TPS61281A is fed as input to NCP1402 IC to obtain 5 V regulated power supply.

11.4 Power Indication LED for 4G LTE module

The implementation method for this step has been explained in the section 9.13. The calculation of suitable current limiting resistor requires the following data of the LED, such as forward voltage and forward current along with supply voltage provided. Forward voltage varies for different colours in an RGB LED, but the forward current is identical. In perspective to 5060000BRG4 RGB LED, the forward voltage for green light is 3.1 V, the forward current being 30 mA (Yetda Industry Ltd, n.d.) and the supply voltage, provided to Quectel EC25 module is 3.8 V. Now determining the required current limiting resistor (a1ronzo, 2010) with all the above data as follows,

$$R = \frac{V_s - V_f}{i}$$

$$= \frac{3.8 - 3.1}{30 * 10^{-3}} = 23.33\ \Omega$$

Therefore, the obtained current limiting resistor of 23.33 Ohm is a non-standard value. The standard value is considered by rounding down to 22 Ohm and this essentially stabilises the current through 5060000BRG4 RGB LED module during the event of green LED turn ON operation to indicate the power status of Quectel EC25 module.

The schematic drawn for indicating the power status for the 4G LTE module is as below:

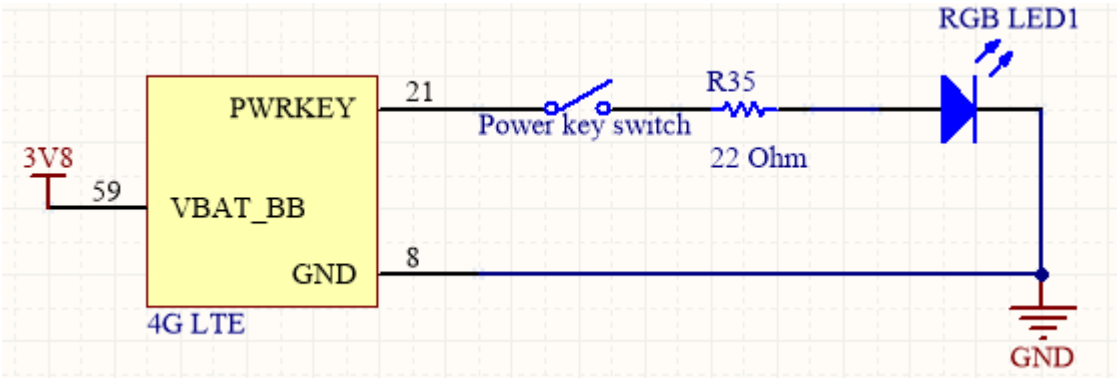

Figure 59: Power indication LED for 4G LTE (Quectel EC25) module

In the above schematic, the pin VBAT_BB is designated pin for powering the baseband part of the Quectel EC25 Mini PCIe module and the ground pin taken into consideration is pin 8. During the scenario, where the Quectel EC25 Mini PCIe module is powered, the power key switch is pressed to turn on the module. As soon as the Quectel EC25 Mini PCIe module is powered, the green LED glows, there by indicates the power ON status of the module.

11.5 Power Indication LED for FPGA board

In the Chapter 9.14, the discussion regarding this step implementation has been carried out. As considered in the previous schematic implementation for the Power indication LED for 4G LTE module by introducing the LED into the power rail, here also similar method is followed by considering the same LED as the previous one. But, here the supply voltage for TE0725-03 TRM FPGA is 3.3 V and thus, the current limiting resistor required will vary.

Consequently, the current limiting resistor requirement for glowing the Green LED of 5060000BRG4 RGB LED module has been calculated and standard value has been considered. So, the resultant current limiting resistor that needs to be employed in this step is 6.8 ohm.

The schematic drawn for indicating the power status for the FPGA board is as below:

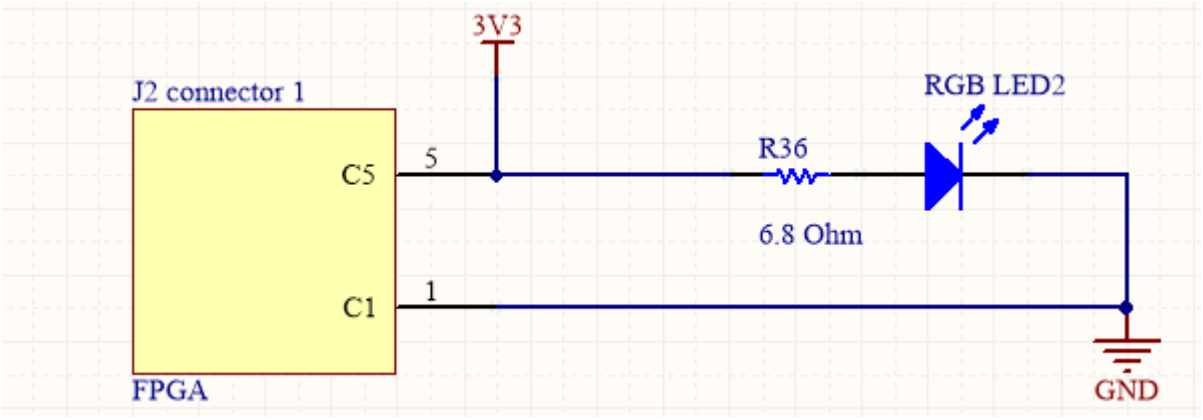

Figure 60: Power indication LED for FPGA (TE0725-03) board

The main motto behind the MEGAphone is to, simplify the design to elementary level. With that in mind, the external board connectors provision provided with TE0725-03 TRM FPGA are considered, as these are GPIO (General Purpose Input/ Output) pins which are user configurable. The header pins that can be connected to those external board connector slots, schematic representation can be referred in TE072-03 TRM FPGA datasheet (Trenz Electronic, 2017c).

Coming to the above schematic, the connector 2 (header pin) is considered for the design, with pin number 5 being, 3.3 V power rail and pin 1 being, ground. A basic LED drive circuit is included between the power pin and the ground pin along with matched current limiting resistor, incorporated to avoid LED burn out. The LED turns on the green light as soon as the connector is powered.

11.6 Power Indication LED for Wi-Fi module

As mentioned earlier, the Wi-Fi module considered in the MEGAphone design is Murata's, Type 1GC-Imp005. The detailed discussion regarding the various method to implement this functional block of MEGAphone is included in Chapter 9.15.

The second way of implementation is considered for the schematic design which involves the inclusion of green LED from Avago technologies, ASMT-UGB5-NV702 as discussed before in the Chapter 9.15 between the Wi-Fi module's power input terminal and the ground. The required pins from the Type 1GC-Imp005 for this step implementation has been overviewed under Chapter 9.15. Even the current limiting resistor that is required for the ASMT-UGB5-NV702 has been calculated and finalised with the standard value under the Chapter 9.15. With all these data, the schematic has been drawn and included below:

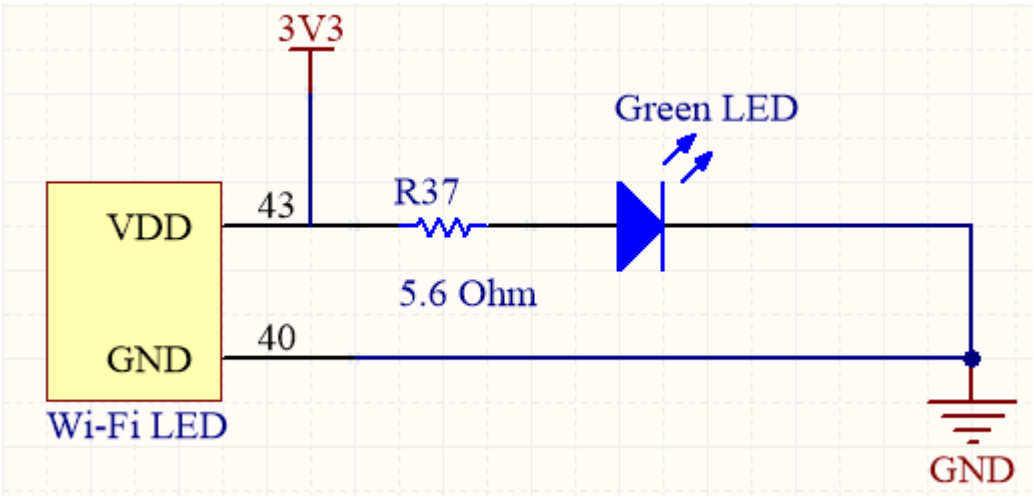

Figure 61: Power indication LED for Wi-Fi module (Murata, 2016).

The Wi-Fi module powering up is possible through the regulated 3.3 V supply voltage delivered by TPS61281A discussed under Chapter 11.2.

11.7 PCM, I2C, UART interface between FPGA board and 4G LTE module

Initially the UART interface between TE0725-03 TRM FPGA and Quectel EC25 4G LTE module are considered.

Since the Quectel EC25 module has two UART modes, main UART mode is considered and reason behind this has been discussed in the Chapter 9.30. The pin assignment for the main UART interface can be referred in Quectel EC25 Mini PCIe datasheet (Quectel, 2017). The voltage level required for operation by Quectel EC25 module and module UART interfacing voltage are not same and this has been thoroughly analysed under the section 9.30. Due to this voltage difference, the level translator chip (TXS0108EPWR) of Texas instrumented suggested by the Quectel EC25 module datasheet has been considered (Quectel, 2017). This translator chip converts 3.3 V input to 1.8 V. Here in the design, TE0725-03 TRM FPGA supplies 3.3 V to translator chip which is converted by translator chip to 1.8 V as it is the required operating voltage for Quectel EC25 module's UART interface.

Coming to the TE0725-03 TRM FPGA pins considered for this interface implementation, external connector slots provided by the board are considered which can be plugged with header pins. There are 100 external connector slots on board and out of 100, 86 are GPIO's (General Purpose Input Output) pins which are user configurable. So, J1 connector has 42 IOs and 8 pins are considered here along with supply voltage pin being 5 (C5).

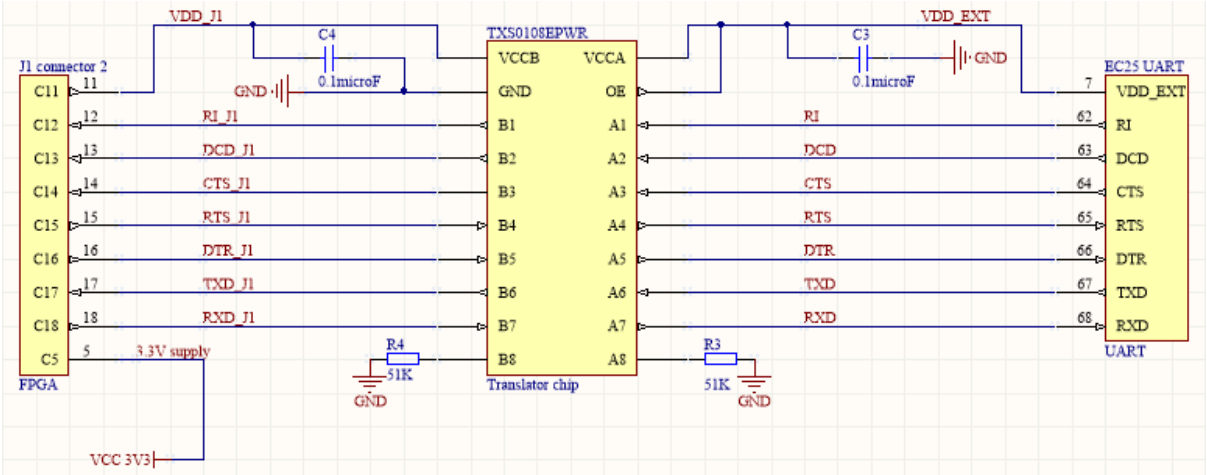

Figure 62: UART interface between TE0725-03 TRM FPGA and Quectel EC25 module.

The above schematic is drawn by referencing the reference circuit with translator chip (Quectel, 2017). The 3.3 V supply for the TE0725-03 TRM FPGA external connectors connected via header pins is obtained through TPS61281A DC-DC converter as discussed in Chapter 11.2.

The number of PCM interface and modes provided by the Quectel EC25 Mini PCIe module has been thoroughly discussed under the Chapter 9.30. The primary mode PCM interface is selected where in, the module can operate both as master and slave device and this is necessary for this functional block design of the MEGAphone. The Quectel EC25 PCM interface voltage requirement is 1.8 V and the supply provided by the TE0725-03 TRM FPGA is 3.3 V. To bring down the voltage from 3.3 V to 1.8 V, voltage level shifter has been employed. The Texas instruments, SN74LV1T34 is a logic level shifter that is capable for delivering the down translation from 3.3 V to 1.8 V. This level shifter is ideal for telecom oriented application. It is basically a five pin module and further information regarding the pin configuration and operating characteristics can be referred from datasheet (Texas Instruments, 2017b).

While coming to the I2C interface of the Quectel EC25 module, this interface functions as master device only and both I2C clock and data pins are open drain configured and requires the pull up resistor. Normally, for initial testing 4.7 Kilo Ohm pull up resistor is considered. The pin configuration for both PCM and I2C interface of Quectel EC25 Mini PCIe module can be referred from its datasheet (Quectel, 2017).

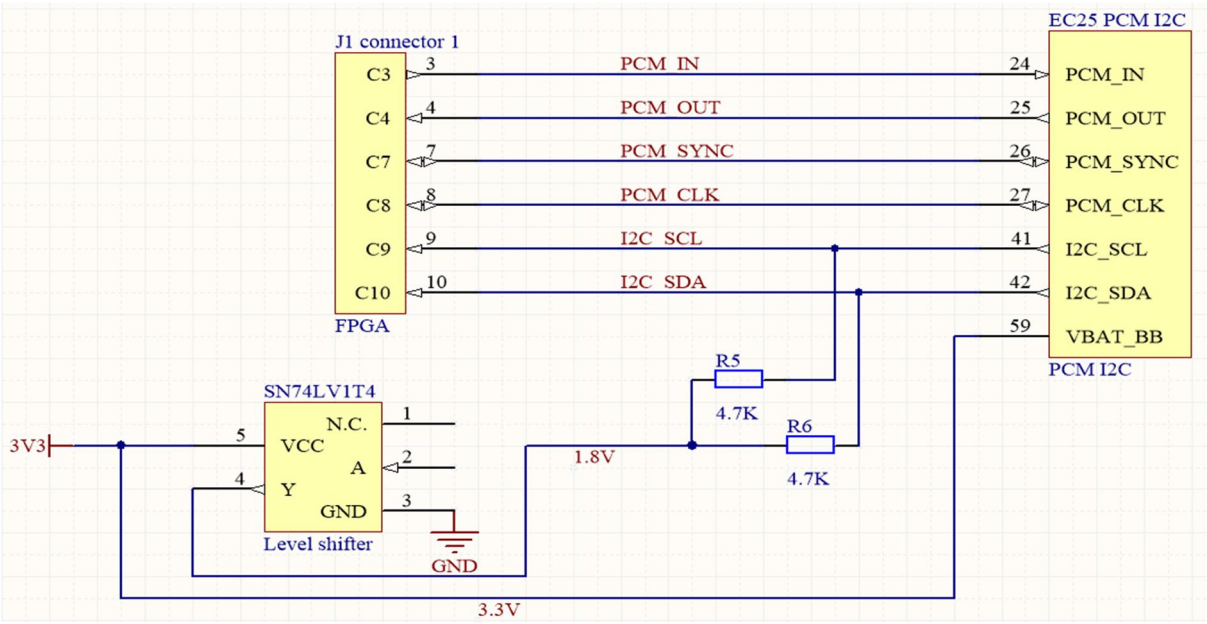

Figure 63: PCM and I2C interface between TE0725-03 TRM FPGA and Quectel EC25 4G LTE module

The above schematic is drawn by referencing the PCM and I2C interface with an external codec IC included in the datasheet (Quectel, 2017). For the MEGAphone design, external codec inclusion is not considered. The TE0725-03 TRM FPGA is only considered as codec. The 3.3 V supply for the TE0725-03 TRM FPGA external connectors connected via header pins is obtained through TPS61281A DC-DC converter as discussed in Chapter 11.2.

11.8 Interfacing Proximity sensor with FPGA

The proximity sensor requirement, preferred interface as well as the power supply requirement for the module has been sorted out in the section 9.36.

For the schematic design implementation depicting the APDS9130 proximity sensor interfaced via I2C interface to the TE0725-03 TRM FPGA, the APDS9130 datasheet has been referred. The below screen grab depicts the schematic obtained for this functional block of the MEGAphone.

Now moving on to the schematic discussion. The APDS9130 proximity sensor module can be driven by two power supplies or single power supply. It must be noted that, the entire MEGAphone is powered by a single cell LiFePO4 battery. As a result, single power supply method is considered. The Application information of hardware is described in APDS9130 datasheet (Avago Technologies, 2015), with this as reference proximity sensor part of the schematic has been derived.

In the APDS9130 module, I2C signals (SCL, SDA) and Interrupt are designated as open drain outputs. Consequently, the inclusion of pull up resistor in these lines are mentioned in APDS9130 datasheet (Avago Technologies, 2015). The value for the pull up resistor for the Interrupt line (R_{PI}) has been assigned as 10 kilo-ohm. But, the pull up resistors for I2C signal lines (R_P) needs to be calculated through I2C bus speed, I2C bus voltage and capacitive load.

The Texas instruments has precise information regarding the I2C bus pull up resistor calculation. By referring that, it was interpreted that, the calculation of pull up resistor requires following data such as, supply voltage (V_{DD} or V_{cc}), clock/ data rise time (t_r), low level output voltage in fast mode (V_{OL}) and corresponding, sink current (I_{OL}) also capacitive bus load for each bus line (C_b) (Texas Instruments, 2015).

The APDS9130 datasheet provides all the data required for the calculation. The data obtained are as follows,

Parameters	**Values**
Clock/ data rise time (t_r)	300 ns (Nano-seconds)
Supply voltage (V_{DD} or V_{cc})	3.3 V (Volt)
Output Voltage Level (V_{OL}(max))	0.4 V (Volt)
Sink current (I_{OL})	3 mA (milli-ampere)

Table 34: Data required for the I2C pull resistor calculation

But, capacitive bus load (C_b) is not given in the datasheet. As the APDS9130 operates in I2C fast mode providing up to 400 kHz, the capacitive load for this mode can be considered as 400 pF (pico-farad). Now, with the available data, the pull up resistors can be calculated using the following formulas (Texas Instruments, 2015).

$$R_P(max) = \frac{t_r}{0.8473 * C_b}$$

$$= \frac{(300 * 10^{-9})}{(0.8473 * 400 * 10^{-12})} = 885.16\ Ohm$$

$$R_P(min) = \frac{V_{cc} - V_{OL}(max)}{I_{OL}}$$

$$= \frac{(3.3 - 0.4)}{(3 * 10^{-3})} = 966.66\ Ohm$$

Therefore, the pull up resistor for I2C line is selected between 885.16 Ohm and 966.66 Ohm. The chosen pull up resistor in the schematic for both SCL (Serial Clock) and SDA (Serial Data) line is 910 Ohm.

Again, with respect to the TE0725-03 TRM FPGA, the external connectors are considered as these are user configurable Input/ Outputs pins there by eases. The J1 connector pins are considered. With all the necessary calculations and considerations discussed so far, the schematic to establish the I2C interface between APDS9130 proximity sensor and TE0725-03 TRM FPGA has been drawn and attached below:

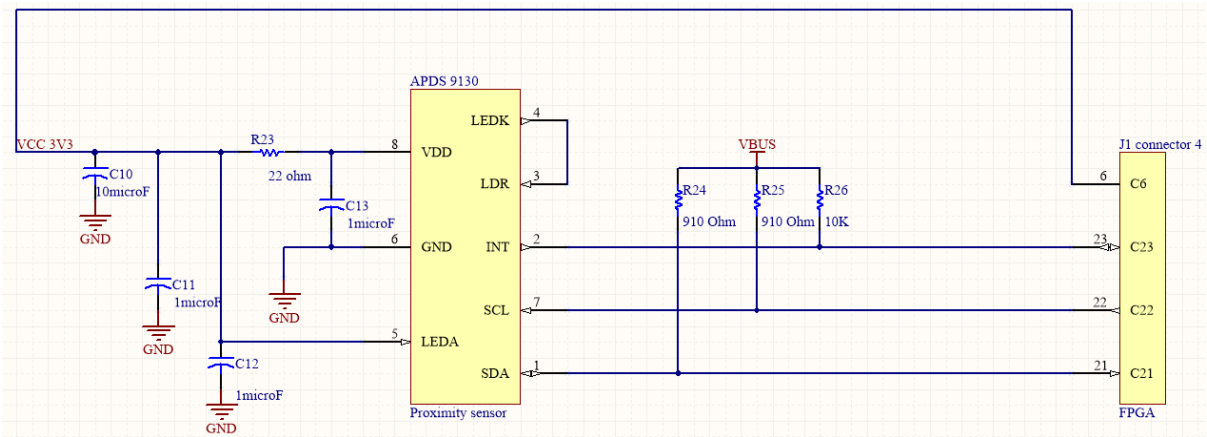

Figure 64: I2C interface between APDS9130 proximity sensor and TE0725-03 TRM FPGA

11.9 Microphone connected to FPGA

The detailed discussion regarding microphone inclusion and its function with respect to the MEGAphone has been discussed in Chapter 9.25. Consequently, Nexys4 DDR board microphone unit has been considered for the MEGAphone design and even, the discussion regarding that chip has been included in Chapter 9.25.

Coming to the schematic design of this functional block, with respect to the TE0725-03 TRM FPGA, again the boards external connectors connected via header pins are considered as these pins are user configurable input/ output pins and this would ease the design process.

The ADMP421 microphone datasheet, has the information regarding the application implementation (Analog Devices, 2011). The need for, the external codec must be investigated and this is possible once the result obtained by employing TE0725-TRM FPGA itself as codec is available. The hardware and software testing is out of scope in this project. So, for the schematic design, TE0725-03 TRM FPGA is considered as codec. The derived schematic is as below:

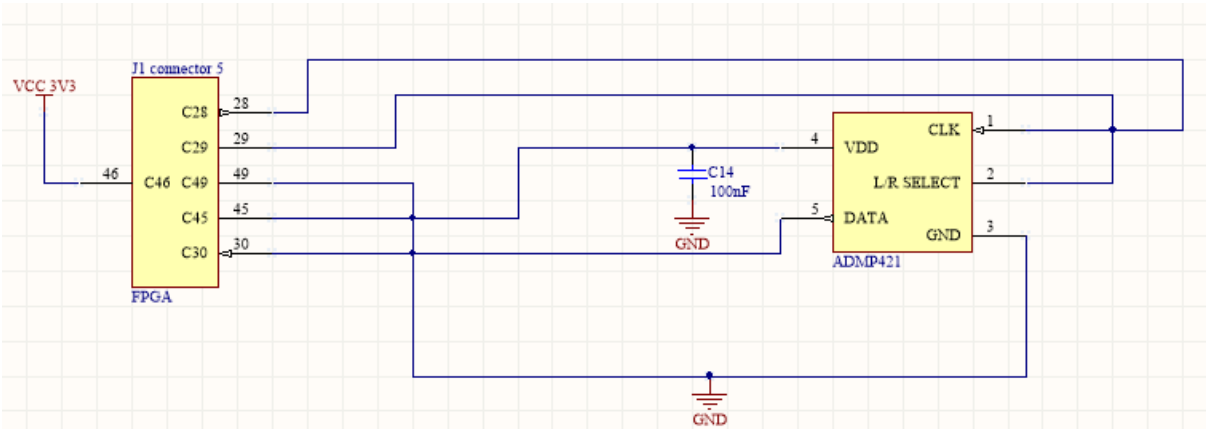

Figure 65: Interconnection of ADMP421 (Microphone) chip with TE0725-03 TRM FPGA

The 3.3 V supply for the TE0725-03 TRM FPGA external connectors connected via header pins is obtained through TPS61281A DC-DC converter as discussed in Chapter 11.2.

11.10 Real Time Clock interconnected to FPGA through I2C interface

Under the section 9.8, the Real-Time Clock (RTC) module to be incorporated has been discussed. The various function it delivers with respect to the MEGAphone has been discussed in Chapter 9.8 and 9.12 in detail.

Now in this section, the general schematic design is derived for the interconnection of TE0725-03 TRM FPGA and the PCF8563TS/5 RTC module via I2C interface. It is required to calculate

suitable pull up resistor that should be included along the I2C signal lines, SCL (Serial Clock) and Serial Data. The PCF8563TS/5 RTC module delivers two I2C modes, standard and fast mode. Considering the standard mode for the MEGAphone design, the pull up resistor can be calculated by noting down the, rise time of both SDA and SCL signals (t_r) in standard mode and capacitive load for each bus line (C_b). By referring the PCF8563 datasheet, the corresponding values were noted, $t_r = 1\ \mu s$ and $C_b = 400$ pF (NXP, 2015). Therefore, the pull up resistor are calculated as follows,

$$R = \frac{t_r}{C_b} = \frac{1 * 10^{-6}}{400 * 10^{-12}} = 2.5\ K\Omega$$

The supply voltage range required for the PCF8563 RTC module is in the range of -0.5 to 6.5 V and through TE0725-03 TRM FPGA, 3.3 V supply is deliverable.

With respect to the TE0725-03 TRM FPGA, again board external connector slots connected via header pins (J1 connector) are considered for interfacing as it is user configurable input/ output pins. The schematic design is obtained by referring application diagram of PCF8563 module (NXP, 2015). The resultant schematic is as below:

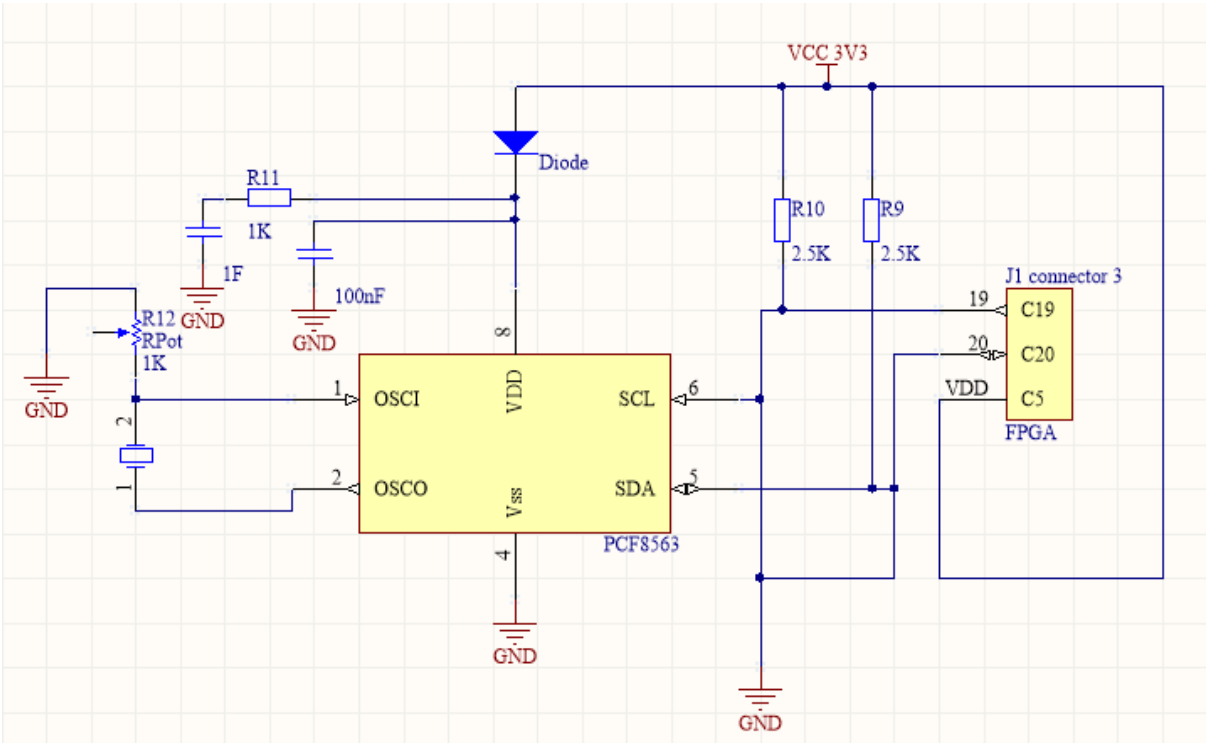

Figure 66: I2C interface between PCF8563TS/5 RTC module and TE0725-03 TRM FPGA

11.11 Interconnection of Accelerometer to FPGA through I2C interface

A detail information regarding the accelerometer functioning and the module that is employed for the MEGAphone design has been included in Chapter 9.20.

By referring the application implementation diagram of LIS3DH accelerometer (ST, 2016), the schematic design has been derived.

Again, with respect to TE0725-03 TRM FPGA, the external connector slots that is connectable via header pins (J1 connector) are considered for interfacing.

The derived schematic is as below:

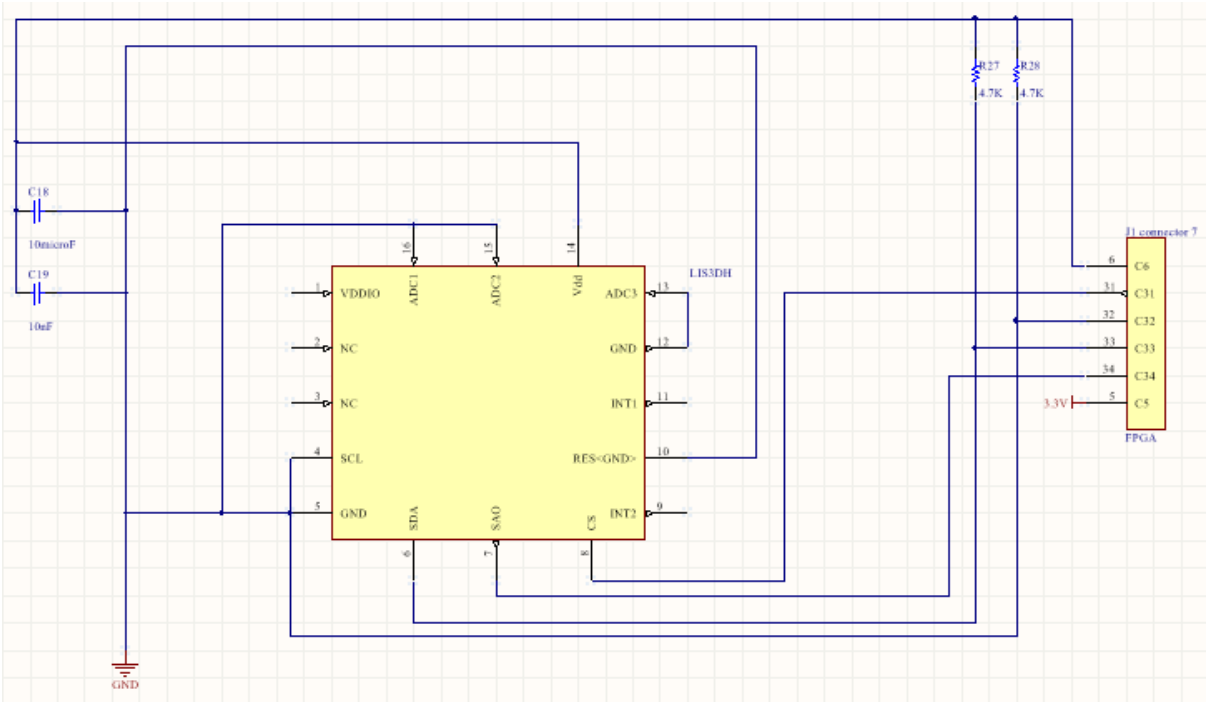

Figure 67: I2C interface between LIS3DH accelerometer and TE0725-03 TRM FPGA connector

12. CONCLUSION

So far, the entire process of the MEGAphone design has been discussed in detail. The schematic design of some of the main individual functional blocks has been completed. There are few specific areas out of the entire design that needs progression in the near future and this includes, LCD screen interfacing with respect to FPGA and various minor functional blocks schematic needs attention. Once all the individual functional blocks schematics are obtained, it would be ideal to combine all of those to derive an integrated design. Before laying out the PCB design, it would be ideal to the test hardware components of each individual functional blocks. Even, for the thorough interpretation of hardware functioning for main module such as 4G LTE module and Wi-Fi module, considering the evaluation board would be a right choice in the process of obtaining the bench prototype design. Once, the bench prototype design is functional, the final process of the PCB design can be initiated.

Conclusively, during this process of designing a Simple and Secured Smartphone, various new challenges evolved. The initial plan of employing Fairphone 2 as platform did not yield the positive result and the reason behind this setback has been discussed under modular phone chapter. Alternative plan of deriving the Artix7 FPGA based Smartphone, the MEGAphone using MEGA65 design was initiated and the entire process involved in the design right from drawing the functionality, identification of ports and modules, selection of suitable cellular modules, FPGA has been thoroughly analysed and discussed under the corresponding Chapters. Once all the main functional modules were selected, the detail discussion of each functional block has been discussed. At every stage of functional block implementation of the MEGAphone, the pin usage is optimised by considering various sub modules to include all the functionalities of the MEGAphone. Throughout the design process, the concept of simplicity and security is maintained by considering the serial interface protocols for all the functional blocks of the MEGAphone. The security oriented functional blocks are discussed. By this way, the security is ensured and even a user with minimum knowledge regarding the interface can interpret this design. Ultimately, even the practicality of the MEGAphone design has been analysed.

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Appendix A

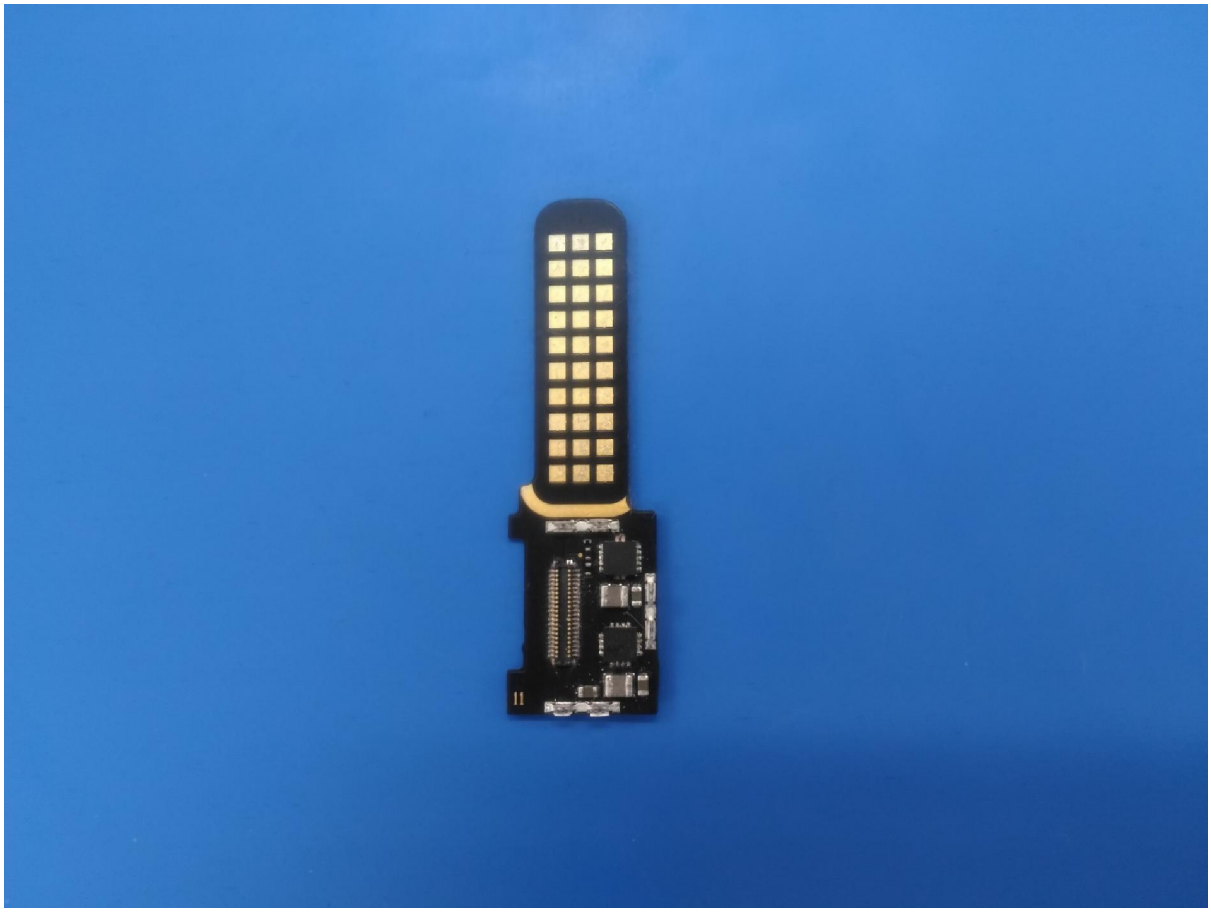
Reverse Engineering the Fairphone 2 Screen

The broken Fairphone 2 screen, used for analysing the internal circuitry design through continuity test.

Figure 68: Fairphone 2 screen inner panel view

In the above image, the internal circuitry of the screen module is enclosed by steel casing. By removing the casing, the continuity test is performed by employing multi-meter and this is observable from the following images.


Made on 03.01.2016
FAIRPHONE
THIS PHONE IS OUR
NEXT STEP TOWARDS
FAIRER ELECTRONICS
Thanks for being part
of the journey
CE 1588
A16AK10252



Initially, the Pogo Pins Interconnection in the screen were tested using the multi-meter for the total of thirty pins and consequently, data recorded are tabulated as follows,

Pin Number	Interconnected Pins	Common(Grounded)	Resistance (Ω)
1	-	-	-
2	3, 4, 5, 12, 14, 21, 22, 23, 30	-	687
3	-	4, 5, 12, 14, 21, 22, 23, 30	-
4	-	5, 12, 14, 21, 22, 23, 30	-
5	-	12, 14, 21, 22, 23, 30	-
6	-	-	-
7	-	-	-
8	-	-	-
9	-	-	-
10	-	-	-
11	-	-	-
12	-	14, 21, 22, 23, 30	-
13	-	-	-
14	-	21, 22, 23, 30	-
15	-	-	-
16	-	-	-
17	-	-	-
18	-	-	-
19	-	-	-
20	-	-	-
21	-	22, 23, 30	-
22	-	23, 30	-
23	-	30	-
24	-	-	-
25	-	-	-
26	30	-	722
27	-	-	-
28	-	-	-
29	30	-	744

Pogo Pins and main circuitry board pin Interconnection. The fairphone2 has thirty pogo pins and forty main circuitry pins. Initially, pogo pins interconnection with even pins are tested and tabulated as following,

Pogo Pin number	Main circuitry Pins(Even)	Common(Grounded)	Resistance (Ω)
1	16	Yes	-
2	10 20, 22, 24, 36 26 30	-	687 691 834 792
3	10, 20, 22, 36 38, 40	Yes -	- 1227
4	10, 20, 22, 36 38, 40	Yes -	- 1225
5	10, 20, 22, 36 38, 40	Yes -	- 1222
6	-	-	-
7	6	Yes	-
8	-	-	-
9	-	-	-
10	14	Yes	-
11	-	-	-
12	40 10, 20, 22, 36, 38	Yes -	 1215
13	12	Yes	-
14	10, 20, 22, 36 38, 40	Yes -	- 1210
15	-	-	-
16	8	Yes	-
17	-	-	-
18	-	-	-
19	32	Yes	-
20	-	-	-

21	10, 20, 22, 36 38, 40	Yes -	- 1210
22	10, 20, 22, 36 38, 40	Yes -	- 1207
23	10, 20, 22, 36 38, 40	Yes -	- 1210
24	-	-	-
25	-	-	-
26	10, 20, 22 36	-	720
27	-	-	-
28	-	-	-
29	10, 20, 22 36	-	740
30	10, 20, 22, 36 38, 40	Yes -	- 1205

Pogo pins interconnection with odd pins are tested and tabulated as following,

Pogo Pin number	Main circuitry Pins(Odd)	Common(Grounded)	Resistance (Ω)
1	-	-	-
2	3, 9, 15, 23, 27, 33 37, 39	-	687 1053
3	3, 9, 15, 21, 27, 33 37, 39	Yes -	- 800
4	3, 9, 15, 21, 27, 33	Yes	-
5	3, 9, 15, 21, 27, 33 1 37, 39	Yes - -	- 725 1277
6	13	Yes	-
7	-	-	-
8	7	Yes	-
9	11	Yes	-
10	-	-	-

11	5	Yes	-
12	3, 9, 15, 21, 27, 33 1 37, 39	Yes - -	- 721 1268
13	-	-	-
14	3, 9, 15, 21, 27, 33 37, 39	Yes -	- 1267
15	23	Yes	-
16	-	-	-
17	19	Yes	-
18	23	Yes	-
19	-	-	-
20	17 19	Yes -	- 1044
21	3, 9, 15, 21, 27, 33 1 19 37, 39	Yes - - -	- 725 1150 1262
22	3, 9, 11, 13, 15, 17 21, 27, 33 1 37, 39	Yes - -	- 723 1260
23	3, 9, 15, 21, 27, 33 1 37, 39	Yes - -	- 723 1260
24	3, 9, 11, 15, 17, 21, 23, 25, 27, 29, 31, 33 1 13 37, 39	Yes Yes - - -	- - 733 122 1253
25	-	-	-
26	-	-	-
27	3, 9, 11, 13, 15, 17, 21, 23, 25, 27, 29, 33	Yes Yes	- -

	1 19 37, 39	- - -	722 144 1256
28	-	-	-
29	-	-	-
30	3, 9, 11, 13, 15, 17, 21, 23, 25, 27, 29, 31, 33 1 19 37, 39	Yes Yes - - -	- - 720 143 1253

IC BCQ 56k A23P

The IC BCQ56k A23P is basically a 14 pin IC. The interconnection of this IC with pogo pins are tested by employing the multi-meter keeping the pogo pins as common (grounded). The below tabulation depicts the recorded observations.

Pogo Pin Number	IC pin number	Common(Grounded)	Resistance (Ω)
1	-	-	-
2	6, 7, 8, 13, 14	-	689
3	6, 7, 10, 13, 14	Yes	-
4	6, 7, 10, 13, 14	Yes	-
5	6, 7, 10, 13, 14	Yes	-
6	6, 7, 10, 13, 14	Yes	-
7	-	-	-
8	6, 7, 10, 13, 14	-	112
9	6, 7, 10, 13, 14	Yes	-
10	-	-	-
11	-	-	-
12	6, 7, 10, 13, 14	Yes	-
13	-	-	-
14	6, 7, 10, 13, 14	Yes	-
15	-	-	-

16	-	-	-
17	6, 7, 10, 13, 14	-	86
18	6, 7, 10, 13, 14	-	76
19	-	-	-
20	6, 7, 10, 13, 14	Yes	-
21	6, 7, 10, 13, 14	Yes	-
22	6, 7, 10, 13, 14	Yes	-
23	6, 7, 10, 13, 14	Yes	-
24	6, 7, 10, 13, 14	Yes	-
25	-	-	-
26	5, 8 6, 7, 10, 13, 14 11, 12	Yes - -	- 712 875
27	6, 7, 10, 13, 14	Yes	-
28	-	-	-
29	6, 7, 10, 13, 14	-	737
30	6, 7, 10, 13, 14	Yes	-

IC CCR T13BK CRPE

The IC CCR T13BK CRPE A23P is basically a 16 pin IC. The interconnection of this IC with pogo pins are tested by employing the multi-meter keeping the pogo pins as common (grounded). The below tabulation depicts the recorded observations.

Pogo Pin Number	IC pin number	Common(Grounded)	Resistance (Ω)
1	2, 3 5, 11, 12 6 10 14, 15, 16	- - - - -	1017 757 1170 1381 1130
2	1 2, 3 4	Yes - -	- 985 1091

	5 6 11, 12 13, 14, 15, 16	- - - -	687 1140 684 788
3	2, 3 5, 11, 12 6 9 14, 15, 16	- Yes - - -	802 - 859 1205 846
4	2, 3 5, 11, 12 6 9, 10 13, 14, 15, 16	- Yes - - -	802 - 859 1201 852
5	2, 3 5, 11, 12 6 9, 10 13, 14, 15, 16	- Yes - - -	805 - 862 1203 852
6	2, 3 5, 11, 12 6 9, 10 13, 14, 15, 16	- Yes - - -	806 - 863 1203 854
7	-	-	-
8	-	-	-
9	2, 3 5, 11, 12 6 9, 10 13, 14, 15, 16	- Yes - - -	804 - 860 1201 845
10	-	-	-

11	-	-	-
12	2, 3 5, 6, 11, 12 9, 10 13, 14, 15, 16	- Yes - -	798 - 1128 848
13	-	-	-
14	1 2, 3 4 5, 11, 12 6 9, 10 13, 14, 15, 16	- - - Yes - - -	1000 796 801 - 853 1385 840
15	-	-	-
16	-	-	-
17	1 2, 3, 4 5, 11, 12 6 9, 10 13, 14, 15, 16	- - - - - -	1032 832 53 870 1406 856
18	1 2 3,4 5, 6, 11, 12 9, 10 13, 14, 15, 16	- - - Yes - -	1024 824 72 - 1392 842
19	-	-	-
20	1 2 3, 4, 5, 6, 11, 12 9, 10 13, 14, 15, 16	- - Yes - -	998 796 - 1384 836

21	1	-	996
	2, 3, 4	-	794
	5, 6, 11, 12	Yes	-
	9, 10	-	1386
	13, 14, 15, 16	-	835
22	1	-	996
	2, 3, 4	-	794
	5, 6, 11, 12	Yes	-
	9, 10	-	1378
	13, 14, 15, 16	-	833
23	1	-	994
	2, 3, 4	-	794
	5, 6, 11, 12	Yes	-
	9, 10	-	1378
	13, 14, 15, 16	-	833
24	1	-	996
	2, 3, 4	-	796
	5, 6, 11, 12	Yes	-
	9, 10	-	1378
	13, 14, 15, 16	-	832
25	-	-	-
26	1	-	1328
	2	-	1068
	3, 4	-	1070
	5, 6	-	712
	11, 12	-	710
	13, 14, 15, 16	-	1102
27	1	-	998
	2, 3, 4	-	799
	5, 6, 11, 12	Yes	-
	9, 10	-	1388
	13, 14, 15, 16	-	834
28	-	-	-

29	1	-	1324
	2, 3, 4	-	1068
	5, 6, 11, 12	-	733
	13, 14, 15, 16	-	1100
30	1	-	992
	2, 3, 4	-	792
	5, 6, 11, 12	Yes	-
	9, 10	-	1373
	13, 14, 15, 16	-	832

The top horizontally mounted SMD Resistor is tested for its resistance. Consequently, the resistance recorded was, 0.3Ω. As it is known that, the resistor does not have the polarity. So, when tested with both the ends of the resistor yielded same readings during the determination of interconnection with Pogo pins. During testing, it was noticed that, only pogo pin number 26, had common (grounded) connection with this resistor.

Now moving on to the horizontally mounted SMD resistor at the bottom, again the resistor was tested for its resistance and 0.2Ω was the recorded resultant resistance. To test this resistor interconnection with pogo pins, multi-meter was used and observations were recorded and tabulated below.

Pogo Pin Number	Resistance (Ω)
2	783
3	843
4	843
5	843
9	853
12	842
14	842
15	903
18	1400 – 1600 (varying)
21	841
22	841

23	841
26	1109
29	1109
30	841

After the testing of the two resistors, the presence of some more SMD components were noticed. Basically, these components were smaller than SMD resistor and when tested for its resistance, it did not yield any variation in the readings and was steady. Conclusively, it was evident that it was not a resistor and multi-meter settings turned to farad mode to test for its capacitance. Ultimately, the multi-meter displayed the readings, as a result it was possible to determine that remaining components are the capacitors. So, there are three of them, yet again the interconnection with pogo pins of these three capacitors are initially recorded and tabulated as follows.

On the top, a vertically mounted SMD capacitor was tested for its capacitance and the recorded capacitance was 7.76μF. To test its interconnection with Pogo pins, multi-meter common pin was placed on pogo pins and tested. Correspondingly, the readings are tabulated as below,

Pogo Pin number	Top notch (Ω)	Common (grounded)
2	692	No
3	-	Yes
4	-	Yes
5	-	Yes
6	1660	No
9	-	Yes
12	-	Yes
14	-	Yes
15	314	No
17	142	No
18	-	Yes
20	282	No
21	-	Yes
22	-	Yes

23	-	Yes
24	-	Yes
26	715	No
29	738	No
30	-	Yes

When measured with the bottom notch of the same capacitor, following recordings were obtained as tabulated below,

Pogo Pin number	Bottom notch (Ω)	Common (grounded)
2	1052	No
3	802	No
4	802	No
5	802	No
6	855	No
9	807	No
12	802	No
14	802	No
15	896	No
17	858	No
18	810	No
20	816	No
21	800	No
22	800	No
23	800	No
24	800	No
26	1076	No
29	1080	No
30	800	No

The second capacitor at the lower end with vertical mounting was tested for its capacitance, the reading obtained was 8.40μF. Again, the interconnection of this capacitor with pogo pins are tested by placing the multi-meter common probe on pogo pins and recordings were obtained for both top and bottom notch of the capacitor as follows.

Pogo Pin number	Top notch (Ω)	Common (grounded)
2	-	Yes
3	1001	No
4	1001	No
5	1001	No
6	1050	No
9	1006	No
12	1001	No
14	1001	No
15	1088	No
17	1004	No
18	1007	No
20	1015	No
21	1000	No
22	1000	No
23	1000	No
24	1000	No
26	1334	No
29	1334	No
30	1000	No

When measured with the bottom notch of the same capacitor, following recordings were obtained as tabulated below,

Pogo Pin number	Bottom notch (Ω)	Common (grounded)
2	689	No
3	-	Yes
4	-	Yes

5	-	Yes
9	-	Yes
12	-	Yes
14	-	Yes
15	-	Yes
17	-	Yes
18	-	Yes
20	-	Yes
21	-	Yes
22	-	Yes
23	-	Yes
24	-	Yes
26	720	No
29	737	No
30	-	Yes

The third capacitor at the bottom is horizontally mounted and capacitance of this capacitor was found to be 7.92 μF. The possible interconnection with the pogo pins is determined by employment of multi-meter.

Pogo Pin number	Left notch (Ω)	Common (grounded)
2	689	No
3	-	Yes
4	-	Yes
5	-	Yes
9	-	Yes
12	-	Yes
14	-	Yes
15	-	Yes
17	-	Yes
18	-	Yes
20	-	Yes

21	-	Yes
22	-	Yes
23	-	Yes
24	-	Yes
26	720	No
29	736	No
30	-	Yes

When measured with the right notch of the same capacitor, following recordings were obtained as tabulated below,

Pogo Pin number	Top notch (Ω)	Common (grounded)
2	1312	No
3	764	No
4	1386	No
5	1386	No
9	1392	No
12	1386	No
14	1388	No
15	1415	No
17	1393	No
18	1496	No
20	1408	No
21	1388	No
22	1388	No
23	1388	No
24	1388	No
30	1386	No

So far, the resistors and the capacitors continuity test was performed to determine the interconnection with respect to the pogo pins. It is also essential to perform the continuity test between resistors and main frame pins also the capacitors with main frame pins. The following section depicts the test performed on a one to one basis.

In the process of testing, the common probe of multi-meter is placed on resistor and red probe on main frame pins. The testing of top resistor having a resistance of 0.3Ω with main frame pins are tabulated with even and odd pins of main frame tabulated individually as follows,

Main frame pin number (Even)	Resistance (Ω)
2	860
10	717
20	716
22	716
24	1756
26	1716
28	1734
30	1755
36	714

Main frame pin number (Odd)	Resistance (Ω)
3	720
5	790
9	719
15	721
21	721
27	717
33	717
37	1069
39	1069

The testing of bottom resistor having a resistance of 0.2Ω with main frame pins are tabulated with even and odd pins of main frame tabulated individually as follows,

Main frame pin number (Even)	Resistance (Ω)
10	762
20	762
22	762
24	1244
26	1247
28	1247
30	1247
36	760
38	1364
40	1364

Main frame pin number (Odd)	Resistance (Ω)
3	760
9	760
15	757
21	757
27	757
33	751
37	787
39	787

The capacitor testing with respect to the main frame pins is initiated in this section. As discussed earlier, there are three capacitors and appears to be non-polarised as the capacitors mounted are tested individually and tabulated as below.

The vertically mounted capacitor at the top having the capacitance of 7.76μF is tested with even and odd pin numbers of main frame individually as follows:

Main frame pin number (Even)	Common (grounded)	Resistance (Ω)
10	Yes	-
18	Yes	-
20	Yes	-
22	No	1234
26	No	1234
24	No	1234
28	No	1234
36	Yes	-
38	No	1356
40	No	1356

Main frame pin number (Odd)	Common (grounded)	Resistance (Ω)
3	Yes	-
9	Yes	-
15	Yes	-
21	Yes	-
27	Yes	-
33	Yes	-
37	No	782
39	No	782

The vertically mounted capacitor at the bottom having the capacitance of 8.40µF is tested with even and odd pin numbers of main frame individually as follows,

Main frame pin number (Even)	Common (grounded)	Resistance (Ω)
10	No	681
20	No	681
22	No	681

24	No	774
26	No	770
28	No	807
30	No	770
36	No	683
38	No	1880
40	No	1880

Main frame pin number (Odd)	Common (grounded)	Resistance (Ω)
3	No	682
9	No	682
15	No	682
21	No	682
27	No	682
33	No	682
37	No	1023
39	No	1023

The horizontally mounted capacitor at the bottom having the capacitance of 7.92µF is tested with even and odd pin numbers of main frame individually as follows. Initially, right notch of the capacitor is measured along with main frame pins as below,

Main frame pin number (Even)	Common (grounded)	Resistance (Ω)
10	No	770
20	No	770
22	No	770
24	No	1715
26	No	1716
28	No	1780
30	No	1725

36	No	770
38	Yes	-
40	Yes	-

Main frame pin number (Odd)	Common (grounded)	Resistance (Ω)
3	No	760
9	No	763
11	No	762
15	No	760
21	No	760
27	No	760
33	No	760
37	No	1056
39	No	1056

The left notch of the capacitor is measured along with main frame pins as below,

Main frame pin number (Even)	Common (grounded)	Resistance (Ω)
10	Yes	-
20	Yes	-
22	Yes	-
26	No	1245
30	No	1252
36	Yes	-
38	No	1374
40	No	1374

Main frame pin number (Odd)	Common (grounded)	Resistance (Ω)
3	Yes	-
9	Yes	-
15	Yes	-
21	Yes	-
27	Yes	-
33	Yes	-
37	No	793
39	No	793