MASTER OF ENGINEERING (ELECTRONICS)

Design and image processing of home–based medical devices for CKD monitoring

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DECLARATION

I, Hanqin Yang, hereby acknowledge, in accordance with the Flinders University's policy on plagiarism, that the content of this report is of my own and nobody else's.

<Hanqin Yang>

<September 2019>

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With the constant help of my topic coordinator and team members, my project can finally successful and achieve productive results.

ABSTRACT

Chronic kidney disease (CKD) refers to all conditions of the kidney, lasting at least 3 months. CKD is categorized into 5 stages according to the level of reduced kidney function and evidence of kidney damage. Evidence of kidney damage manifests as either urinary protein or albumin (a type of protein that is a more sensitive and specific marker of kidney disease), blood in the urine, or scarring detected by imaging tests.

CKD is often referred to as a "silent disease" because up to 90% of kidney function is lost before symptoms appear. As a result, many people do not know that they have this situation. CKD is largely preventable, as long as a simple test of human blood and urine can determine most of the CKD cases at an early stage of the disease, thereby preventing or slowing its progression. Many of the risk factors for CKD also apply to other chronic diseases such as cardiovascular disease (including coronary heart disease and stroke) and diabetes, which are risk factors for CKD.

Traditional CKD monitoring testing requires patients to go to the hospital on a regular basis, which is time consuming, expensive and requires highly trained medical staff and sophisticated diagnostic equipment. Therefore, this project is aim to develop a home-based medical devices for CKD monitoring which patients are able to do the tests at home by themselves with a potable, convenient and affordable device.

Aggregation-induced emission (AIE) bioprobe is used to detect human serum albumin (HSA) concentration ranges in urine for early detection of chronic kidney disease. In the presence of HAS, the non-luminescent bio probe become emissive and visible. In the black box experiment environment, use ultraviolet light to excite the testing cuvette. Then use camera (TRDB-D5M) to record the level of fluorescence. After image processing of micro controller FPGA (Field Programmable Gate Array), the correlation between light intensity and HSA concentration will be determined. The medical device in this project is low cost, efficiently, reliably, sensitive, fast, user-friendly, and is expected to help users to monitor early stage of chronic kidney disease at home.

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1. Introduction

This project is to design a home-based urine testing device that allows patients to detect CKD at home. In a lightweight, low-cost Black Box with UV lights inside, the user can add a test solution to the urine according to the given instructions and use the camera to capture a test tube image to detect the corresponding HSA concentration in the urine. The testing solution contains a aggregation-inducing emission (AIE) bio-probe that emits fluorescence when HSA is present in the urine. After camera image acquisition and image processing of micro controller FPGA, the patient's HSA concentration range level can be determined. The device is very suitable for early detection of kidney disease and allow patients to do their own urine tests at home.

Due to the rapid development of FPGA, it has been applied to more and more medical device fields as its high flexibility, short development cycle and high parallel computing efficiency. FPGA is semiconductor digital integrated circuit in which most of the internal circuit functions can be changed as needed. Since Xilinx created FPGA in 1984, with performance, cost, stability, and long-term maintenance advantages, this programmable logic device has been applied in communications, medical, industrial, and security fields.

The characteristics of the FPGA determine its unique advantages in the medical field, medical images have more textures, higher resolution, greater correlation, and greater storage space requirements than ordinary images. To ensure the reliability of clinical applications, the image compression, segmentation and other image pre-processing and image analysis are more demanding.

As FPGA are able to accelerate image compression, remove redundancy, increase compression ratio, and ensure image diagnostic reliability. Also, with the advantages of low-cost and low-power. This project Design and Develop Home-based CKD monitoring Medical Device is based on FPGA.

2. Literature Review

The Literature Review follows critically reviews contemporary literature regarding medical devices for Chronic kidney disease (CKD) monitoring. Early studies in the area (Diana Smith, 2018) in Chronic Kidney Disease generally concluded that Point Of Care (POC) tests can detect CKD in the laboratory by measuring albumin in the urine. Another laboratory testing product which is the Fully Automated Urine Analyzer AUTION MAX AX-4060 from arkray (Singapore), by measuring turbidity and colour tone in the urine based on test strip. However, these CKD monitoring devices require patients to go to the testing clinic on a regular basis, it is time consuming and costly. Moreover, trained staff and doctors are required for the current testing. The research (IEEE Transactions on Industrial Informatics) stated a powerful indicator for detecting the earliest signs of kidney disease, they developed a bio probe which is synthetically readily accessible and environmentally stable for HSA detection and quantitation. By using aggregation-induced emission bio probes for CKD monitoring, patients can reliably perform their own tests at home without the intervention of a medical professional. This project therefore proposes the development of a FPGA based medical device that is user friendly and affordable for patients who can monitor kidney function at home by themselves.

Initial sections discuss the CKD in Australia, CKD monitoring, excising medical device, image processing and analysis technology. The conclusion of the Literature review summaries and critique of the existing literature, followed by a discussion of the home-based device research progress, and hypotheses suggested by the review and examined in this thesis.

2.1 Chronic kidney disease (CKD) in Australia

According to the statistics from Kidney Health Australia, CKD is a significant and growing public health issue, responsible for a substantial burden of illness and premature mortality. More than 1.5 million which means 10% do not know they have indicators of the CKD, such as reduced kidney function or the presence of albumin in the urine. One in three Australians is at an increased risk of developing

CKD. 42% of people over the age of 75 have an indicator of CKD, and people with CKD have a two to three-fold greater risk of cardiac death than people without the disease. [1]

As CKD is irreversible, frequently progressive and tends to present insidiously, it is essential to detect and managed appropriately in the early stage, and help prevent other serious complications, together with the ensuing complications such as cardiovascular disease.

2.2 Current medical devices for CKD monitoring

Figure 1 Point Of Care tests [2]

From Diana Smith in Chronic Kidney Disease: A global crisis medical topics, elevated albumin is one of the earliest signs of kidney disease, simple laboratory Point Of Care (POC) tests can detect CKD by measuring albumin which is a type of protein in the urine. Point-of-care testing shows prospects, especially for areas where lacking medical services. The POC test has been successfully used to identify patients at risk by a team that works in a flea market in San Juan, Texas, USA. [3]

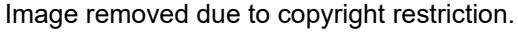


Figure 2 Fully Automated Urine Analyzer AUTION MAX AX-4060[4]

Fully Automated Urine Analyzer AUTION MAX AX-4060 is one of the laboratory testing products from arkray (Singapore). As the sample is drawn through the nozzle and delivered correctly and quantitatively to each pad of the strip, the micro volume samples (minimum 1mL) can be measured easily. Alb, Cre (Alb/Cre ratio, Pro/Cre ratio can be calculated), turbidity and color tone in the urine can be tested by the Urine Analyzer.[4]

2.2.1 CKD monitoring: Detect albumin by the Aggregation-Induced Emission (AIE) bio prober

From Hong's article [6] in quantitation, visualization, and monitoring of conformational transitions of human serum albumin by a tetraphenylethene derivative with aggregation-induced emission (AIE) characteristics (2010). Microalbuminuria being identified as an early sign based on the studies have been done on diabetic nephrosis. Microalbuminuria is commonly diagnosed by elevated protein concentration (30-300 mg/L) in the urine. The human serum albumin (HSA) is a major protein component of blood plasma. Herein, present a readily accessible fluorescent bio probe for HSA detection and quantitation. A non-missive tetraphenylethene derivative is induced to emit by HSA, showing a novel phenomenon of AIE. [5]

- The AIE bioprobe enjoys a broad working range (0-100 nM).
- Low detection limit (down to 1 nM).
- Highly sensitive to albumin.

In their article, they also present figures below, Figure 3 represents under FL intensity of BSPOTPE at 470 nm, BSPOTPE has the highest sensitivity to HSA compare to other different proteins in the urine. Figure 4 shows the relationship between FL intensity at 475 nm and different HSA concentration.[5]

Images removed due to copyright restriction.

Figure 3 Different proteins under FL intensity of BSPOTPE Figure 4 Different HSA concentration under the FL intensity [6]

In summary of their work, they developed a bio probe for HSA detection and quantitation. In the presence of HSA, the BSPOTPE that does not emit light becomes luminescent. The AIE bio probe displays a linear calibration curve of [HSA] 0-100 nM for protein quantification over a wide range of concentrations. It has a low detection limit (down to 1 nM) and a highly selective to albumin. [6]

2.3 Gaps and limitations in the current devices

• Common blood diagnostic and urinalysis processes are conducted in a clinical laboratory, GP or local hospitals.

• Doctors or Professional trained staff are required.

• Time and money required to visit a clinic or hospital.

• Not always accessible as funding not always available for sophisticated analysis equipment, chemical, and facilities.

2.4 Current group work on CKD monitoring device

In the current group work with Tran Tam Anh Pham and Xinyi Zhang, we aim to develop a home based CKD monitoring device, that is, under a stable and uniform stimulating light wavelength from UV LED lights, using camera to capture the testing cuvette with solutions in different HSA concentrations, and FPGA hardware will be used to analyse the levels of fluorescent light and give feedback to patient via user interface. Finally, find the relationship between light intensity and HSA concentrations. The project has demonstrated very encouraging results, the correlation between the fluorescence emitted by the bio-probe and the detected HSA concentration indicates the possible presence of CKD.

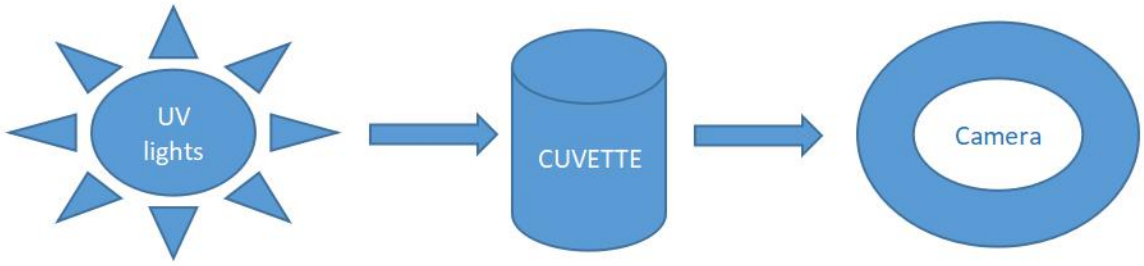


Figure 5 Principle diagram of CKD monitoring device

Testing need to be in the black box environment to remove light contamination from the external environment. Tran Tam Anh Pham developed a Urine tester device that is usable and affordable by 3D printer, the camera holder is firmly attached with the black box, and it firmly fitting the camera's position to secure the image's quality, inside the black box, it has CUVETTE holder and UV light fixing frame. The UV LED he used is small and commercial (3.2V – 20 mA). The light beam angle is 30 degrees. Also use Samsung Mobile Phone Charger: DC output 5.3 V -2.0 A, Micro USB - Type B to provide consistent light supply as Figure 6 shows. [7]

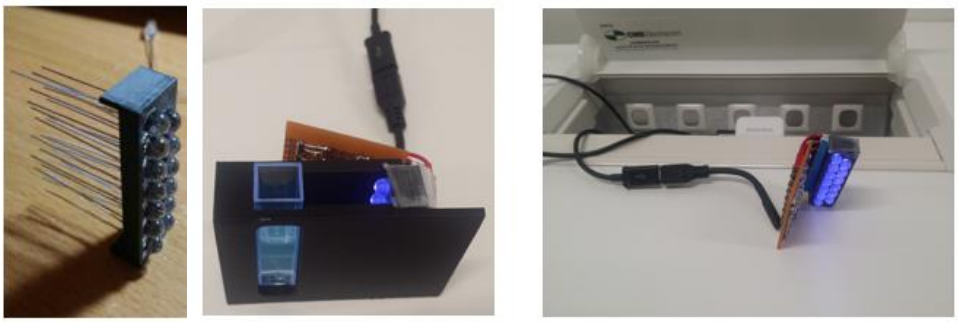


Figure 6 UV lights, CUVETTE holder and Samsung Mobile Phone Charger [7]

From the literature above, early detection of failing kidney function is critical to allow treatment before irreversible damage or other complications occur, but current CKD monitoring devices require the human and economic costs. Therefore, this project proposes the development of a home-based medical device that is user friendly and affordable for patients who can monitor kidney function at home by themselves. AIE bio probe which will absorb the stimulating light and then emit fluorescence for CKD Monitoring. As the advantages of FPGA that state above, this project developed portable medical device based on FPGA hardware, using camera to capture the images of urine and processing by image processing unite on FPGA, and give feedback to the patients via display system. The FPGA based medical device is low cost, efficiently, reliably and deliverable to end-use. The direction of the next chapter is based on the achievement of image processing and the whole system.

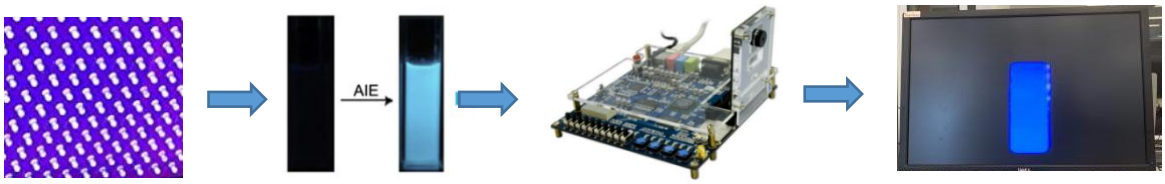


Figure 7 The whole hardware experiment system

2.4.1 Current Practice and Advantages over Existing Technology

• The speed and simplicity of the test allows for more frequent monitoring, as well as earlier detection, to manage deteriorating renal function

• Small and convenient, hand-held devices can be used in the home testing.

• Usable for CKD patient

• Extension of an existing, readily accessible technology

• Readily available for regular health monitoring

• Low cost hardware device and accessible manufacturing technologies of experiment environment: FPGA hardware device and 3D Printing.

• Doctors or Professional trained staff are not required.

2.5 Applications of FPGA in medical engineering

Medical imaging equipment is taking on an increasingly critical role in healthcare as the industry strives to lower patient costs and longer life utility and achieve earlier disease prediction using noninvasive means. Advances in the fusion of diagnostic imaging modalities and their associated algorithm developments are the primary drivers in developing equipment to meet these patient needs. Advanced algorithms require scalable system platforms with significant increases in image-processing performance. [8]

To provide the functionality needed to meet these industry goals, equipment developers are turning to programmable logic devices such as Altera FPGA. In smaller, more accessible, portable equipment Integrated into multicore CPU platforms, Altera FPGA provide the DSP horsepower for the most flexible, highest performance systems. To help accelerate the implementation of sophisticated imaging algorithms onto these platforms, high-level development tools and IP implementation libraries are required. The FPGA has outstanding features such as low cost, optimization, high computational density. [8]

2.5.1 The advantages of FPGA in this project

As FPGA are ideal for image processing applications such as medical imaging. The greater future potential lies in including FPGA on-chip with the main processor, giving the benefit of general-purpose acceleration without the communication bottleneck created by placing the FPGA in a co-processor. At present, applications written directly in Verilog are more efficient. Thus, this project is based on FPGA, the fluorescent emission emerging from the test tube is imaged onto the digital camera TRDB_D5M, processes the image, calculates the concentration, and finally displays the analysis result through a LCD screen as Figure 8 shown below.

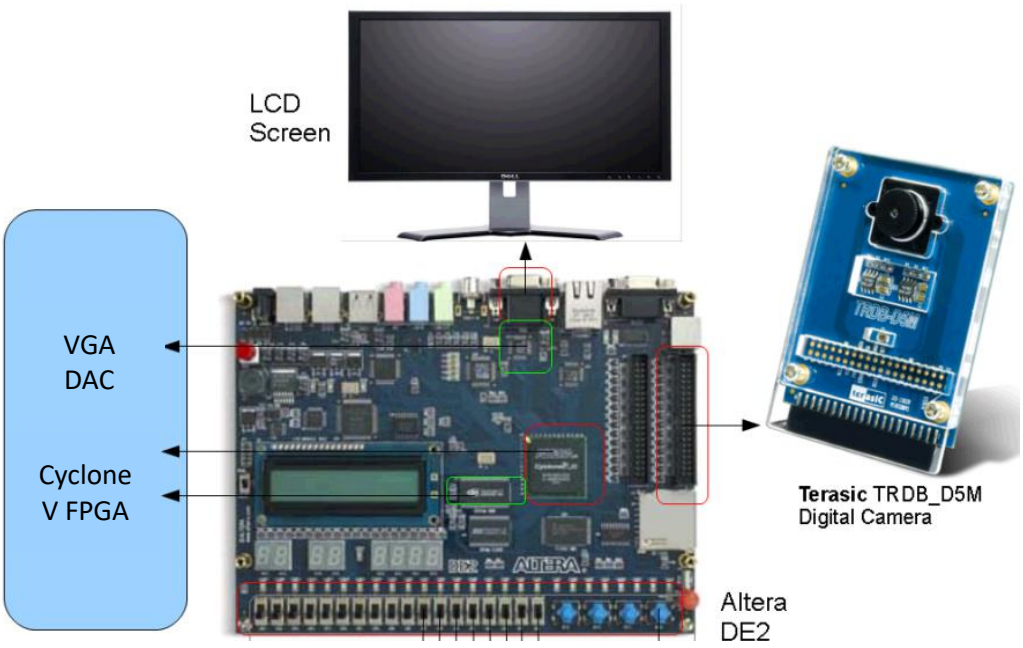


Figure 8 FPGA based medical device [9]

2.5.2 Image processing and analysis

Using camera that based on FPGA to capture the fluorescence light intensity, after image processing unit on FPGA, the albumin concentration in the urine can be presented for patients. As image processing is essential in this project for processing the solutions, the principle and appropriate algorithm can demonstrate first.

There are many cameras use CCD image sensor in combination with a color filter array (CFA). Each pixel needs three color values which are Red, Green and Blue to get a full range color image. Figure 9 shows the processing of transforming raw image data to RGB image data. [10]

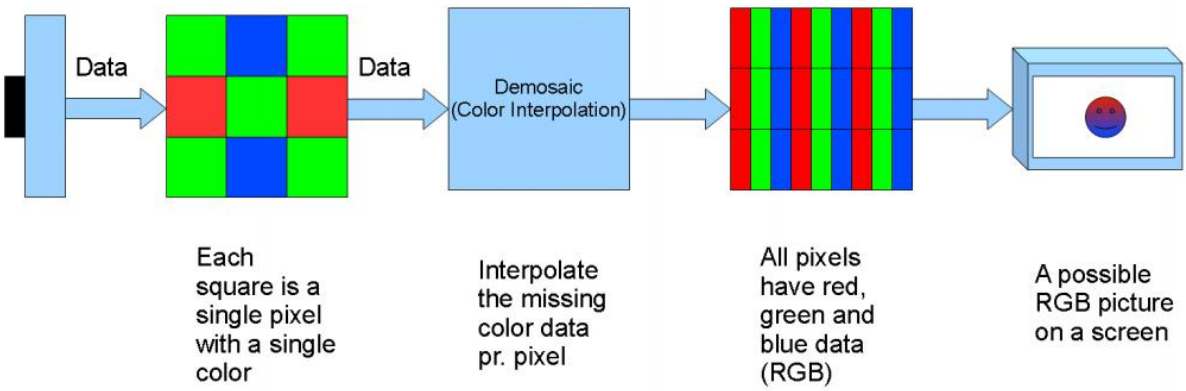


Figure 9 Raw image data to RGB image data [10]

3. Theoretical framework

3.1 Experimental device selection

FGPA can perform any digital device function up to high-performance CPU. Engineers can design a digital system using traditional schematic inputs or hardware description languages such as Verilog HDL. Through software simulation, the correctness of the design can be verified in advance. After PCB (Printed circuit board) is completed, online modification of FGPA can also be used to modify the design at any time without changing the hardware circuit. Using FGPA to develop digital circuits can significantly reduce design time and PCB size and increase system reliability. With the rapid development of FPGA, it has been applied to many fields due to its high flexibility, short development cycle and high parallel computing efficiency. Cyclone series of FPGA are low-cost, low-power products from Altera Company. Cyclone series FPGA have introduced Cyclone/II/III/IV/V series products. For general logic design development, Cyclone V series FPGA is a good choice. Cyclone V of FPGA use an optimized low-power process that extends the low-power advantages of previous generation Cyclone III FPGA, and simplifies the power distribution network, which is very cost-effective. [11]

3.2 Software language

Verilog HDL (Hardware Description Language) is developed on the basis of most widely used C language. It has the characteristics of high flexibility, easy to learn and use. Verilog HDL can be learned in a short period of time and now is an absolute leader in FPGA development/IC design. The Verilog language was originally developed in 1983 by Gateway Design Automation company as a hardware modeling language for its simulator products. It can represent logical circuit diagrams, logical expressions, and logic functions performed by digital logic systems. Digital circuit designers who use this language can describe their design ideas from the top to the bottom and use a series of hierarchical modules to represent extremely complex digital systems. Then use the Electronic Design Automation (EDA) tool to perform simulation verification layer by layer and combine the modules that need to be turned into actual circuits, then convert them to the gate level circuit net-list through the automatic synthesis tool. Last, the dedicated integrated circuit FPGA automatic place and routing tool is used to convert the net-list into a specific circuit structure. [12]

Why needs Verilog?

In FPGA design, there are a variety of design methods, such as schematic design, and writing code. At the beginning, many engineers prefer schematic design, which the input method can intuitively see the circuit structure and understand it quickly. However, as the scale of circuit design increases, the logic circuit design becomes more and more complicated. This has become less satisfied with the actual project needs compare to Verilog language. [12]

The difference between Verilog and C

Verilog is a hardware description language. After compiling and downloading to FPGA, it will generate circuits, so Verilog is all processed and run in parallel; C language is a software language, after compiling and downloading to the microcontroller, it is still software instructions and cannot generate hardware circuits according to the code. Single-chip processing software instruction needs address, decoding, and executing, it is executed serially. The difference between Verilog and C is also the difference between FPGA and MCU/CPU. Because FPGA is processed in parallel, the processing speed is very fast which is the biggest advantage of FPGA and cannot be replaced by MCU.

3.3 Why choose CCD camera and its advantages

To image in ultraviolet light, the camera module needs to have a thicker photon absorption area. This is because the absorption of visible light in silicon in ultraviolet light is deeper. Most CMOS manufacturing processes are tailored for high volume applications that are only imaged in visible light, which are less sensitive to UV imaging. CCD camera, by increasing the substrate thickness (the thickness of epitaxial Epi layer) to increase the UV sensitivity will reduce the ability of image to resolve spatial features. CD with a thicker epitaxial layer can be present in the CCD camera while protecting its ability to resolve fine spatial features. CCD camera used in this experiment, the thickness of the epi is greater than 100 microns, while in most CMOS imagers, the thickness of the epi is 5 to 10 microns.

In addition, the influence of CCD on CCD circuit can be managed more easily than CMOS. CCD cameras designed specifically in ultraviolet light are much more sensitive than CMOS imagers. [13]

3.4 FPGA software development

3.4.1 Quartus software (programming design)

Quartus II software is FPGA development software from Altera company, it can completes FPGA design flow from design input to hardware configuration. Quartus software development interface is as shown in Figure 10.

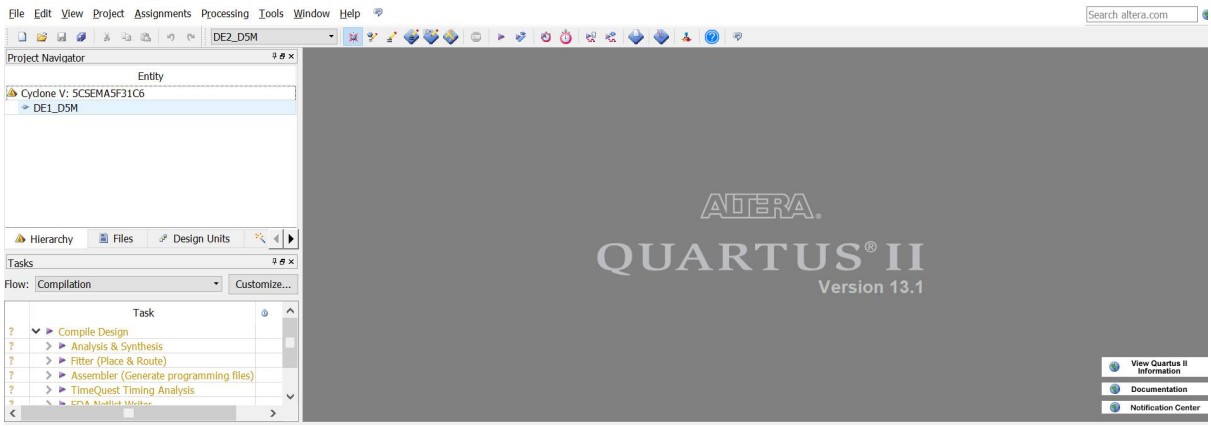


Figure 10 Quartus software development interface

3.4.1.2 Quartus software design flow chart

The design flow of the Quartus software design flow chart in this design is shown in Figure 12.

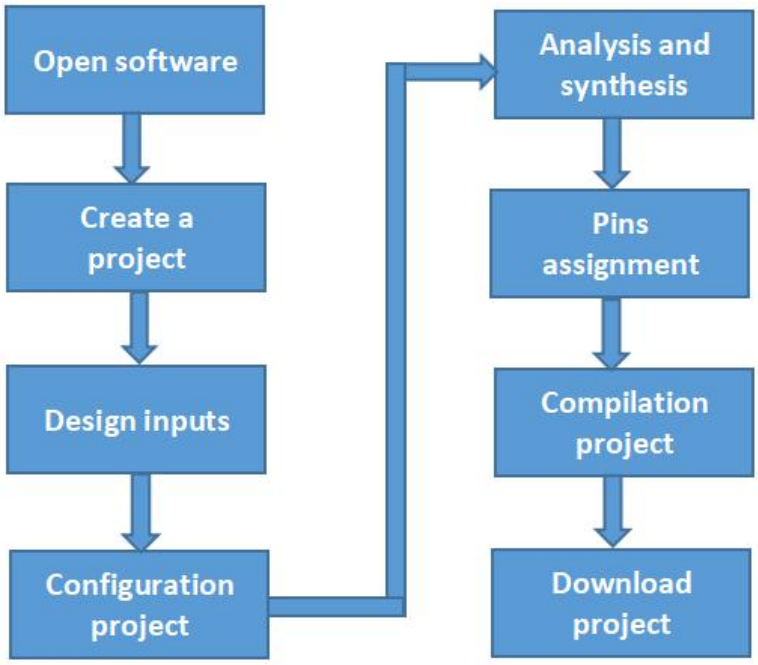


Figure 12 The design flow of the Quartus software

Firstly, open Quartus software and create a new project. After building the project, create a new Verilog top-level file. Then input the designed code to the new Verilog top-level file and configure the project. Next, analyze and synthesize the design file. Meanwhile, Quartus software will check code and will give relevant error warning if code has an error. Otherwise, it will display compile completion. After compiled the project, assign pins to the project. Then, start compiling the entire project. During the compilation process, Quartus software will re-check code, and will generate a sof file for downloading to the FPGA chip if the code and other configuration are correct. Finally, download the compiled sof file to FPGA through the download tool to complete the development process. If there are any problems with any design step, return to the appropriate step to modify or redesign based on the wrong location.

3.4.2 ModelSim software (RTL simulation)

ModelSim from Mentor company is the best language simulator in industry, it is a single-core simulator that supports Verilog simulation. It uses direct optimization of the compilation technology and single core simulation, not only has the fastest compilation and simulation speed, but also compiled code is platform-independent, and easy to protect the IP core. It also provides the

friendliest debugging environment, and has a personalized graphical and user interface, which providing a powerful means for users to speed up debugging. It is the preferred simulation software for FPGA design. As Figure 13 is ModelSim software RTL simulation.

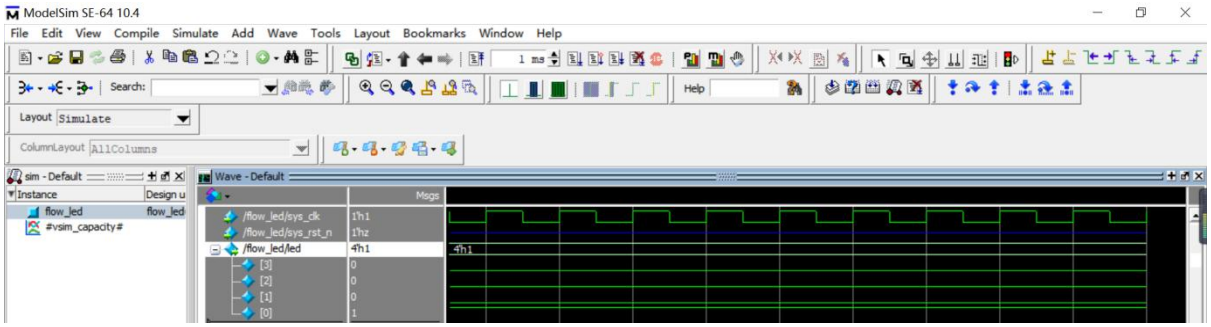


Figure 13 ModelSim software RTL simulation

3.4.3 SignalTap II timing diagram (Timing analysis)

SignalTap II Logic Analyzer (SignalTap II) is the second generation of system-level debugging tools that can capture and display real-time signals. It is a powerful and practical FPGA on-chip debugging tool. SignalTap II can select the signal to be captured and can select triggering method of acquisition and the depth of data acquisition sample. As shown in Figure 14 is SignalTap II software operation interface for this experiment.

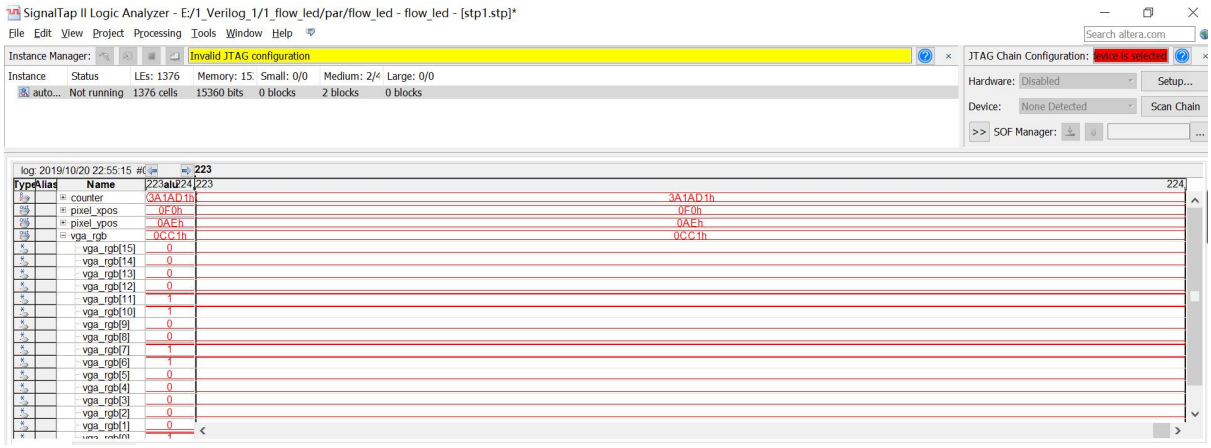


Figure 14 SignalTap II software operation interface

Traditional FPGA board debugging is use external logic analyzer and connected to the control pin of FPGA, and then the internal signal is led out to pin IO for board debugging. The disadvantage of this method is that a logic analyzer is needed, however the logic analyzer is generally expensive, and also

it is cumbersome to choose an external logic analyzer when it comes to test dozens of pins. SignalTap II online logic analyzer overcomes all the shortcomings. It used the traditional logic analyzer concept and most of the functions, implants these functions into the design of FPGA, and stores them in the target device of the board after programming, then use FPGA resources to form an embedded logic analyzer. SignalTap II does not need to lead the signal to be tested to I/O, and does not to have board traces or probes. It is integrated into FPGA development tool Quartus II software from Altera.

3.5 FPGA hardware resources

3.5.1 Hardware interface

JTAG interface

10-pin standard JTAG debug port is on FPGA development board. It can be directly connected to the FPGA down-loader (debugger) for downloading programs or debugging the program online.

GPIO interface

This design used GPIO interface (General-purpose input/output) of FPGA embedded system as the connection interface of the camera module.

VGA interface

VGA interface on FPGA development board can connect to a display interface. FPGA drives VGA display for displaying color bars, images, etc through VGA interface.

FPGA (EPCQ256) Processing unit

This is processing unit of development board EPCQ256. The chip has 10320 logic cells, 414Kbits of embedded memory resources, 23 18×18 embedded multipliers, 2 universal phase-locked loops, 10 global clock networks, 8 user I/O BANK and a maximum of 179 User I/O, which is a cost-effective chip.

3.5.2 Hardware circuit introduction

Clock input: FPGA development board provides clock crystal oscillator circuit as Figure 15 shows:

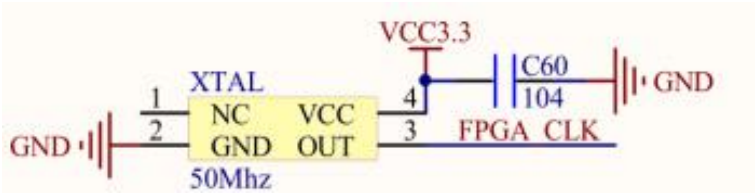


Figure 15 Clock crystal oscillator circuit [14]

VGA interface: FPGA development board has a VGA interface in RGB565 data format. The circuit schematic is shown in Figure 16:

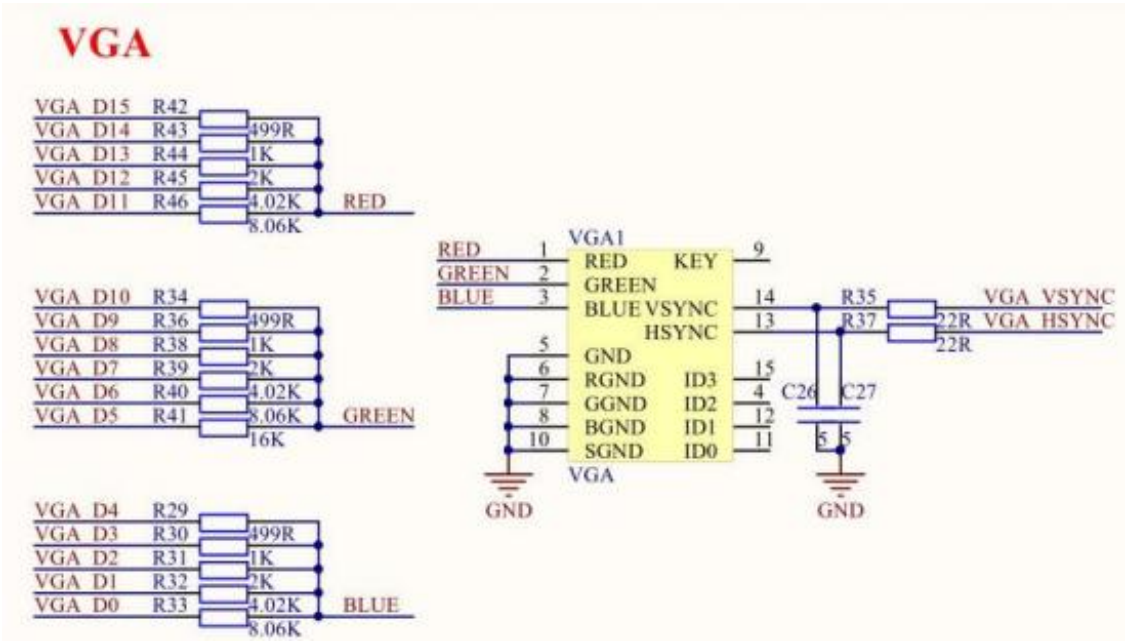


Figure 16 VGA interface in RGB565 data format [14]

Video Graphics Array (VGA) is a video transmission standard for analog signals. VGA interface protocol stipulates the analog voltage range of red, green and blue is 0~0.714V, 0V stands for colorless and 0.714V stands for full color. RGB565 format means red occupies 5 bits of data, green occupies 6 bits of data, and blue occupies 5 bits of data. A total of 65,536 colors can be represented.

FPGA development board of this design uses resistance network to realize the circuit of RGB565 signal to VGA interface three color signal conversion, 5-bit resistance network is used to realize the red signal R, 6-bit resistance network is used to realize the green signal G, 5 bits resistance network is used to realize the blue signal B.

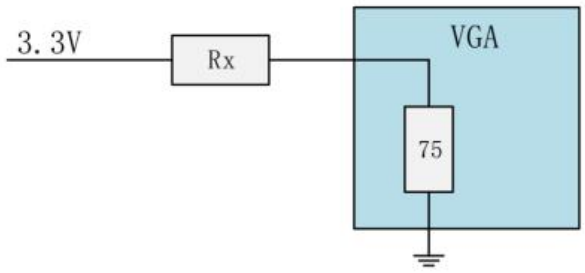


Figure 17 Resistance network of VGA signal conversion

Where Rx is the equivalent resistance of the 5-bit resistor network, when all 5 bits are 1:

$$Rx = R||2R||4R||8R||16R$$

$$3.3 \times \frac{75}{(Rx + 75)} = 0.714$$

The equivalent resistance Rx = 271.6 Ω , R = 526.3 Ω . Considering that all resistors must take the nominal value to reduce the error of the theoretical calculation, let R take 499 Ω , and the following nominal values take 1K Ω , 2K Ω , 4.02K Ω , 8.06K Ω .

FPGA has a camera extension interface to connect TRDB - D5M camera module as Figure 19 shows, the board provides one 40-pin expansion headers. The header connects directly to 36 pins of the Cyclone V SoC FPGA, also provides DC +5V (VCC5), DC +3.3V (VCC3P3).

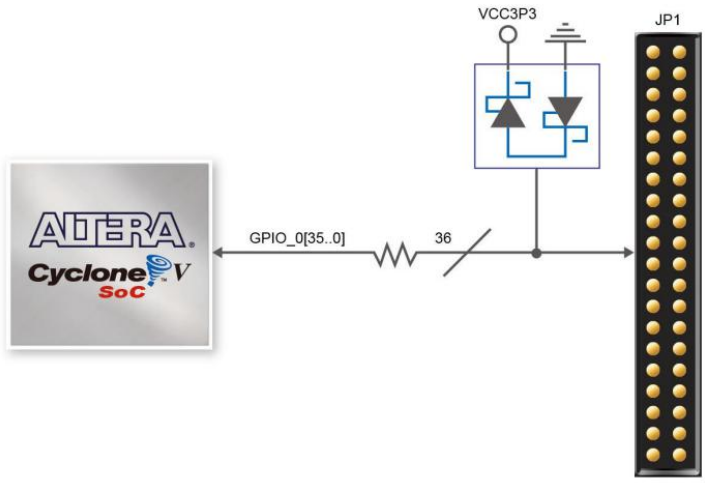


Figure 19 The camera extension interface [14]

IO pin assignment

As shown in Figure 20 is IO pin assignment for clock inputs, which is the interface of I/O of the core chip EPCQ256 and 50Mhz of the clock module.

Signal Name	FPGA Pin No.	Description	I/O Standard
CLOCK_50	PIN_AF14	50 MHz clock input	3.3V

Figure 20 pin assignment for clock inputs [14]

As shown in Figure 21 is the IO pin assignment for VGA, which is the I/O of core chip EPCQ256 and VGA interface.

Signal Name	FPGA Pin No.	Description	I/O Standard
VGA_R[0]	PIN_A13	VGA Red[0]	3.3V
VGA_R[1]	PIN_C13	VGA Red[1]	3.3V
VGA_R[2]	PIN_E13	VGA Red[2]	3.3V
VGA_R[3]	PIN_B12	VGA Red[3]	3.3V
VGA_R[4]	PIN_C12	VGA Red[4]	3.3V
VGA_R[5]	PIN_D12	VGA Red[5]	3.3V
VGA_R[6]	PIN_E12	VGA Red[6]	3.3V
VGA_R[7]	PIN_F13	VGA Red[7]	3.3V
VGA_G[0]	PIN_J9	VGA Green[0]	3.3V
VGA_G[1]	PIN_J10	VGA Green[1]	3.3V
VGA_G[2]	PIN_H12	VGA Green[2]	3.3V
VGA_G[3]	PIN_G10	VGA Green[3]	3.3V
VGA_G[4]	PIN_G11	VGA Green[4]	3.3V
VGA_G[5]	PIN_G12	VGA Green[5]	3.3V
VGA_G[6]	PIN_F11	VGA Green[6]	3.3V
VGA_G[7]	PIN_E11	VGA Green[7]	3.3V
VGA_B[0]	PIN_B13	VGA Blue[0]	3.3V
VGA_B[1]	PIN_G13	VGA Blue[1]	3.3V
VGA_B[2]	PIN_H13	VGA Blue[2]	3.3V
VGA_B[3]	PIN_F14	VGA Blue[3]	3.3V
VGA_B[4]	PIN_H14	VGA Blue[4]	3.3V
VGA_B[5]	PIN_F15	VGA Blue[5]	3.3V
VGA_B[6]	PIN_G15	VGA Blue[6]	3.3V
VGA_B[7]	PIN_J14	VGA Blue[7]	3.3V
VGA_CLK	PIN_A11	VGA Clock	3.3V
VGA_BLANK_N	PIN_F10	VGA BLANK	3.3V
VGA_HS	PIN_B11	VGA H_SYNC	3.3V
VGA_VS	PIN_D11	VGA V_SYNC	3.3V
VGA_SYNC_N	PIN_C10	VGA SYNC	3.3V

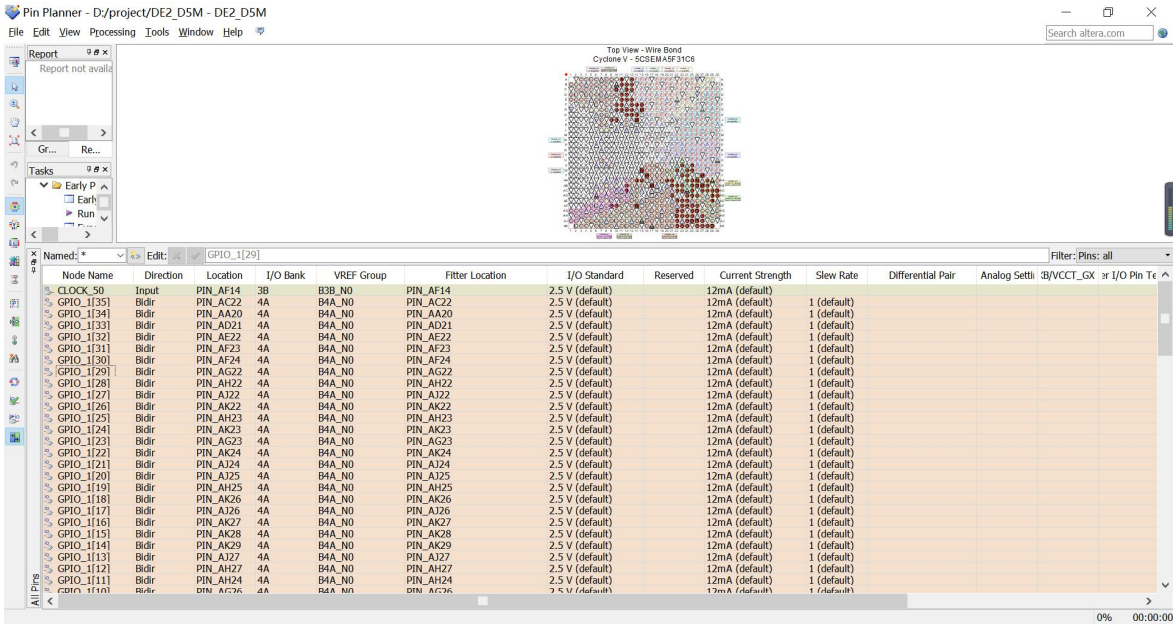
Figure 21 Pin assignment for VGA [14]

As shown in Figure 22 is the IO pin assignment for camera module, which is the interface between the I/O of the core chip EPCQ256 and camera module.

GPIO_1[0]	PIN_AB17	GPIO Connection 1[0]	3.3V
GPIO_1[1]	PIN_AA21	GPIO Connection 1[1]	3.3V
GPIO_1 [2]	PIN_AB21	GPIO Connection 1[2]	3.3V
GPIO_1 [3]	PIN_AC23	GPIO Connection 1[3]	3.3V
GPIO_1 [4]	PIN_AD24	GPIO Connection 1[4]	3.3V
GPIO_1 [5]	PIN_AE23	GPIO Connection 1[5]	3.3V
GPIO_1 [6]	PIN_AE24	GPIO Connection 1[6]	3.3V
GPIO_1 [7]	PIN_AF25	GPIO Connection 1[7]	3.3V
GPIO_1 [8]	PIN_AF26	GPIO Connection 1[8]	3.3V
GPIO_1 [9]	PIN_AG25	GPIO Connection 1[9]	3.3V
GPIO_1[10]	PIN_AG26	GPIO Connection 1[10]	3.3V
GPIO_1 [11]	PIN_AH24	GPIO Connection 1[11]	3.3V
GPIO_1 [12]	PIN_AH27	GPIO Connection 1[12]	3.3V
GPIO_1 [13]	PIN_AJ27	GPIO Connection 1[13]	3.3V
GPIO_1 [14]	PIN_AK29	GPIO Connection 1[14]	3.3V
GPIO_1 [15]	PIN_AK28	GPIO Connection 1[15]	3.3V
GPIO_1 [16]	PIN_AK27	GPIO Connection 1[16]	3.3V
GPIO_1 [17]	PIN_AJ26	GPIO Connection 1[17]	3.3V
GPIO_1 [18]	PIN_AK26	GPIO Connection 1[18]	3.3V
GPIO_1 [19]	PIN_AH25	GPIO Connection 1[19]	3.3V
GPIO_1 [20]	PIN_AJ25	GPIO Connection 1[20]	3.3V
GPIO_1 [21]	PIN_AJ24	GPIO Connection 1[21]	3.3V
GPIO_1 [22]	PIN_AK24	GPIO Connection 1[22]	3.3V
GPIO_1 [23]	PIN_AG23	GPIO Connection 1[23]	3.3V
GPIO_1 [24]	PIN_AK23	GPIO Connection 1[24]	3.3V
GPIO_1 [25]	PIN_AH23	GPIO Connection 1[25]	3.3V
GPIO_1 [26]	PIN_AK22	GPIO Connection 1[26]	3.3V
GPIO_1 [27]	PIN_AJ22	GPIO Connection 1[27]	3.3V
GPIO_1 [28]	PIN_AH22	GPIO Connection 1[28]	3.3V
GPIO_1 [29]	PIN_AG22	GPIO Connection 1[29]	3.3V
GPIO_1 [30]	PIN_AF24	GPIO Connection 1[30]	3.3V
GPIO_1 [31]	PIN_AF23	GPIO Connection 1[31]	3.3V
GPIO_1 [32]	PIN_AE22	GPIO Connection 1[32]	3.3V
GPIO_1 [33]	PIN_AD21	GPIO Connection 1[33]	3.3V
GPIO_1 [34]	PIN_AA20	GPIO Connection 1[34]	3.3V
GPIO_1 [35]	PIN_AC22	GPIO Connection 1[35]	3.3V

Figure 22 pin assignment for camera module [14]

After determining that all external circuits are connected to FPGA pins, the FPGA pin selection needs to be done according to the connection number of the external circuit as shown in Figure 23. Select pin selection in the Quartus II software to ensure that all hardware connections have corresponding pin serial number.



Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength	Slew Rate	Differential Pair	Analog Settli	:B/VCCT_GX	:r I/O Pin Te
CLOCK_50	Input	PIN_AF14	3B	B3B_N0	PIN_AF14	2.5 V (default)		12mA (default)					
GPIO_1[35]	Bidir	PIN_AC22	4A	B4A_N0	PIN_AC22	2.5 V (default)		12mA (default)	1 (default)				
GPIO_1[34]	Bidir	PIN_AA20	4A	B4A_N0	PIN_AA20	2.5 V (default)		12mA (default)	1 (default)				
GPIO_1[33]	Bidir	PIN_AD21	4A	B4A_N0	PIN_AD21	2.5 V (default)		12mA (default)	1 (default)				
GPIO_1[32]	Bidir	PIN_AE22	4A	B4A_N0	PIN_AE22	2.5 V (default)		12mA (default)	1 (default)				
GPIO_1[31]	Bidir	PIN_AF23	4A	B4A_N0	PIN_AF23	2.5 V (default)		12mA (default)	1 (default)				
GPIO_1[30]	Bidir	PIN_AF24	4A	B4A_N0	PIN_AF24	2.5 V (default)		12mA (default)	1 (default)				
GPIO_1[29]	Bidir	PIN_AG22	4A	B4A_N0	PIN_AG22	2.5 V (default)		12mA (default)	1 (default)				
GPIO_1[28]	Bidir	PIN_AH22	4A	B4A_N0	PIN_AH22	2.5 V (default)		12mA (default)	1 (default)				
GPIO_1[27]	Bidir	PIN_AJ22	4A	B4A_N0	PIN_AJ22	2.5 V (default)		12mA (default)	1 (default)				
GPIO_1[26]	Bidir	PIN_AK22	4A	B4A_N0	PIN_AK22	2.5 V (default)		12mA (default)	1 (default)				
GPIO_1[25]	Bidir	PIN_AH23	4A	B4A_N0	PIN_AH23	2.5 V (default)		12mA (default)	1 (default)				
GPIO_1[24]	Bidir	PIN_AK23	4A	B4A_N0	PIN_AK23	2.5 V (default)		12mA (default)	1 (default)				
GPIO_1[23]	Bidir	PIN_AG23	4A	B4A_N0	PIN_AG23	2.5 V (default)		12mA (default)	1 (default)				
GPIO_1[22]	Bidir	PIN_AK24	4A	B4A_N0	PIN_AK24	2.5 V (default)		12mA (default)	1 (default)				
GPIO_1[21]	Bidir	PIN_AJ24	4A	B4A_N0	PIN_AJ24	2.5 V (default)		12mA (default)	1 (default)				
GPIO_1[20]	Bidir	PIN_AJ25	4A	B4A_N0	PIN_AJ25	2.5 V (default)		12mA (default)	1 (default)				
GPIO_1[19]	Bidir	PIN_AH25	4A	B4A_N0	PIN_AH25	2.5 V (default)		12mA (default)	1 (default)				
GPIO_1[18]	Bidir	PIN_AK26	4A	B4A_N0	PIN_AK26	2.5 V (default)		12mA (default)	1 (default)				
GPIO_1[17]	Bidir	PIN_AJ26	4A	B4A_N0	PIN_AJ26	2.5 V (default)		12mA (default)	1 (default)				
GPIO_1[16]	Bidir	PIN_AK27	4A	B4A_N0	PIN_AK27	2.5 V (default)		12mA (default)	1 (default)				
GPIO_1[15]	Bidir	PIN_AK28	4A	B4A_N0	PIN_AK28	2.5 V (default)		12mA (default)	1 (default)				
GPIO_1[14]	Bidir	PIN_AK29	4A	B4A_N0	PIN_AK29	2.5 V (default)		12mA (default)	1 (default)				
GPIO_1[13]	Bidir	PIN_AJ27	4A	B4A_N0	PIN_AJ27	2.5 V (default)		12mA (default)	1 (default)				
GPIO_1[12]	Bidir	PIN_AH27	4A	B4A_N0	PIN_AH27	2.5 V (default)		12mA (default)	1 (default)				
GPIO_1[11]	Bidir	PIN_AH24	4A	B4A_N0	PIN_AH24	2.5 V (default)		12mA (default)	1 (default)				
GPIO_1[10]	Bidir	PIN_AG26	4A	B4A_N0	PIN_AG26	2.5 V (default)		12mA (default)	1 (default)				

Figure 23 The connection number of the external circuit.

3.6 The structure of this experiment design (Top-down modular design)

Modular design can make simulation test of a large design more easier, and can make code maintenance or upgrade more convenient. When a sub-module is modified, the result of other modules will not be affected. The ultimate goal of modular, standardized design is to increase the versatility of the design and reduce the amount of work cause by the same function design and verification in different projects. The basic principle of partitioning modules is that the sub-module functions are relatively independent, the internal connections of the modules are as close as possible, and the connections between the modules are as simple as possible.

In the modular design, for a complex image processing system, this project used a top-down design which can divide the system into several functional modules. Each function module is subdivided into sub-modules of the next layer, each module is designed as a Verilog program file. Therefore, for the top-level module of a system, use a structured design, which top-level module can call each functional module separately. The following Figure 24 is the functional block diagram of this project modular design. The top-level module is only used to call other modules and not for logic. There are module A, module B, module C, module D below top-level.

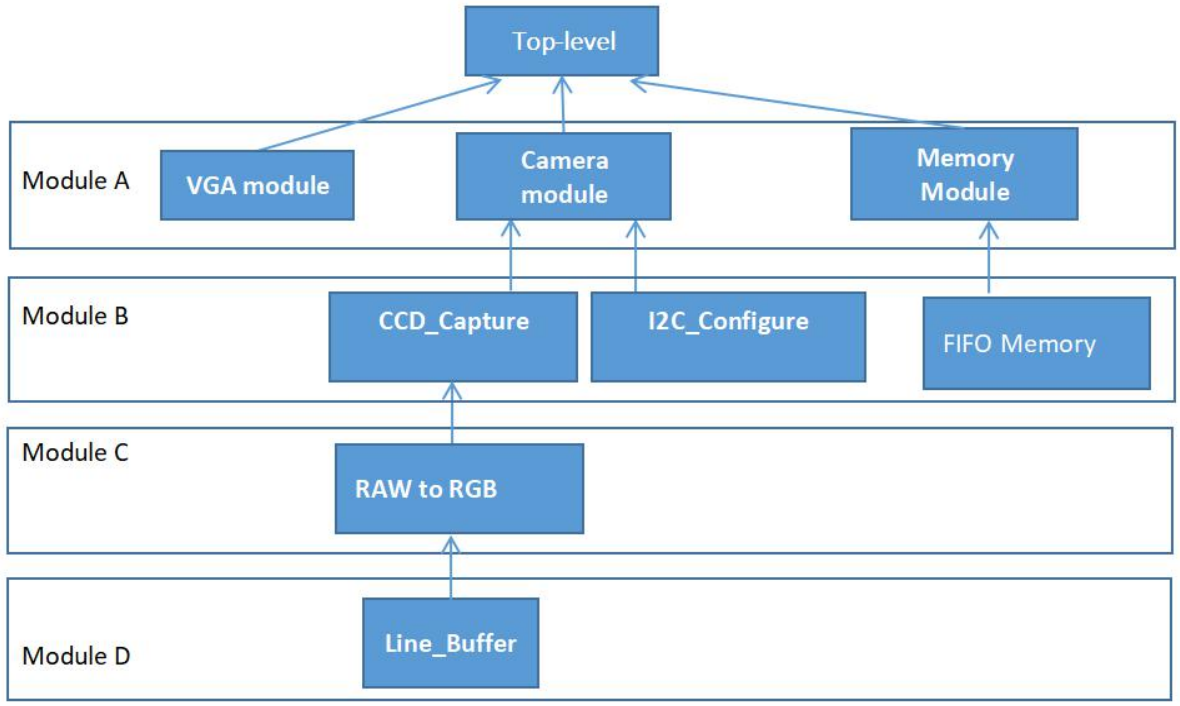


Figure 24 The functional block diagram of this project modular design.

3.7 FPGA programming design

The main steps of FPGA design flow generally include design inputs, RTL simulation, design, layout and routing, timing simulation, timing analysis, and system verification, as shown in Figure 25. If there are any problems with any simulation or verification steps, then will need to return to the corresponding step to modify or redesign based on the wrong location. RTL simulation is in ModelSim software, timing simulation is in SignalTap II software. And the rest of the steps are in Quartus.

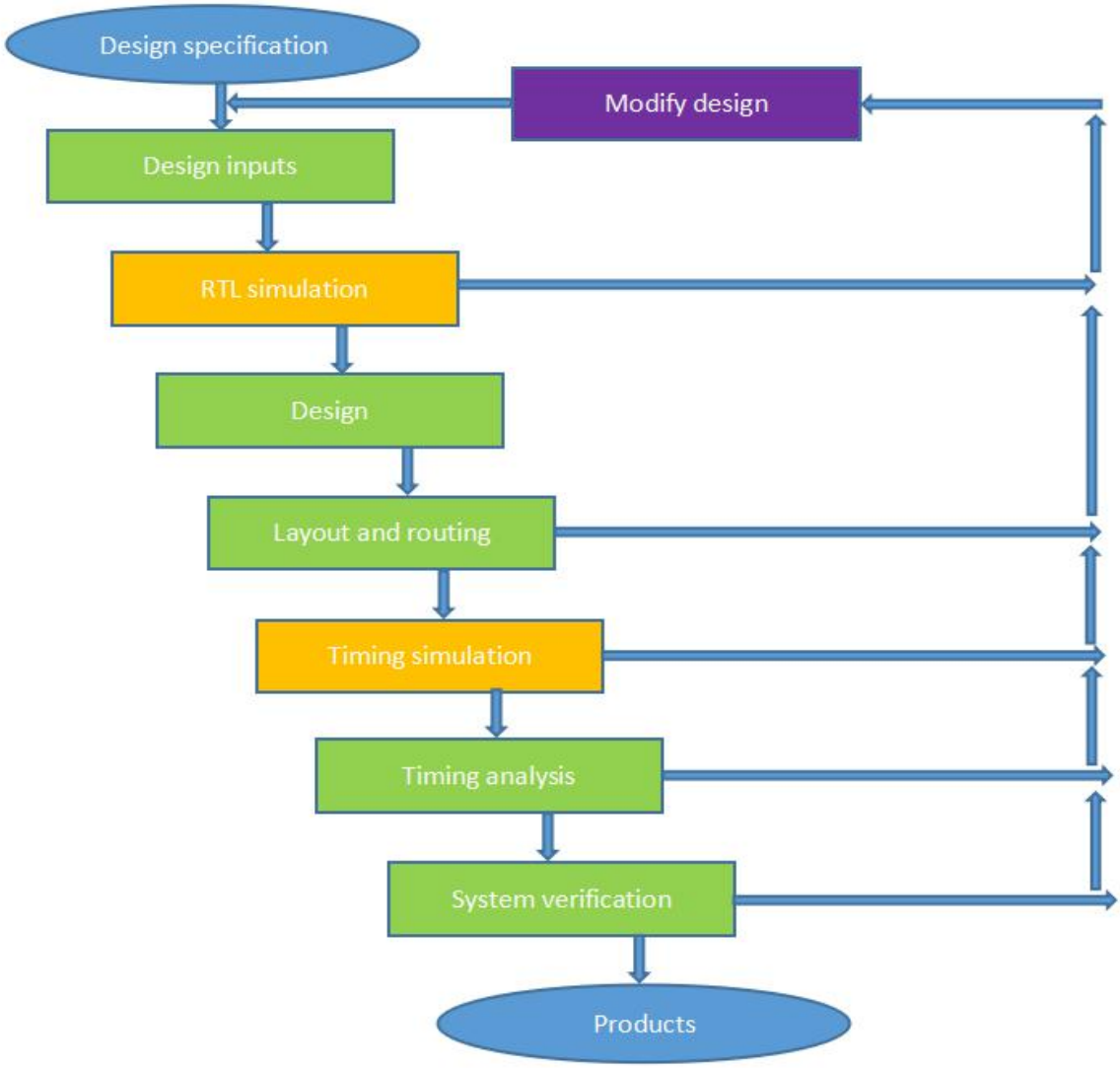


Figure 25 The main steps of FPGA design flow

3.7.1 Verilog hardware description language design

HDL language used in this design is Verilog HDL. It is top-down design, which is conducive to the module division and reuse. It has good portability and high versatility. The design does not need to change with different process and structure of the chip, which is more conducive to the transplantation of programs.

3.7.2 ModelSim software simulation and verification

After circuit design, use simulation tool to perform RTL simulation (functional simulation) to verify whether the circuit function meets the design requirements. Functional simulation is sometimes

referred as pre-simulation. The simulation tool used is ModelSim from ModelTech. Errors in the design can be found in time through simulation, which will increase the design progress and reliability.

3.7.3 I/O pin layout and routing

The synthesize results is a logical network consisting of basic logic units such as AND, OR, NOT, triggers, which is still not the actual configuration of the chip. Now use the software tools (Quarts) provided by FPGA to adapt the logical network to the current FPGA device according to the model of the selected chip. This process is called layout and routing.

3.7.4 SignalTap II Software timing simulation

In order to ensure the reliability of the design, some verification is required after the timing simulation. This design uses the Quartus embedded timing analysis tool to perform static timing analysis (STA, StaticTimingAnalyzer).

3.7.5 System verification

This design uses SignalTap II embedded in Quartus II software for online logic analysis. SignalTap II is a FPGA on-chip signal analysis tool. The main function is to read the internal signals of FPGA online and in real time through JTAG port. The basic principle is to use the unused Block RAM in FPGA to save the signal to these Block RAM in real time according to the trigger conditions set by the user, then transfer them to computer through JTAG port, finally display timing waveform on computer screen.

4. Programming design

4.1 Overall development process of FPGA image processing system

The design is divided into three major parts, including PLL design, VGA display module design and camera module design. After each module is designed, it needs to perform simulation verification of ModelSim and SignalTap II to determine the program executes the set logic, and then design the next module. PLL design mainly includes clock control module and memory first-in first-out module. VGA design mainly includes VGA display and drive module. Camera design mainly includes I2C camera drive module and camera acquisition module. The clock module of PLL design is used in VGA module, and clock module of PLL design and memory first in first out memory module are used in camera module as Figure 26 shows.

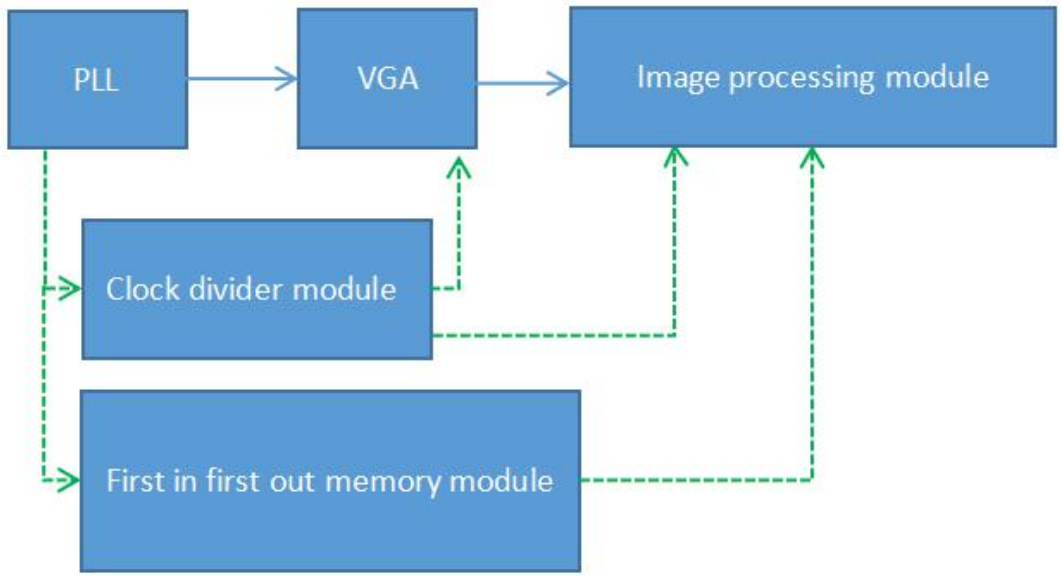


Figure 26 Overall development process of FPGA image processing system

4.2 Design of phase-locked loop feedback control circuit

Phase Locked Loop (PLL) is a feedback control circuit. PLL provides system clock management and offset control for clock network, it has functions of clock multiplication, frequency division, phase offset, and programmable duty cycle. For a simple design, the entire system of FPGA can use a clock or divide the clock by writing code. However, for a more complicated system, multiple clocks and clocks phase offset are often used in the system, and clock multiplication cannot be achieved by

writing code of clock output. Therefore, it is very important and effective to control the system clock by using Altera PLL IP core.

Some functional blocks are commonly used in digital circuits, but are more complicated, such as clock modules and memory management modules are designed to modify parameters by IP core.

As FPGA become larger and more complex (the complexity of IC increases at a rate of 55% per year, while design capabilities increase by only 21% per year), the main task of the designer is to complete complex designs in time. Calling IP cores can avoid duplication of work and greatly reduce the burden on engineers. Therefore, the use of IP cores is a development trend, and reuse of IP cores greatly shortens the time to the market. The modules that need PLL in this design is clock divider module and FIFO read/write module as shown in Figure 27.

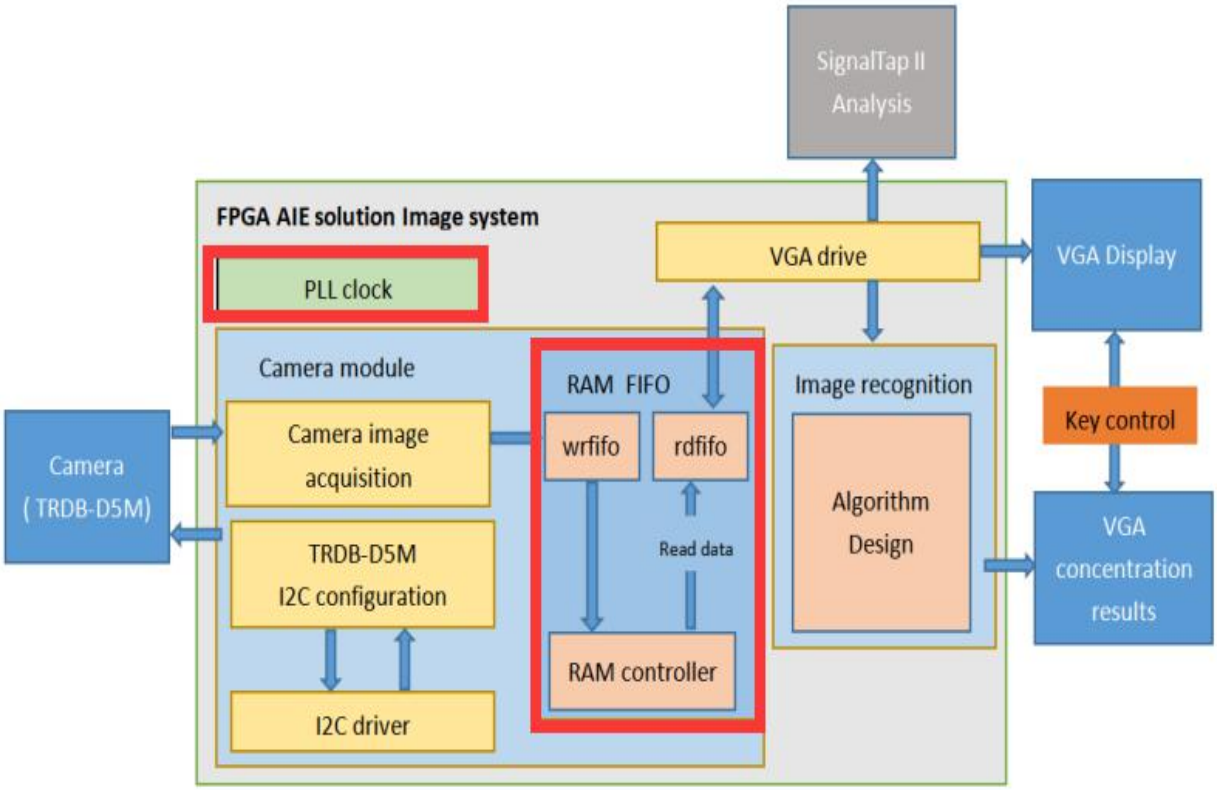


Figure 27 The modules that need PLL in this design

4.2.1 PLL feedback control module

4.2.1.1 Clock PLL configuration and design

As the frequency of the clock signal used by camera module, VGA display module and FIFO memory module is different in this design, it is necessary to design PLL for clock division processing. Set clock

frequency of image acquisition module of camera to 60Mhz, set read and written frequency of FIFO memory module to 50Mhz, and set scanning frequency of VGA display module to 25Mhz.

As shown in Figure 28 is a schematic diagram of FPGA system clock configuration using PLL. Set clock frequency to 100Mhz in the Requested Setting. c2 clock is set to 50MHz and c3 clock is set to 25MHz. Which means the input clock is connected to image acquisition module of camera, c2 is connected to FIFO read/write module, and c3 is connected to VGA display module.

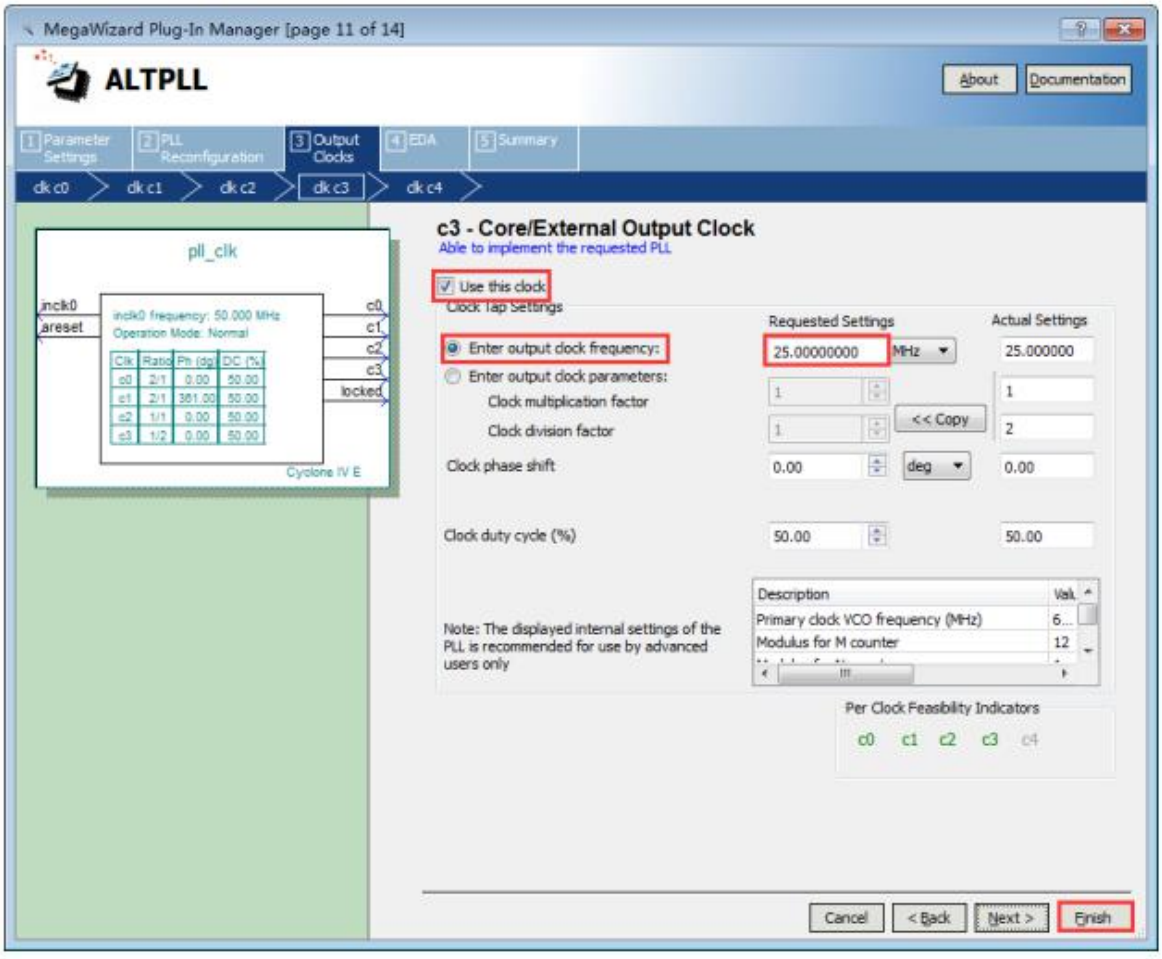


Figure 28 FPGA system clock configuration using PLL

4.2.1.2 ModelSim software simulation and verification

The waveform of clock division module from ModelSim simulation is shown in Figure 29.

After locked signal is pulled high, PLL outputs four stable clocks. clk_100m period is 10000ps (10000 ps=10 ns), which means clock frequency is 100Mhz. clk_50m period is 20000 ps (20000 ps=20 ns),

which means clock frequency is 50Mhz. clk_25m period is 40,000 ps (40000 ps=40 ns), which means clock frequency is 25 MHz. From the simulation results, PLL is designed correctly.

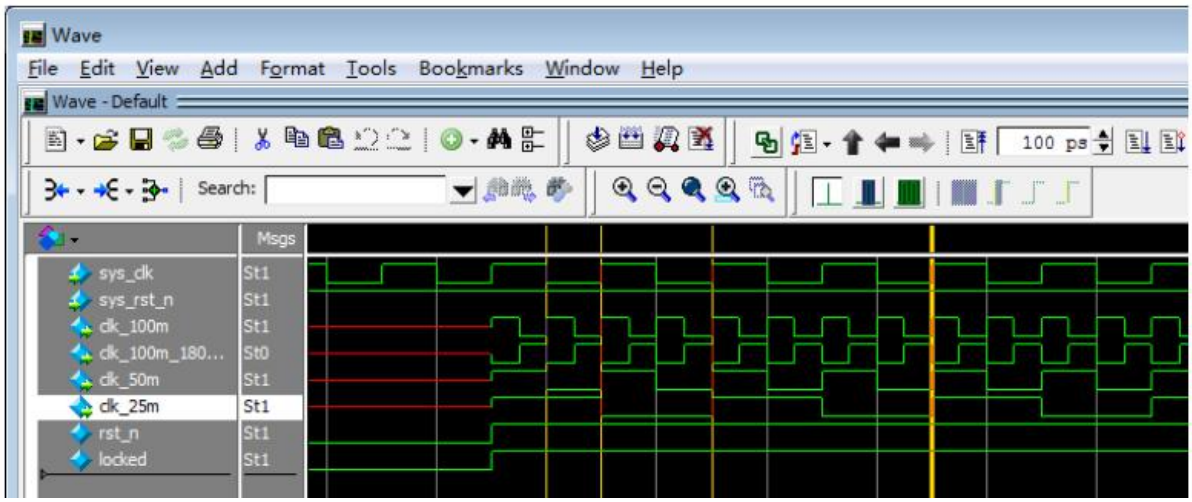


Figure 29 The waveform of clock division module from ModelSim simulation

4.2.1.2 Simulation and verification from oscilloscope

As shown in Figure 30 is the waveform of clock divider sampled from oscilloscope. Connect oscilloscope to the GND pin of FPGA board, and then place the other probe on the output pin of the clock division. The waveform of the clock can be observed, the clock frequency measured by oscilloscope is25Mhz, which is the same as the simulation result.

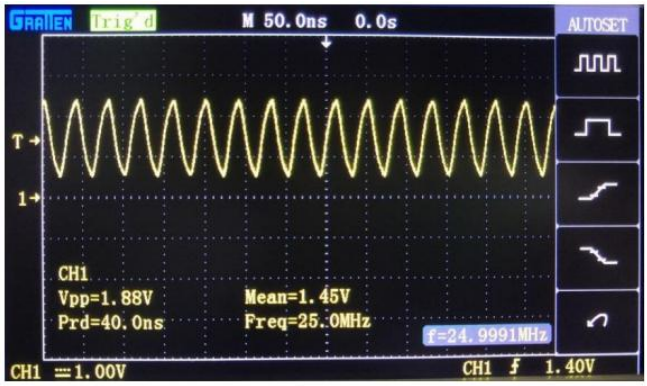


Figure 30 The waveform of clock divider from the oscilloscope.

4.2.2 FIFO memory read and write module

First In First Out (FIFO) used by FPGA generally refers to a buffer with first-in first-out characteristics for data storage. This experiment is used for buffering image data, which is the interaction between image acquisition data and image display data. It is simple and convenient to use as it is writing and reading data sequentially. FIFO module used in this experiment is shown in Figure 31. For a single

clock FIFO, it has a separate clock port: clock, so all the input and output signals are synchronized to the clock signal. The width is 8 bytes which is consistent with the number of output pixels of image acquisition module. The depth of the FIFO is 256.

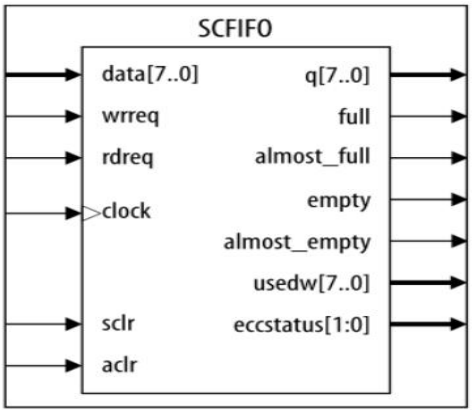


Figure 31 FIFO memory read and write module

According to the experimental requirements and the idea of modular design, the following four modules are designed: fifo module, writing fifo module, reading fifo module and top-level module to achieve the signal interaction of the first three modules. As Figure 32 shows.

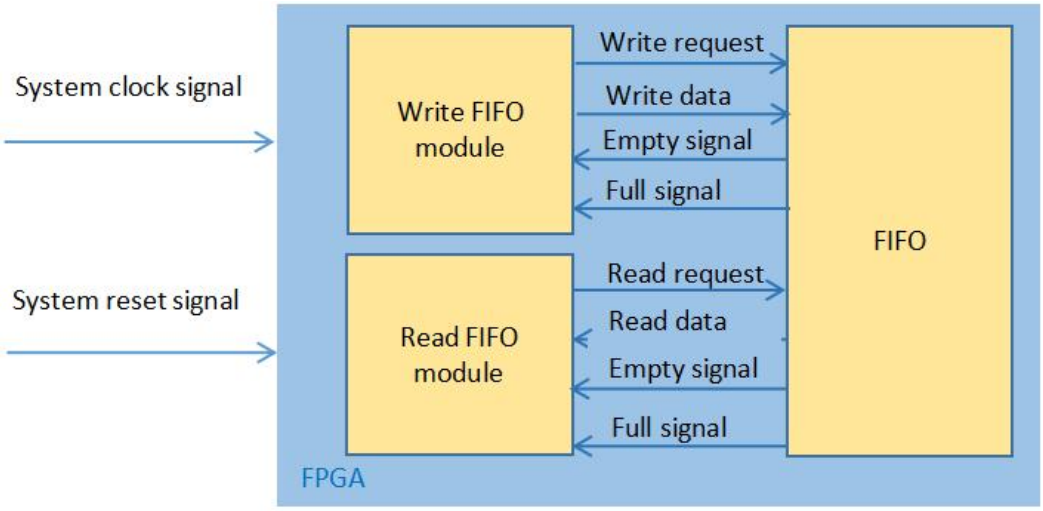


Figure 32 Signal interaction of fifo module, writing fifo module, and reading fifo module.

4.2.2.1 FIFO memory read and write module

PLL configuration and design

Configured FIFO module by using IP core as Figure 33 shown below. The bit width is 8bits, the depth of FIFO is 256 words which is the number of specified bit width can be stored. After setting, FIFO capacity is 256 8bits.

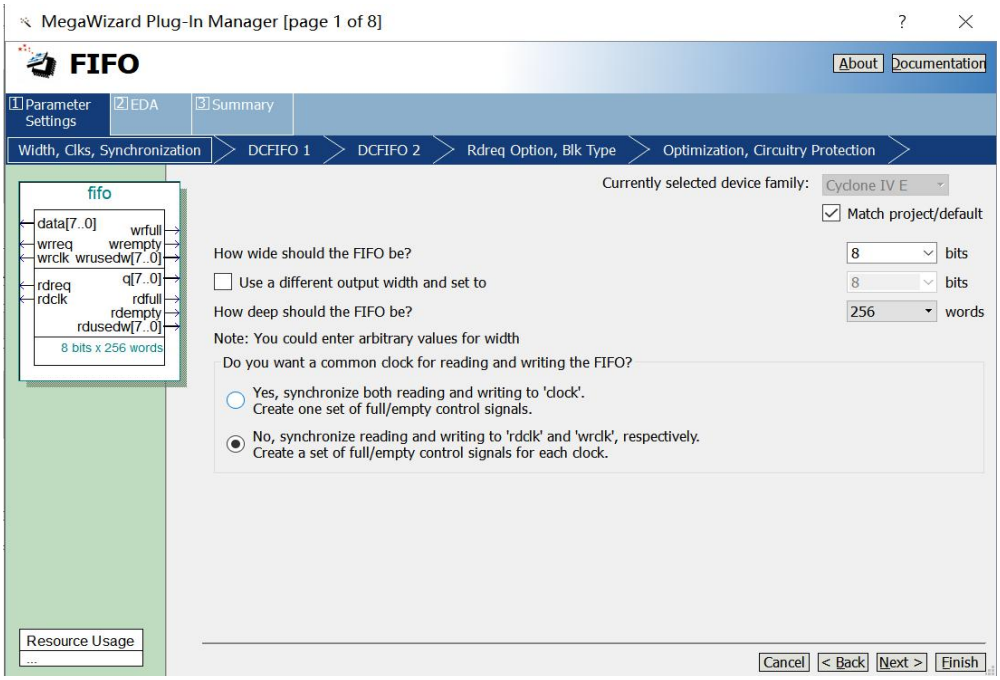


Figure 33 Configured the FIFO module by using the IP core

4.2.2.2 Top-level module connection diagram

FIFO read/write module instantiates fifo module, write FIFO module (wr_fifo), and read FIFO module (rd_fifo). The signal connection diagram of each module is shown in Figure 34 below.

Write empty signal (wrempty) and write full signal (wrfull) output by FIFO module are connected to write FIFO module (fifo_wr), and when write FIFO module detects that write empty signal (wrempty) is pulled high, write request signal (wrreq) is sent to FIFO module and the data is written. When write full signal (wrfull) is detected to be high, data writing to FIFO module is stopped. Read empty signal (rdempty) and read full signal (rdfull) output by FIFO module are connected to read FIFO module (fifo_rd). When read FIFO module detects that read full signal (rdfull) is pulled high, read request signal (rdreq) is sent to FIFO module and read from FIFO module. Stop reading data from FIFO module when read empty signal (rdempty) is pulled high.

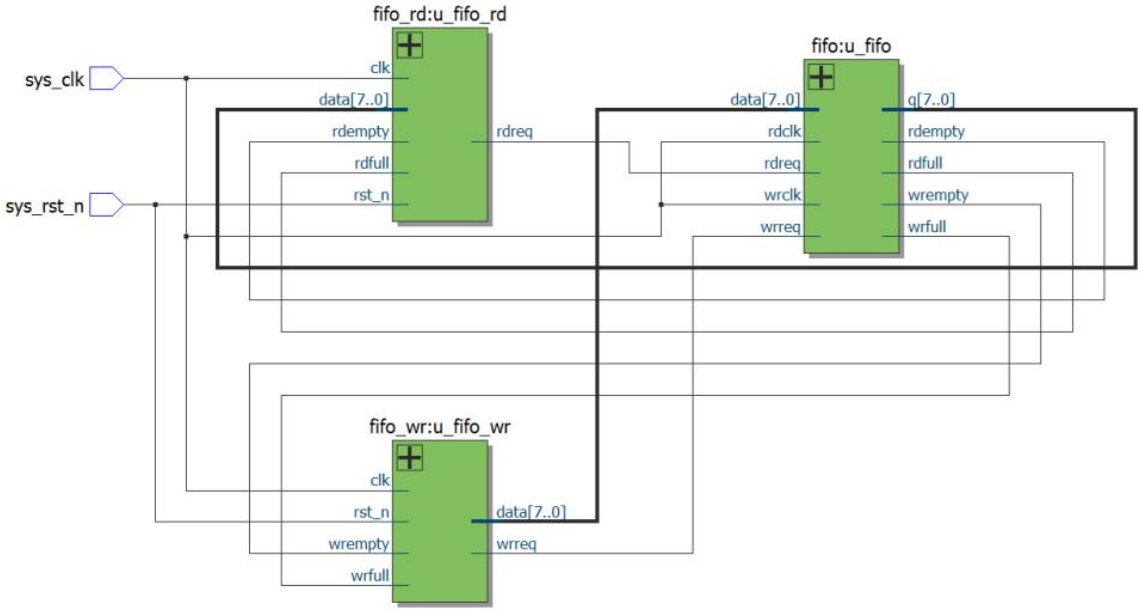


Figure 34 Top-level module connection diagram

4.2.2.3 Modelsim software simulation and verification

It can be seen from Figure 35 that read full signal (rdfull) is valid after write full signal (wrfull) is pulled high for 2 clock cycles, and write full signal (wrfull) is pulled low after read request signal (rereq) is pulled high for third clock cycle.

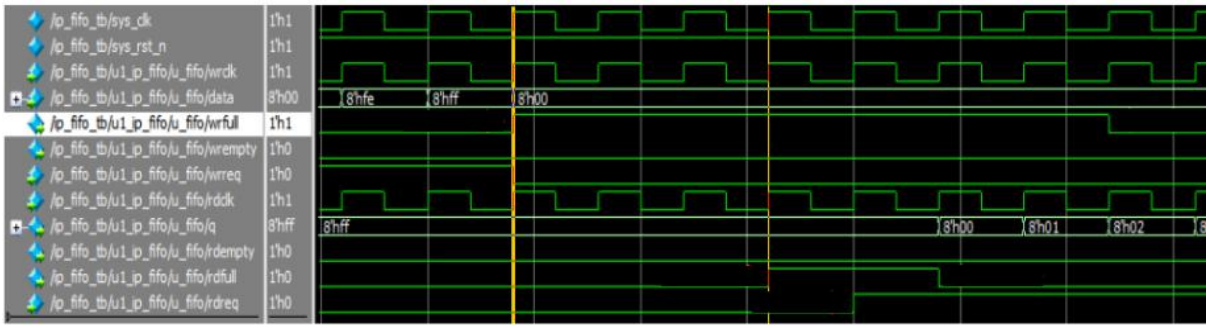


Figure 35 The waveform of the FIFO module from Modelsim simulation

4.2.2.4 SignalTap II software simulation and verification

Use SignalTap II software to debug FIFO IP core, firstly create a SignalTap II debug file in Quartus II software, add eight signals which are wrempty, wrfull, wrreq, data, rdreq, rdempty, rdfull, and q to SignalTap II debug file. The following Figure 36 shows the waveform of FIFO acquired empty by SignalTap II software.

It can be seen that when reading empty FIFO, read empty signal (rdempty) is first pulled high, and after two clock cycles, write empty signal (wrempty) is pulled high, which is determined by the

internal structure of FIFO, after four clock cycles of write request signal (wrreq) is pulled high, read empty signal (rdempty) is pulled low.

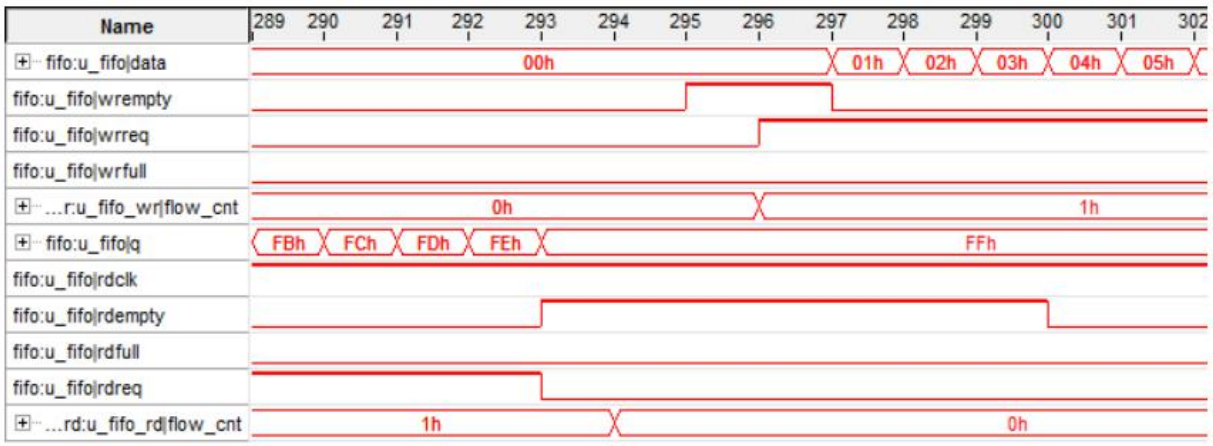


Figure 36 The waveform of FIFO acquired empty by SignalTap II software

4.3 VGA display module

VGA driver module and VGA display module are as shown in Figure 37.

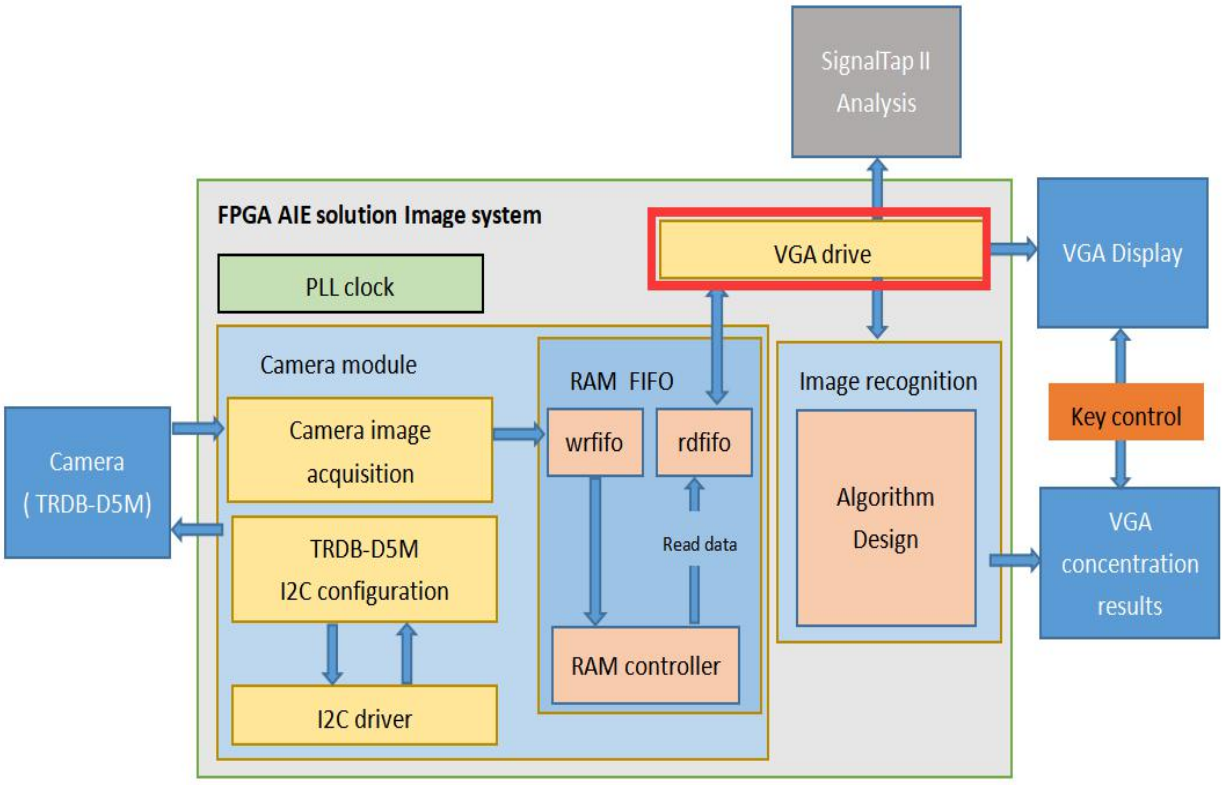


Figure 37 VGA driver module and VGA display module.

VGA timing consists of three elements: pixel clock, horizonal and vertical sync signal, and image data. The system structure can be outlined as shown in Figure 38. Clock dividing module is for generating a

pixel clock, VGA driving module generates horizonal sync signal, and VGA display module outputs image data.

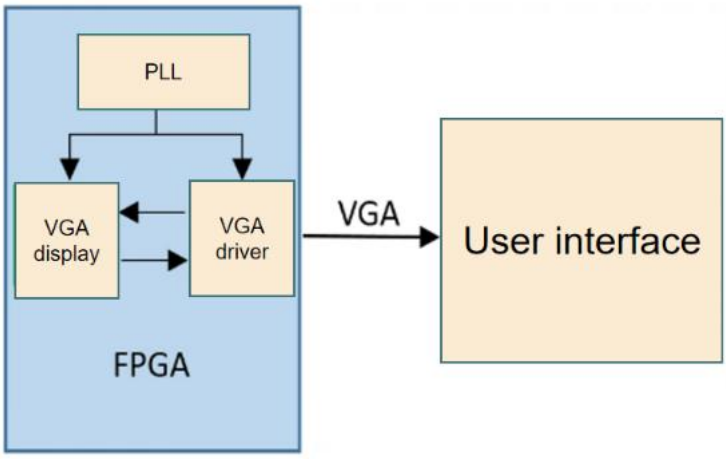


Figure 38 The system structure of VGA timing

4.3.1 VGA display principle and timing divider signal selection

In VGA video transmission standard, the image is decomposed into three primary color signals: red, green, and blue. After digital-to-analog conversion, the data is transmitted in three independent channels under synchronization signals. The synchronization timing of VGA during transmission is divided into vertical synchronization timing and horizontal synchronization timing. As shown in Figure 39 and Figure 40.

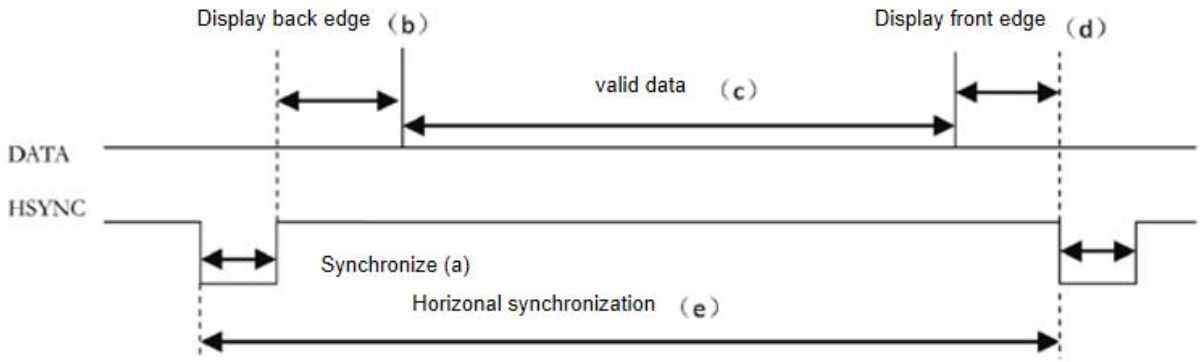


Figure 39 Vertical synchronization timing

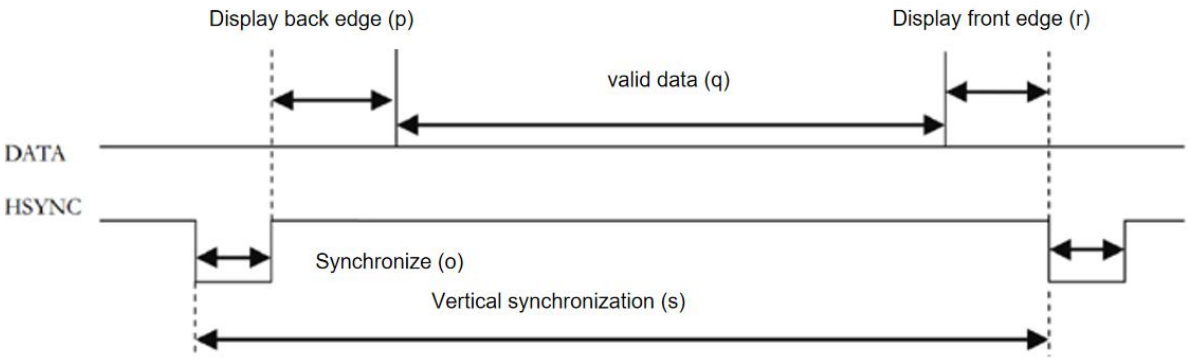


Figure 40 Horizontal synchronization timing

Horizontal synchronization (HSYNC) signals achieves one line of image display in a horizontal scan period. Vertical synchronization signal achieves display one frame image in one vertical scan period, the basic unit of horizontal scan period is pixel clock, which is the time required to complete one pixel display, the basic unit of the vertical scan period is the time required to complete one line of image display. As shown in Figure 41 is horizontal counter counts pixel clocks in verilog design according to the horizontal timing diagram. Figure 42 is vertical counter counts horizontal counter in verilog design according to the vertical timing diagram.

```
//Horizontal counter counts Pixel clocks
always @(posedge vga_clk or negedge sys_rst_n) begin
    if (!sys_rst_n)
        cnt_h <= 10'd0;
    else begin
        if(cnt_h < H_TOTAL - 1'b1)
            cnt_h <= cnt_h + 1'b1;
        else
            cnt_h <= 10'd0;
    end
end
```

Figure 41 Horizontal counter counts pixel clocks in the verilog design

```
//Vertical counter counts Horizontal counter
always @(posedge vga_clk or negedge sys_rst_n) begin
    if (!sys_rst_n)
        cnt_v <= 10'd0;
    else if(cnt_h == H_TOTAL - 1'b1) begin
        if(cnt_v < V_TOTAL - 1'b1)
            cnt_v <= cnt_v + 1'b1;
        else
            cnt_v <= 10'd0;
    end
end
```

Figure 42 Vertical counter counts horizontal counter in the verilog design.

When the resolution is the same but the refresh rate (the number of image updates per second) is different, the corresponding VGA pixel clock and timing parameters are also different, as Figure 43 shown below. The clock frequency used in this experiment is 60Mhz, and the displayed mode is 1024 * 768, which means the line timing is 1344 and the frame timing is 806.

Display modes	Clock	Horizontal timing (pixel number)					Frame timing (horizontal number)				
	(MHz)	a	b	c	d	e	o	p	q	r	s
640x480@60	25.175	96	48	640	16	800	2	33	480	10	525
640x480@75	31.5	64	120	640	16	840	3	16	480	1	500
800x600@60	40.0	128	88	800	40	1056	4	23	600	1	628
800x600@75	49.5	80	160	800	16	1056	3	21	600	1	625
1024x768@60	65	136	160	1024	24	1344	6	29	768	3	806
1024x768@75	78.8	176	176	1024	16	1312	3	28	768	1	800
1280x1024@60	108.0	112	248	1280	48	1688	3	38	1024	1	1066
1280x800@60	83.46	136	200	1280	64	1680	3	24	800	1	828
1440x900@60	106.47	152	232	1440	80	1904	3	28	900	1	932

Figure 43 The resolution, refresh rate, corresponding VGA pixel clock and timing parameters

As shown in Figure 44 is parameter configuration of horizontal synchronization and vertical synchronization according to the resolution in verilog design.

```
//parameter define
parameter  H_SYNC   =  11'd136;   //Horizontal synchronization
parameter  H_BACK   =  11'd160;   //Horizontal display back edge
parameter  H_DISP   =  11'd1024;  //Horizontal valid line
parameter  H_FRONT  =  11'd24;    //Horizontal display front edge
parameter  H_TOTAL  =  11'd1344;  //Horizontal scan cycle

parameter  V_SYNC   =  11'd6;     //Vertical synchronization
parameter  V_BACK   =  11'd29;    //Vertical display back edge
parameter  V_DISP   =  11'd768;   //Vertical valid line
parameter  V_FRONT  =  11'd3;     //Vertical display front edge
parameter  V_TOTAL  =  11'd806;   //Vertical scan cycle
```

Figure 44 Parameter configuration of H_SYNC and V_SYNC Clock divider module

The clock divider module (vga_pll) is implemented by calling previously designed phase-locked loop (PLL) IP core. According to the resolution and scan rate required by the experiment, the pixel clock used in VGA display is 25.175Mhz. Because the resolution is not very high, set PLL IP core to output 25 MHz clock as pixel clock.

VGA driver module (vga_driver) is driven by pixel clock and outputs horizonal (Hga_hs) and vertical (vga_vs) sync signals according to the parameters of VGA timing. At the same time, VGA driver

module also needs to output vertical and horizontal coordinates of pixels for VGA display module (vga_display) to call.

VGA display module divides screen display into five equal width columns according to VGA display testing module and assigns different color values to pixels by judging abscissa of pixels are located, thereby achieving color bar display.

```
if((pixel_xpos >= 0) && (pixel_xpos < (H_DISP/5)*1))
    pixel_data <= WHITE;
else if((pixel_xpos >= (H_DISP/5)*1) && (pixel_xpos < (H_DISP/5)*2))
    pixel_data <= BLACK;
else if((pixel_xpos >= (H_DISP/5)*2) && (pixel_xpos < (H_DISP/5)*3))
    pixel_data <= RED;
else if((pixel_xpos >= (H_DISP/5)*3) && (pixel_xpos < (H_DISP/5)*4))
    pixel_data <= GREEN;
else
    pixel_data <= BLUE;
```

Figure 46 Color bar display

4.3.2 Top-level module connection diagram

As shown in system block diagram, FPGA includes four modules, top-level module (vga_colorbar), clock divider module (vga_pll), VGA display module (vga_display), and VGA driver module (vga_driver). Each module port and signal connection are as shown in Figure 47.

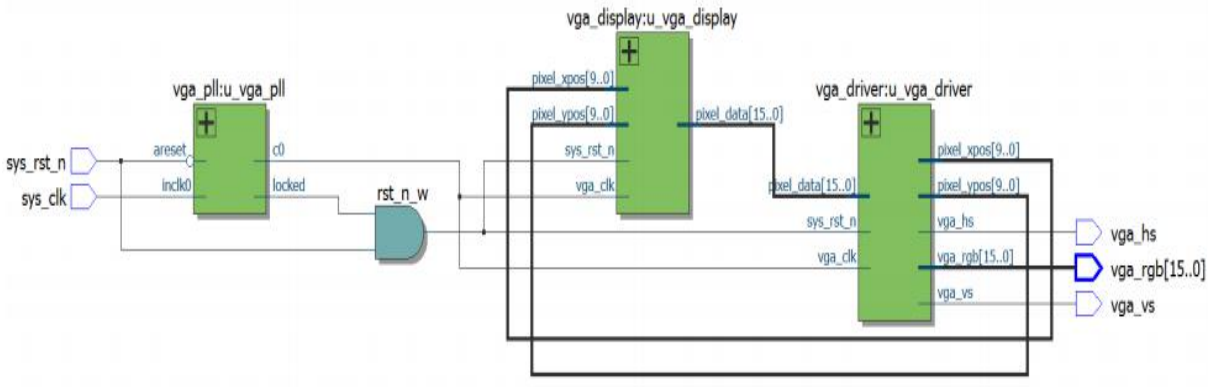


Figure 47 Top-level module connection diagram.

4.3.3 SignalTap II software simulation and verification

The waveform of display one-line images of VGA color bar program is captured by SignalTap. Figure 48 contains a complete horizonal scan period. The effective image area is divided into five different areas, and the pixel colors of different areas are different.

Figure 48 The waveform of display one-line images of VGA color bar program.

4.3.4 Simulation and verification of screen display

After downloading, the display on the screen is as shown in Figure 49, VGA color bar display program download verification is successful.

Figure 49 VGA color bar display on the screen

4.4 Camera acquisition module

Image acquisition module and I2C configuration module are as shown in Figure 50.

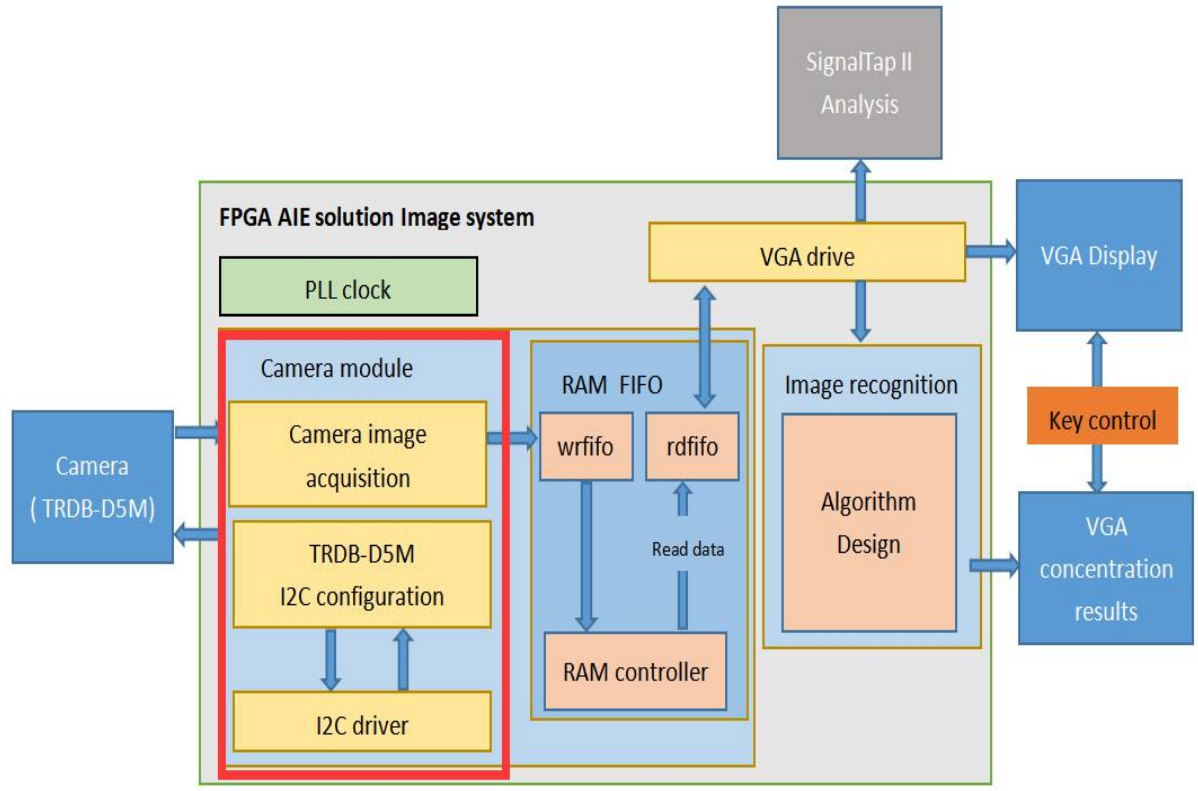


Figure 50 Image acquisition module and I2C configuration module

The system block diagram of TRDB-D5M camera module for this experiment is shown in Figure 51. Then use the previously designed PLL module and VGA display module to form a complete set of image acquisition system. PLL clock module provide clocks for I2C driver module, VGA driver module and FIFO memory control module.

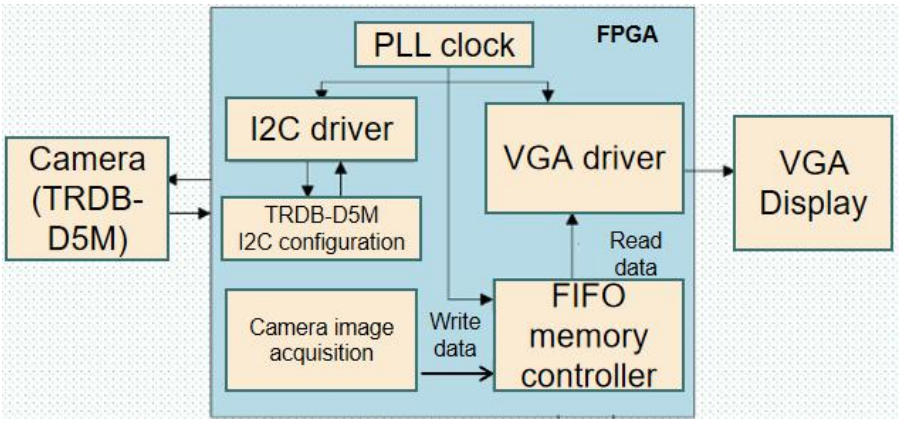


Figure 51 The system block diagram of TRDB-D5M camera module.

4.4.1 Camera acquisition principle and background introduction

TRDB - D5M is a 1/4-inch single-chip image sensor with a 2,961*1944 (500W pixel) photosensitive array, and can achieve the fastest image acquisition for 15fps QSXVGA (2592*1944) or 90fps VGA (640*480) resolution. The sensor enables higher performance such as high sensitivity, low crosstalk and low noise.

Figure 52 TRDB - D5M Camera

As can be seen from Figure 53, timing generator controls image array, amplifier (AMP), AD conversion and output external timing signals (VSYNC, HREF, and PCLK). The external clock XVCLK passes through PLL and output clock is used as system control clock; photosensitive array converts optical signal into analog signal, and then to 10-bit AD converter after passing through gain amplifier; AD converter converts analog signal into digital signal, and performs related image processing by ISP, finally outputs 10-bit video data stream in configured format. Gain amplifier control and ISP can be configured through registers. TRDB - D5M uses two-wire IIC interface bus to configure registers, it uses 16 bits (two bytes) to represent the register address. The write transfer protocol of TRDB - D5M SCCB is shown in Figure 53 below.

In the image acquisition system, the setting of the color gain is a necessary acquisition parameter. Image acquisition process is to convert analog signals to digital signals and setting reasonable value can ensure that the image does not appear distorted in the display system.

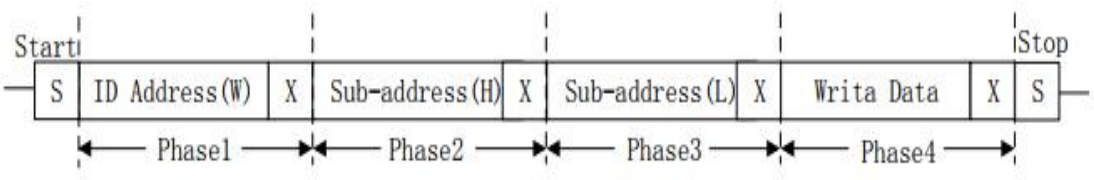


Figure 53 I2C communication.

4.4.2 Camera input configuration -- I2C communication

TRDB - D5M camera must be initialized first before operation properly, by configuring the registers to operate in expected mode to obtain a better-quality image. Write transfer protocol use IIC driver code to configure camera directly. The configuration code for this design is shown in Figure 54.

```
//Combinatorial logic to determine state transition conditions
always @( * ) begin
//    next_state = st_idle;
    case(cur_state)
        st_idle: begin                          // Idle state
           if(i2c_exec) begin
               next_state = st_sladdr;
           end
           else
               next_state = st_idle;
        end
        st_sladdr: begin
            if(st_done) begin
                if(bit_ctrl)                    // Judging it is a 16-bit or 8-bit byte address
                   next_state = st_addr16;
                else
                   next_state = st_addr8 ;
            end
            else
                next_state = st_sladdr;
        end
         st_addr16: begin                                // Write 16-bit byte address
             if(st_done) begin
                 next_state = st_addr8;
             end
             else begin
                 next_state = st_addr16;
             end
         end
         st_addr8: begin                                 // Write 8-bit byte address
             if(st_done) begin
                 if(wr_flag==1'b0)                       // Judging Read/Write
                     next_state = st_data_wr;
                 else
                     next_state = st_addr_rd;
             end
             else begin
                 next_state = st_addr8;
             end
         end

         st_data_wr: begin                              // Write 8-bit data
             if(st_done)
                 next_state = st_stop;
             else
                 next_state = st_data_wr;
         end
         st_addr_rd: begin                              // Write address to read data
             if(st_done) begin
                 next_state = st_data_rd;
             end
             else begin
                 next_state = st_addr_rd;
             end
         end
```

```
        st_data_rd: begin                          // Read 8-bit data
            if(st_done)
                next_state = st_stop;
            else
                next_state = st_data_rd;
        end
        st_stop: begin                             // End I2C Communication
            if(st_done)
                next_state = st_idle;
            else
                next_state = st_stop ;
        end
        default: next_state= st_idle;
    endcase
end
```

Figure 54 The configuration code of I2C communication

Output image parameter setting

ISP input window setting, pre-zoom window setting and output size window setting of TRDB - D5M are shown as Figure 55.

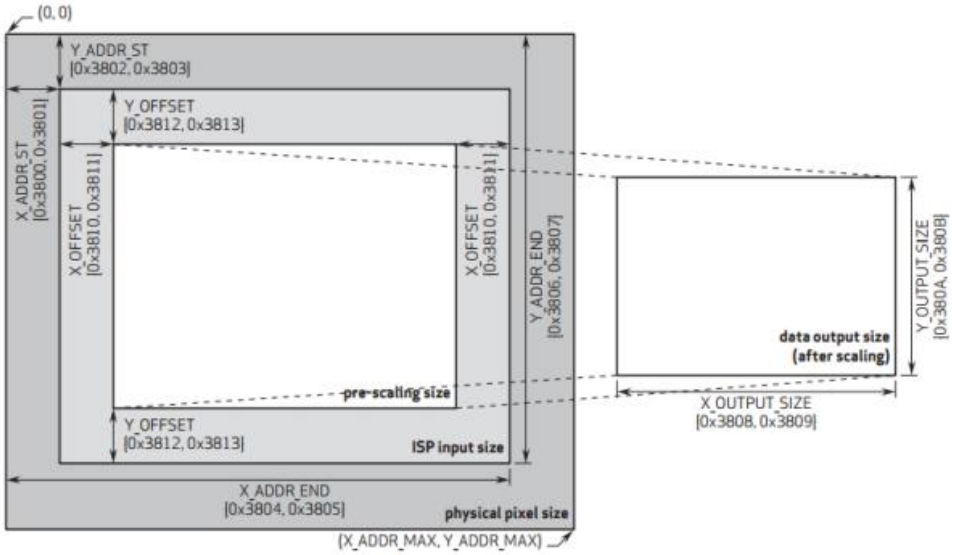


Figure 55 Output image parameter setting

ISP Input Size setting: Allow user to set the entire sensor display area (physical pixel size, 2632*1951, where 2592*1944 pixels are valid).

- X_ADDR_ST (Register address: 0x3800、0x3801)
- Y_ADDR_ST (Register address: 0x3802、 0x3803)
- X_ADDR_END (Register address: 0x3804、0x3805)
- Y_ADDR_END (Register address: 0x3806、0x3807)

The pixel data in this window setting range will enter ISP for image processing.

However, many registers can take the default values and do not need to be configured, TRDB-D5M Software Application Note used for register reference configuration. In this experiment, output format and size are configured as expected value, and other registers follow the recommended configuration of TRDB-D5M Software Application Note.

4.4.3 Output signal timing diagram from camera and acquisition method

Figure 57 shows the timing diagram of TRDB-D5M output image data. As can be seen from the figure, each PCLK clock outputs an 8-bit or 10-bit pixel data. the rising edge of FVAL is the start of a frame, LVAL starts to pull high, and then output valid data.

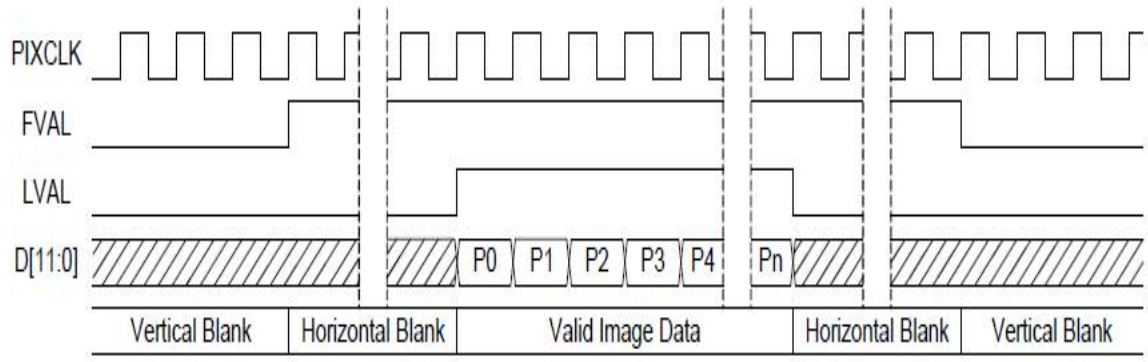


Figure 57 Frame timing diagram

As shown in Figure 58 are the frame number of output image data and code of valid bit of this design.

```
//Count the number of frames
always @(posedge cam_pclk or negedge rst_n) begin
    if(!rst_n)
        cmos_ps_cnt <= 4'd0;
    else if(pos_vsync && (cmos_ps_cnt < WAIT_FRAME))
        cmos_ps_cnt <= cmos_ps_cnt + 4'd1;
end

//Frame valid flag
always @(posedge cam_pclk or negedge rst_n) begin
    if(!rst_n)
        frame_val_flag <= 1'b0;
    else if((cmos_ps_cnt == WAIT_FRAME) && pos_vsync)
        frame_val_flag <= 1'b1;
    else;
end
```

Figure 58 The frame number of the output image data and the code of the valid bit.

Linear interpolation algorithm

Through the output configuration of TRDM D5M, it can be found that the image is output in Bayer format. To display RGB, the conversion between Bayer format and RGB format must be performed. Linear interpolation algorithm is simple and based on four adjacent points. As Figure 59 shows, odd rows include pixels of green and red, and even rows include pixels of blue and green. Odd column s include pixels of green and blue, and even columns include pixels of red and green.

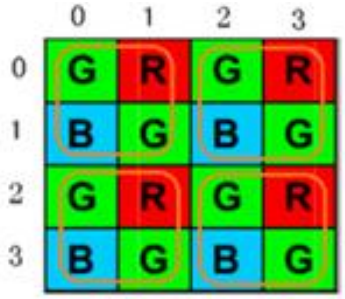


Figure 59 The Linear interpolation algorithm

Figure 60 shows verilog code of Linear interpolation algorithm design.

```
if({iY_Cont[0],iX_Cont[0]}==2'b10)
begin
    mCCD_R   <= mDATA_0;
    mCCD_G   <= mDATAd_0+mDATA_1;
    mCCD_B   <= mDATAd_1;
end
else if({iY_Cont[0],iX_Cont[0]}==2'b11)
begin
    mCCD_R   <= mDATAd_0;
    mCCD_G   <= mDATA_0+mDATAd_1;
    mCCD_B   <= mDATA_1;
end
else if({iY_Cont[0],iX_Cont[0]}==2'b00)
begin
    mCCD_R   <= mDATA_1;
    mCCD_G   <= mDATA_0+mDATAd_1;
    mCCD_B   <= mDATAd_0;
end
else if({iY_Cont[0],iX_Cont[0]}==2'b01)
begin
    mCCD_R   <= mDATAd_1;
    mCCD_G   <= mDATAd_0+mDATA_1;
    mCCD_B   <= mDATA_0;
end
```

Figure 60 Verilog code of Linear interpolation algorithm design

4.4.4 The connection diagram of the camera top-level module

The schematic diagram of top-level module is shown as Figure 61. From the figure, IIC configuration module and I2C driver module control the start and end of sensor initialization. After initialize the sensor, image acquisition module writes acquired data to RAM read/write control module, and VGA driver module read data from RAM control module, therefore achieve data collection, caching, and display. It should be noted that image data acquisition module starts to output data after RAM and sensor are initialized, this avoids data writing during RAM initialization process.

PLL clock module (pll_clk):

PLL clock module is implemented by calling PLL IP core. It outputs three clocks with frequencies of

FIFO phase offset clock, clock for FIFO read/write control module, and drive clock for I2C driver module and VGA driver module.

I2C driver module (i2c_dri):

I2C driver module is for driving TRDB - D5M SCCB interface bus. Users can configure TRDB - D5M registers according to user interface provided by the module.

I2C configuration module (i2c_TRDB - D5M_rgb565_cfg):

The drive clock of I2C configuration module is provided by clock output from I2C driver module, which facilitates data interaction between I2C driver module and I2C configuration module. The data and register address that needs to be configured, and the start and stop bits of initialization, also the register address and data of TRDB - D5M that output from module and control signal that controls the start of I2C driver module, are directly connected to the user interface of I2C driver module.

Camera image acquisition module (cmos_capture_data):

By pixel clock driven, camera image acquisition module converts vertical, horizontal sync signal and 8-bit data into write enable signal of FIFO read/write control module and 16-bit write data signal. Then complete the acquisition of FIFO sensor image.

FIFO memory read/write control module (fifo_top):

FIFO memory read/write controller module is for cache the image data output by image sensor. This module encapsulates the complex read and write operations of RAM into FIFO user interface, which is very convenient for users.

VGA driver module (vga_driver):

VGA driver module is for driving VGA display. The module outputs pixel data by reading FIFO read/write control module. In this experiment, module internal signal data_req (data request signal) is output to the port to read data from FIFO controller.

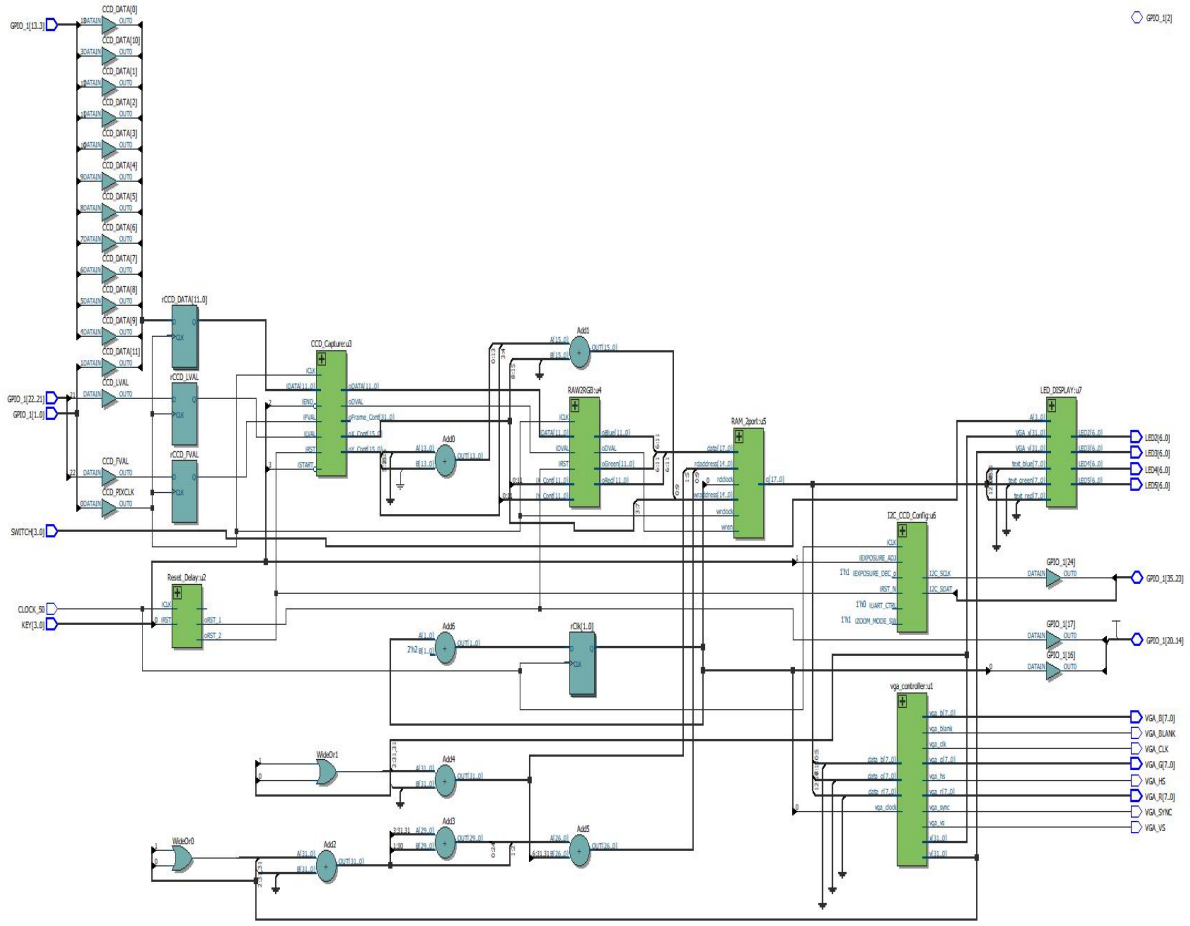


Figure 61 The schematic diagram of top-level module

4.4.5 Simulation and verification of the acquisition image from Camera module

Color bar testing mode

After image sensor is configured in color test mode, colors are output on the screen to test image sensor is on normal operation. By configured Bit[7] of register 0x503d, the color text bar mode can be turned on and off. When the color bar mode needs to be turned on, the register 0x503d is configured to 0x80. When it needs to be turned off, the register 0x503d is configured to 0x00. Figure 62 shows the image output after color bar mode is turned on.

Figure 62 Color bar test

5. Development and Testing

Figure 63 shows the schematic diagram of FPGA image acquisition system in this project, which includes UV lights emission device and black box acquisition environment, FPGA acquisition system, and experiment solutions with urine. UV lights are emitted to the experiment solution by UV lights emitting device, and the images of solutions are from dark blue to light green depending on the solution concentration. After FPGA image acquisition system, the solution concentration can be recognized by RGB data.

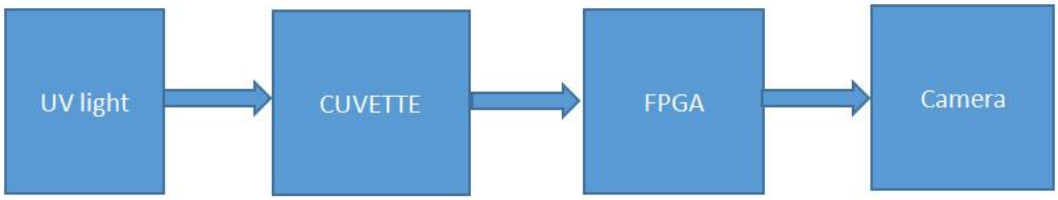


Figure 63 The schematic diagram of the entire FPGA image acquisition system

5.1 Experiment solution testing environment

The black box environment is achieved by Tran Tam Anh Pham in my group. The main function of the device is to reduce the influence of external noise on the external environment, and fix the distance between camera and solutions as shown in Figure 64.

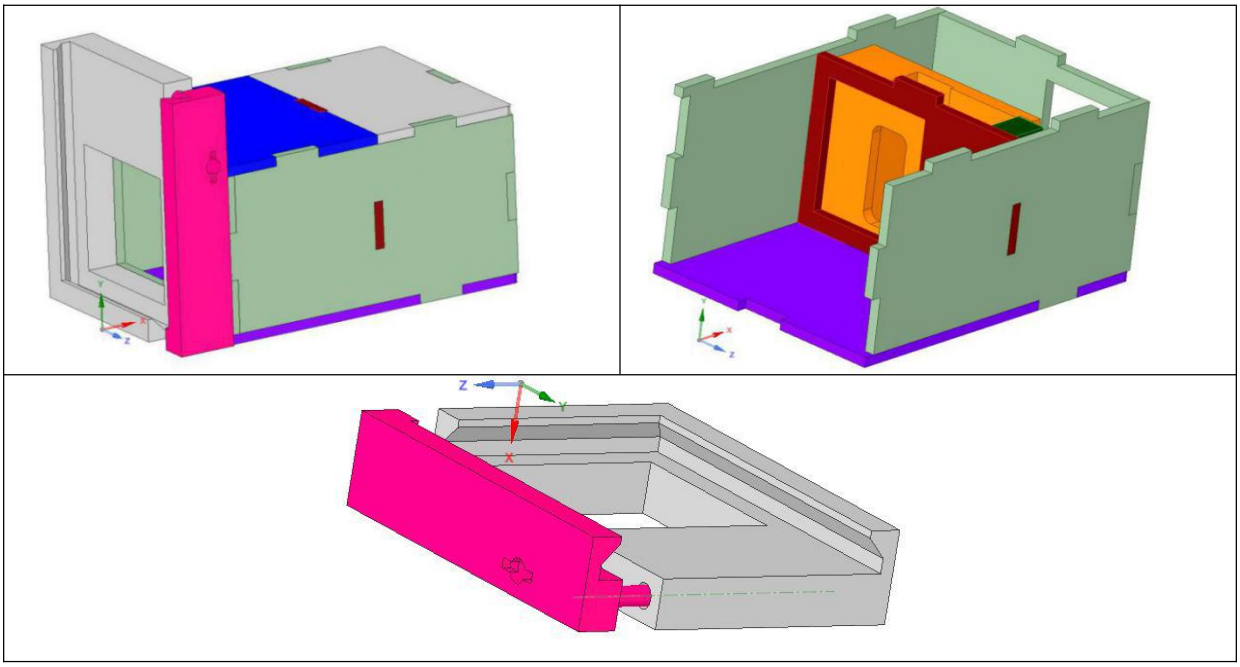


Figure 64 Urine tester device and Camera holder.

When the distance between camera and solution is different, camera acquisition module will generate some noise due to the distance. As the parameter configuration of camera module has been

configured according to the recommended parameters of TRDB - D5M, the resolution of image cannot be changed by changing the registers inside camera. Therefore, the specific acquisition distance between camera and solution has the highest illumination sensitivity, which means that camera module can obtain the highest quality image information.

The main function of UV lights emitting device is to change the intensity of UV lights by changing the resistance of slide rheostats. As shown in Figure 65, it can be found that the greater the resistance of the slide rheostat is, the stronger the illumination intensity.

Figure 65 Physical picture of Urine tester device

Because of the different light intensities, solutions will generate different images. However, camera module itself has the highest sensitivity to specific light intensity, which means photosensitive module of camera can obtain the highest quality image information.

The experiment solution with urine is achieved by Xinyi Zhang. The solution is colorless under normal light but is light blue under UV light. However, AIE solution is an organic ethanol solution, it is greatly affected by the temperature and humidity in the laboratory. Therefore, the testing solution is stored

in refrigerator to reduce the volatility. However, because the acquisition process of image system has lasted a long process, the volatility of solution causes a decrease in concentration. However, based on laboratory conditions, this design does not discuss the volatility of the solution under different temperatures and humidity.

The solution in this experiment is Ethanol solution, which has a certain volatility. I usually put the solution in a laboratory refrigerator and at a temperature of zero degrees to prevent the Ethanol solution from volatilizing and avoid leading to errors in the solution concentration. During the acquisition process, the acquisition method can be used on demand, which reduce the interference of the external environment on the overall solution concentration.

Because the image acquisition system needs certain portability and includes image acquisition, processing and display. Therefore, in the early stage of the experiment, I used the Quarts software to verify whether the data of the image acquisition system was accurately recorded in the processor. When the test is completed, I can directly observe the RGB data at different concentrations through the VGA display module. The method of displaying the solution image by software is not involved in this experiment. The main reason is that additional programming is required, also it does not meet the requirements of system portability.

This project in the group is responsible for FPGA acquisition module. The main function of the device is the acquisition and processing of image information. The concentrations of solutions are identified according to the solution image collected by camera.

5.2 RGB image acquisition method (VGA result and SignalTap II)

FPGA acquisition system is RGB acquisition through camera module, after RAM storage and finally displayed to the screen through VGA interface. There are two different methods when read RGB data.

1. Observe the input value of VGA interface in SignalTap II by running the program.

Through previous experiments, it can be found that we are able to observe the running program through SignalTap II from Quarts. However, observing RGB has certain disadvantages. Firstly, the

measurement method is not direct enough, user needs to have a certain Quarts use basis to complete the measurement. Secondly, this does not meet the requirement of potable as FPGA needs to be connected to the computer by USB.

2. It also can output RGB data to screen through VGA interface, the way to collect RGB data is more intuitive, user can directly obtain RGB value through screen and it also meet the requirements of system portability.

The display module of the image acquisition system in this experiment was processed by VGA display module. The main advantage of using Dell series of VGA displays is the ease of image display. In a portable image acquisition system, LCD display module has better display performance and can be perfectly compatible with a portable image acquisition system.

This experiment results use two different methods to collect RGB values, and the collected point is the center points of the camera acquisition range. As shown in Figure 66 is the operation diagram of the identification system.

In this experiment, our team designed an acquisition box for image acquisition to reduce the external environment's interference to the acquisition system. Therefore, fixing the solution in the middle of the acquisition box can ensure that the acquisition center of the image acquisition system is the center point of the solution. The method of collecting more image data to obtain the average value can effectively improve the stable value of data, but it requires more processing resources. So this experiment did not involve that.

Image acquisition module	RGB value acquisition module
	
SignalTap II software acquisition module	

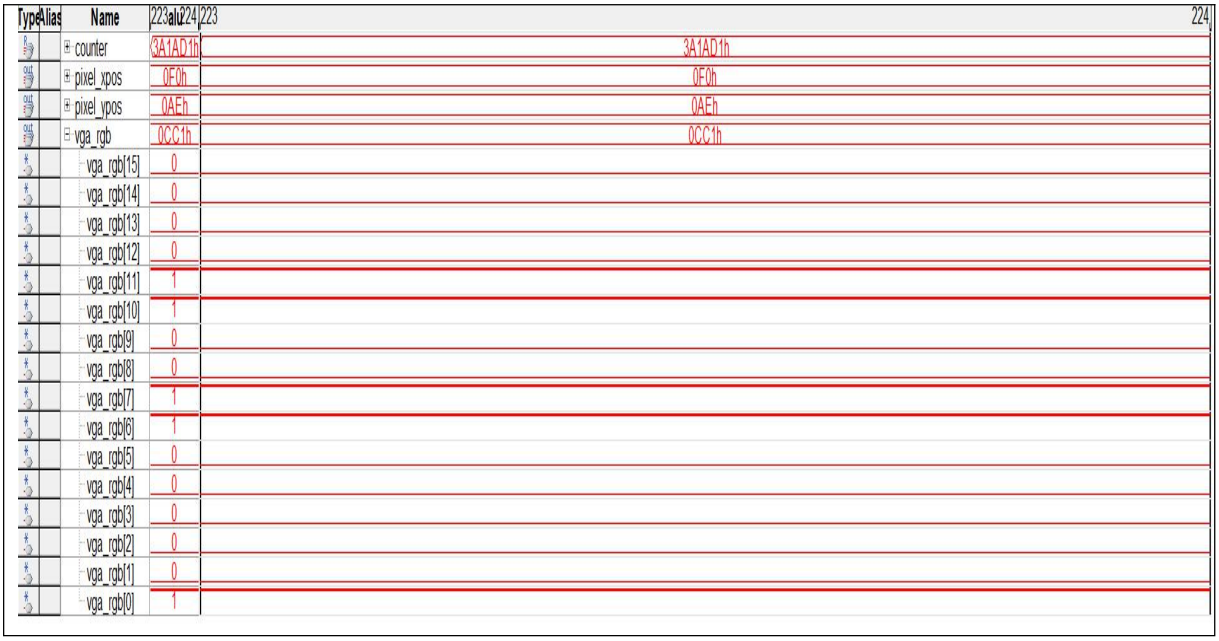


Figure 66 The operation diagram of the identification system

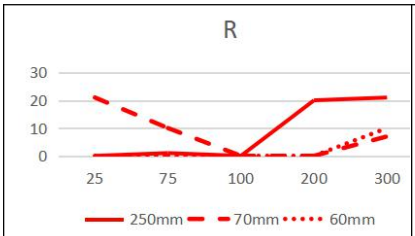
5.2 The experiment solutions acquisition results by RGB image acquisition format

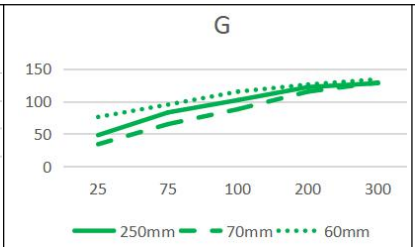
5.3.1 Camera module is at a different distance from the solutions

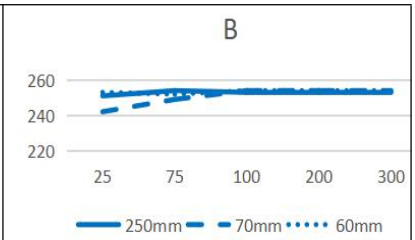
As shown in Table 1, the distance between the solution and camera is adjusted by using black box environment, and the solutions to be tested are from 25 mg/L to 300 mg/L. It can be found that when the concentration increase, red and green value are decreased, and blue value is increased. This match the color change from shallow to deep throughout the solution concentration. When the distance of the solution changes, it can be found that RGB change at the same trend, but when the distance of the solution and camera module are kept at 60 cm, RGB change is the most significant which also meets the parameter requirements of TRDB - D5M design.

It can be found through experiments that when the concentration is constant, the RGB value collected by the acquisition system is approximately the same and the accuracy is 50 PPb, the error of the image system will not affect the accuracy of the solution concentration. Therefore, the image acquisition system of this experiment only collected the center point in the image as the acquisition point of the image.

Table 1 The distance between the solution and the camera

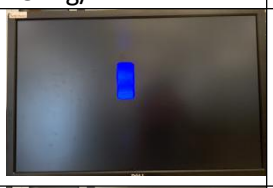
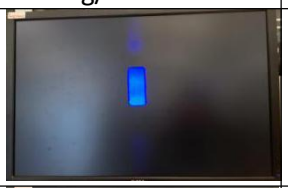






(Distance)	Deviation	(Distance)	Deviation	(Distance)	Deviation
R (250 mm)	21	G (250 nm)	80	B (250 nm)	2
R (70 mm)	21	G (70 nm)	95	B (70 nm)	12
R5 (60 mm)	10	G (60 nm)	58	B (60 nm)	2

Table 2 VGA screen display with different distances at different concentrations

	Screen display at different concentrations				
	25 mg/L	75 mg/L	100 mg/L	200 mg/L	300 mg/L
250 mm					
70 mm					
60 mm					

As shown in Figure 67 is the RED values of different concentrations at different distances.

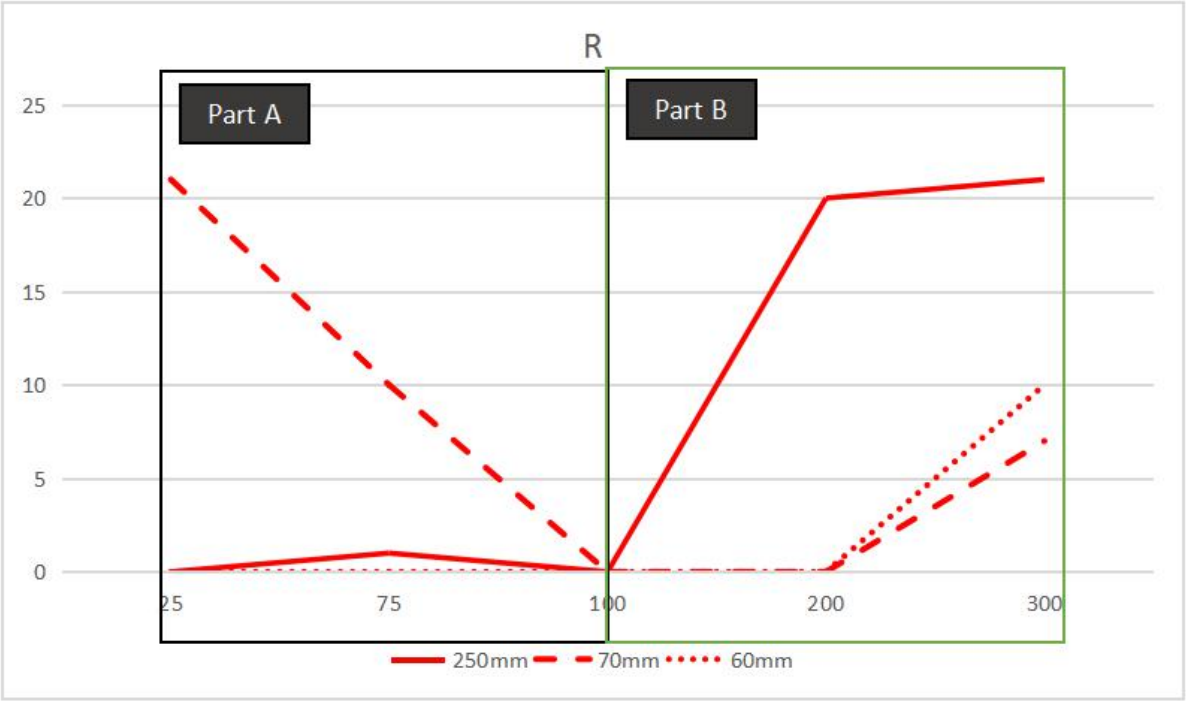


Figure 67 The RED values of different concentrations at different distances

Table 3 The RED values of different concentrations at different distances

Sample concentrations	R (250 mm)	R (70 mm)	R (60 mm)
25 mg/L	0	21	0
75 mg/L	1	10	0
100 mg/L	0	0	0
200 mg/L	20	0	0
300 mg/L	21	7	10
Deviation= (MAX value - MIN value)	21	21	10

As shown in Figure 68 is the Green values of different concentrations at different distances.

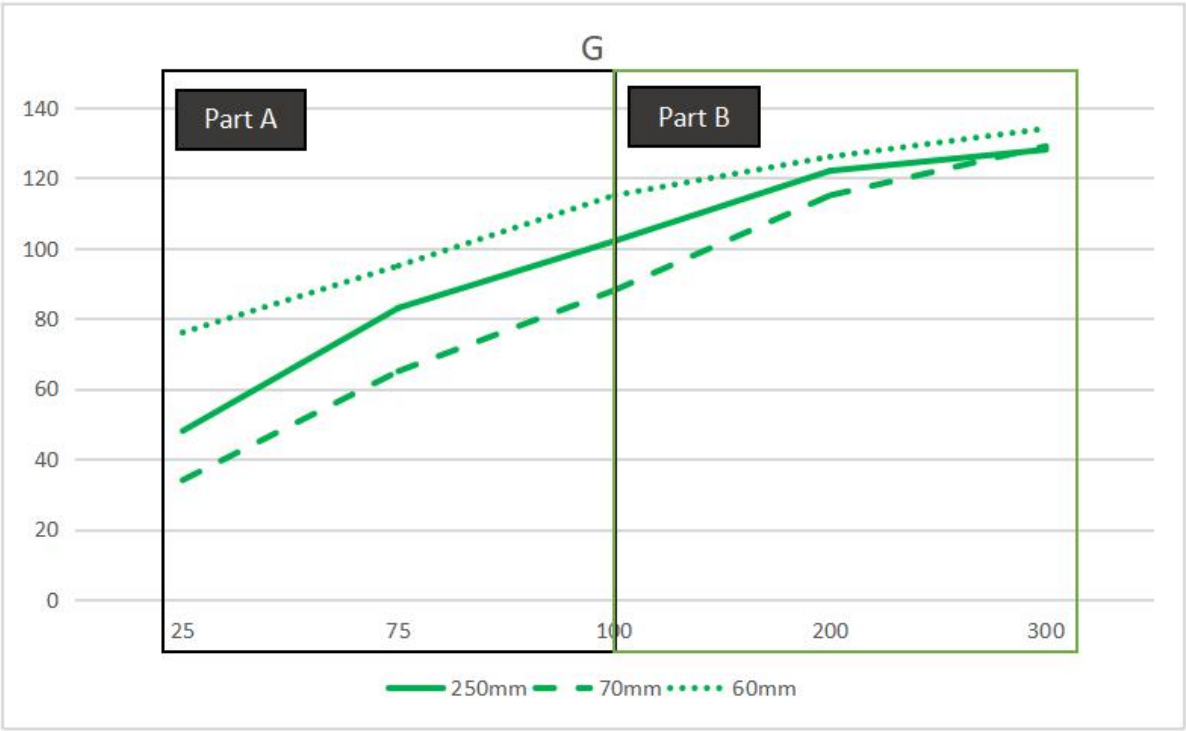


Figure 68 Green values of different concentrations at different distances

Table 4 The Green values of different concentrations at different distances

Sample concentrations	G (250 mm)	G (70 mm)	G (60 mm)
25 mg/L	48	34	76
75 mg/L	83	65	95
100 mg/L	102	88	115
200 mg/L	122	115	126
300 mg/L	128	129	134
Deviation = (MAX value - MIN value)	80	95	58

As shown in Figure 69 is the Blue values of different concentrations at different distances.

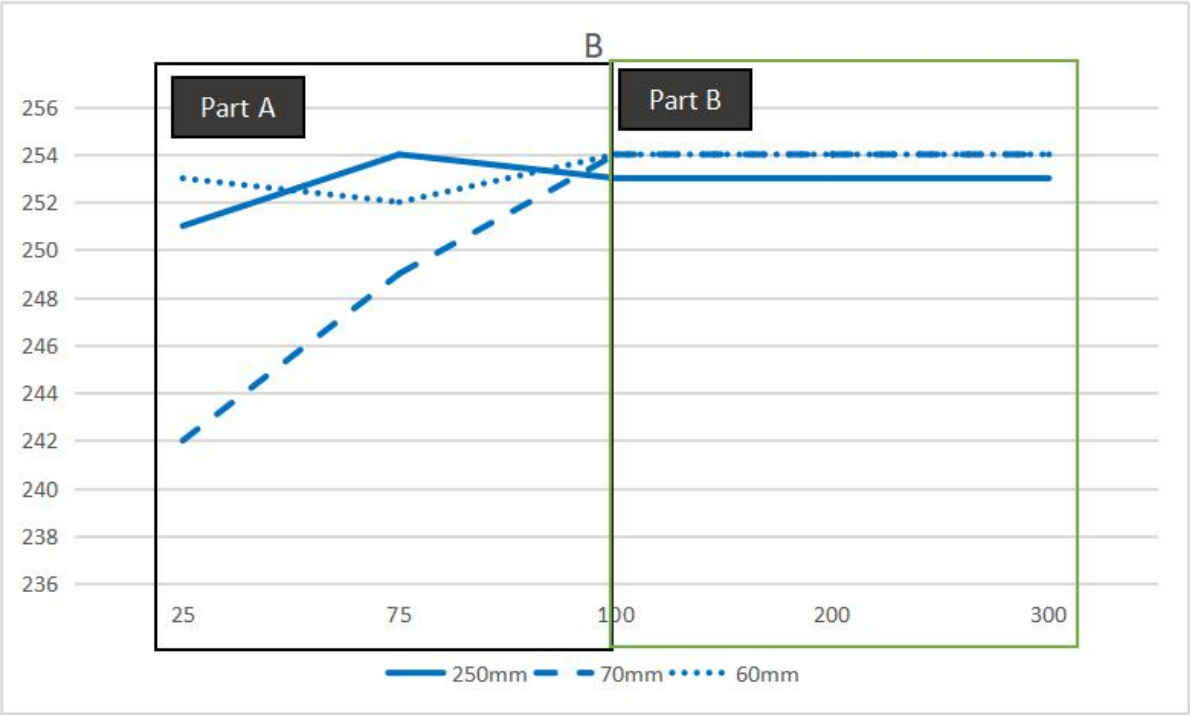


Figure 69 Blue values of different concentrations at different distances

Table 5 The Blue values of different concentrations at different distances

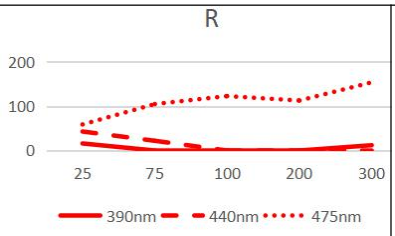
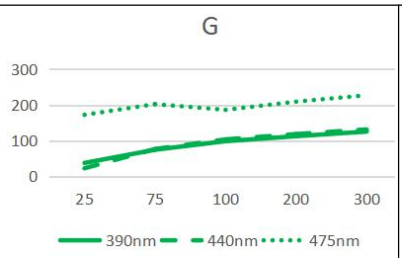
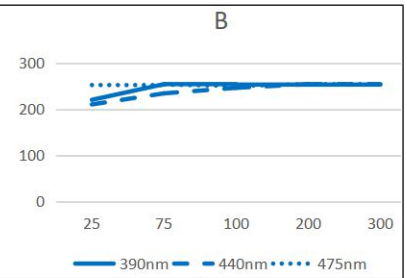
Sample concentrations	B (250 mm)	B (70 mm)	B (60 mm)
25 mg/L	251	242	253
75 mg/L	254	249	252
100 mg/L	253	254	254
200 mg/L	253	254	254
300 mg/L	253	254	254
Deviation = (MAX value - MIN value)	2	12	2

5.3.2 UV lights in different intensities conditions

Adjust the light intensity of UV lights, RGB curve is shown in Table 6. It can be found that when the concentration increase, red and green value are decreased, and blue value is increased. This match

the color change from shallow to deep throughout the solution concentration. When UV lights intensity changes, RGB value will change. But when the light intensity is kept at 440nm, RGB change is the most significant.

Table 6 UV lights are in different brightness conditions

R	G	B
		

(Intensity)	Deviation	(Intensity)	Deviation	(Intensity)	Deviation
R (390nm)	16	G (390 nm)	88	B (390 nm)	34
R (440nm)	43	G (440 nm)	109	B (440 nm)	44
R5 (475nm)	95	G (475 nm)	55	B (475 nm)	4

Table 7 VGA screen display with different intensities at different concentrations

	Scren display at different concentrations				
	25 mg/L	75 mg/L	100 mg/L	200 mg/L	300 mg/L
390nm					
440nm					
475nm					

As shown in Figure 70 is the RED values of different concentrations under different light intensities (475 nm to 390 nm).

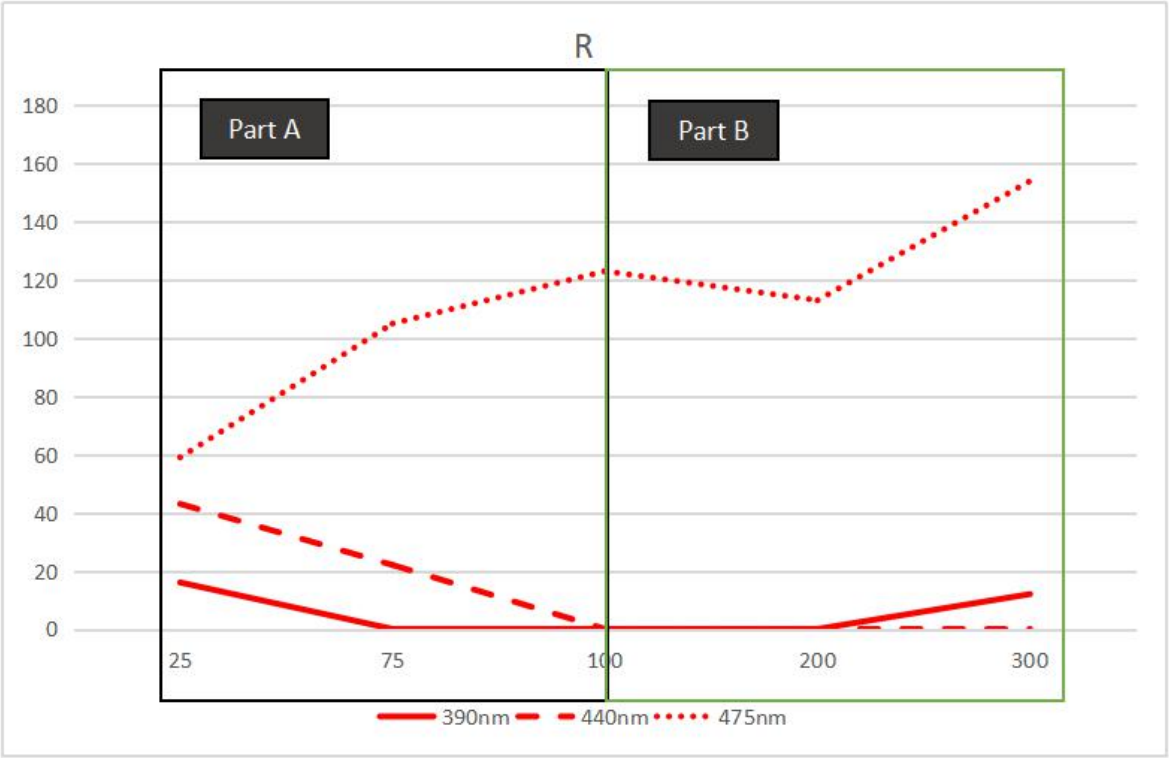


Figure 70 The RED values of different concentrations under different light intensities

Table 8 The RED values of different concentrations under different light intensities

Sample concentrations	R (390 nm)	R (440 nm)	R5 (475 nm)
25 mg/L	16	43	59
75 mg/L	0	22	105
100 mg/L	0	0	123
200 mg/L	0	0	113
300 mg/L	12	0	154
Deviation = (MAX value - MIN value)	16	43	95

As shown in Figure 71 is the Green values of different concentrations under different light intensities

(475 nm to 390 nm).

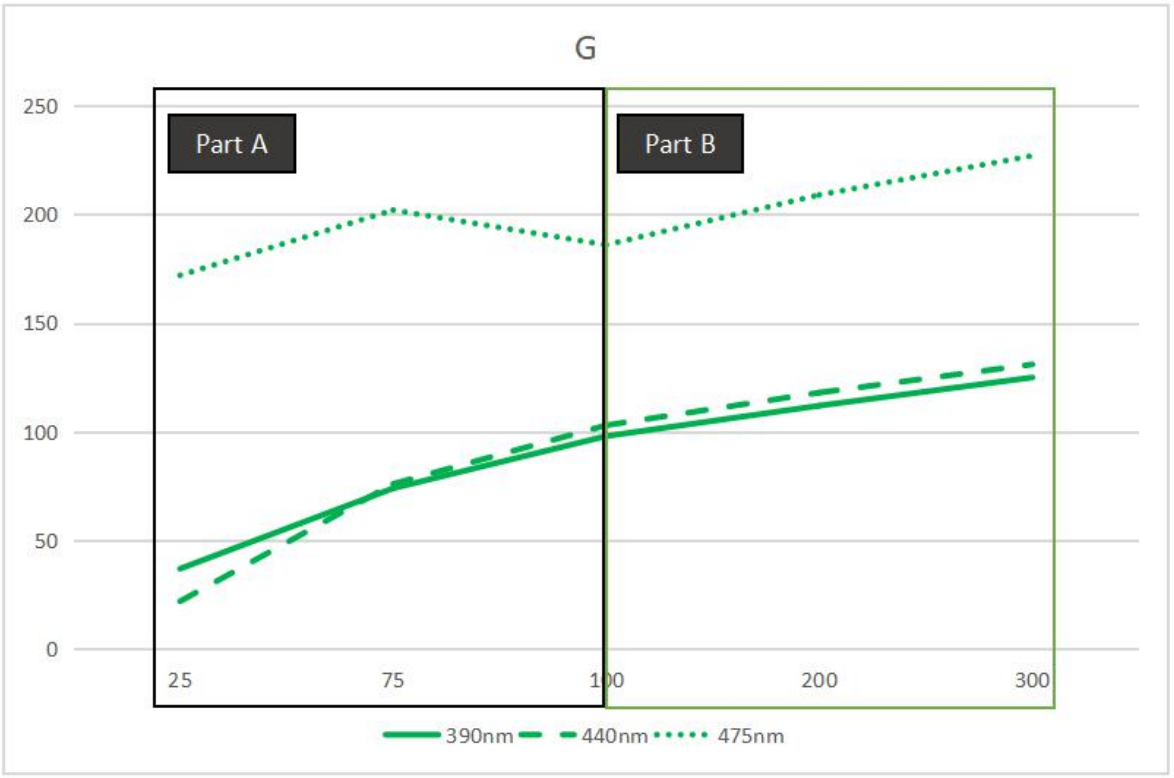


Figure 71 The Green values of different concentrations under different light intensities

Table 9 The Green values of different concentrations under different light intensities

Sample concentrations	G (390 nm)	G (440 nm)	G (475 nm)
25 mg/L	37	22	172
75 mg/L	74	76	202
100 mg/L	98	103	186
200 mg/L	112	118	209
300 mg/L	125	131	227
Deviation = (MAX value - MIN value)	88	109	55

As shown in Figure 72 is the Blue values of different concentrations under different light intensities (475 nm to 390 nm).

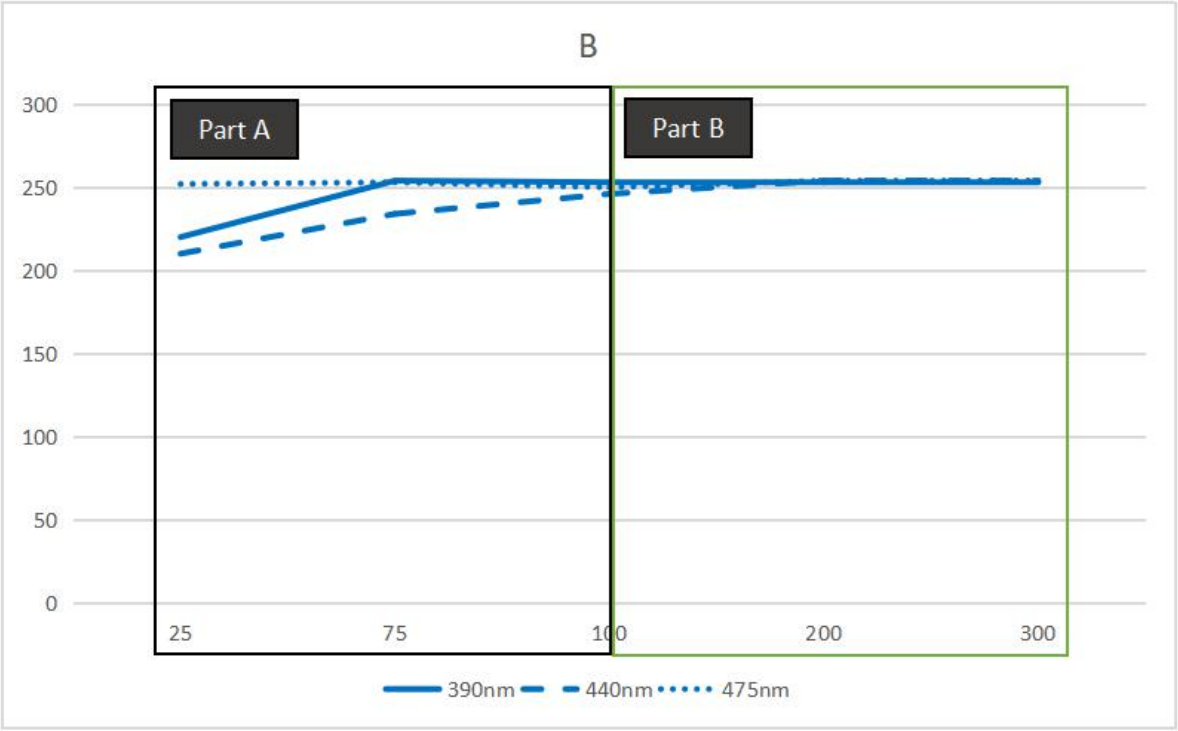


Figure 72 Blue values of different concentrations under different light intensities

Table 10 Blue values of different concentrations under different light intensities

Sample concentrations	B (390 nm)	B (440 nm)	B (475 nm)
25 mg/L	220	210	252
75 mg/L	254	234	253
100 mg/L	253	246	250
200 mg/L	253	254	254
300 mg/L	253	254	254
Deviation = (MAX value - MIN value)	34	44	4

5.4 Analyze RGB data

5.4.1 UV lights intensity limit

It can be found that when UV light intensity is at 475nm, the RGB curve shows a significant oscillation, and RGB value shows a significant deviation. This is because the light intensity is too large and cause

the sampled image overexposed, which means the image displayed by VGA will be always light blue or white regardless of the concentration of the solutions. Therefore, in order to ensure the stability of image data acquisition, this experiment does not recommend using light intensity that higher than 440nm to collect image information of solutions.

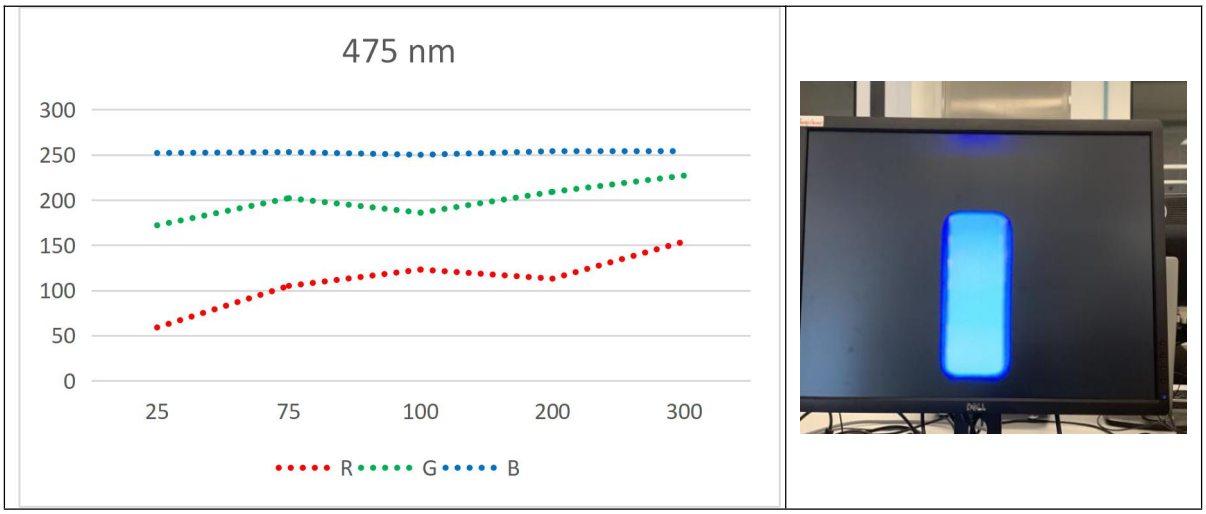


Figure 73 UV light intensity is at 475 nm

5.4.2 Analyze RGB trend

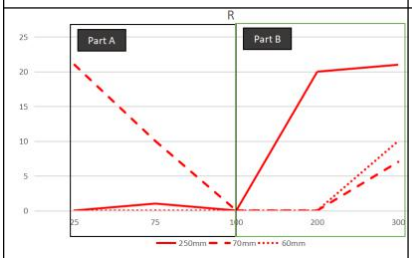
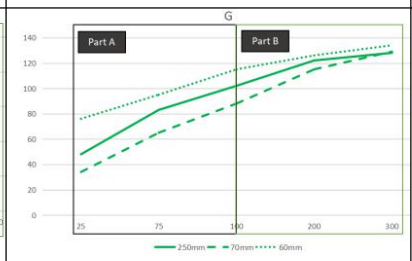
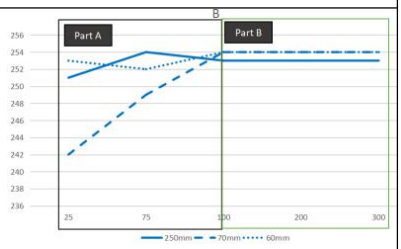
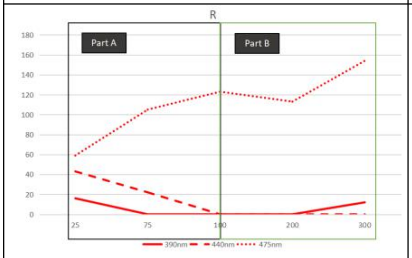
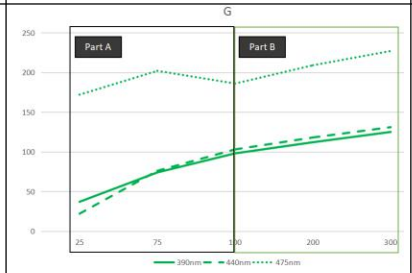
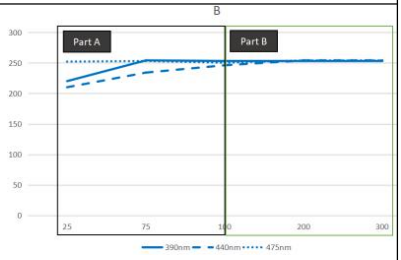
As shown in Table 11 is a comparison chart in the case of different intensities and solution distances of RGB values. It can be found that when the value of solution is in the range of 25 mg/L - 100 mg/L, linear change is not the same as the solution at 100 mg/L - 300 mg/L. For example, the red is slowly decreasing at 25 mg/L - 100 mg/L, and is slowly increasing at 100 mg/L - 300 mg/L. Green is in a steady upward trend at 25 mg/L -100 mg/L and is slowly increasing at 100 mg/L -300 mg/L. Blue is in a steady upward trend from 25 mg/L - 100 mg/L, and is slowly increasing from 100 mg/L to 300 mg/L. Therefore, this experiment divides the collection range into two groups which are 25 mg/L - 100 mg/L and 100 mg/L - 300 mg/L, respectively.

Due to the uncertainty of the noise source, it is difficult to use a linear function or threshold to perform effective filtering. In order to ensure the integrity of the image data, this experiment did not design an additional filter in the image acquisition system.

In this experiment, light source noise and salt and pepper noise caused relatively large interference to the image acquisition system. By adding a filter, it is indeed possible to effectively reduce the

interference of external environmental noise on the image system, but how to distinguish whether the signal in the image is a noise signal or an effective solution signal has become a major problem in design.

Table 11 Comparison chart in the case of different intensities and solution distances of RGB

Intensity 440nm		
R (250 mm 70mm 60 mm)	G (250 mm 70mm 60 mm)	B (250 mm 70mm 60 mm)
		
Distance 70mm		
R (390nm 440nm 475nm)	G (390nm 440nm 475nm)	B (390nm 440nm 475nm)
		

5.4.2.1 Obtained the solutions concentration range by reading GREEN value

It can be found that GREEN value in RGB is always in a stable range even under different illumination conditions and acquisition distances, while the changes of RED and BLUE are less obvious.

Table 12 Obtained the solutions concentration range by reading GREEN value

Distance	Sample concentrations	R (min)	R (max)	G (min)	G (max)	B (min)	B (max)
250 mm	25 mg/L — 100 mg/L	0	1	48	102	251	102
70 mm		0	21	34	88	242	254
60 mm		0	0	76	115	252	254

250 mm	100 mg/L — 300 mg/L	20	21	122	128	253	128
70 mm		0	0	115	129	254	254
60 mm		0	10	126	134	254	254

Table 13 Obtained the solutions concentration range by reading GREEN value

Intensity	Sample concentrations	R (min)	R (max)	G (min)	G (max)	B (min)	B (max)
390 nm	25 mg/L — 100 mg/L	0	16	37	98	220	253
440 nm	25 mg/L — 100 mg/L	0	43	22	103	210	246
390 nm	100 mg/L — 300 mg/L	0	12	112	125	253	253
440 nm	100 mg/L — 300 mg/L	0	0	118	131	254	254

The acquisition distance is 250 mm

When the concentration is between 25 mg/L - 100 mg/L, the value of GREEN ranges from 48 - 102.

When the concentration is between 100 mg/L- 300 mg/L, the value of GREEN ranges from 112 - 128.

The acquisition distance is 70 mm

When the concentration is between 25 mg/L- 100 mg/L, the value of GREEN ranges from 34 - 88.

When the concentration is between 100 mg/L- 300 mg/L, the value of GREEN ranges from 115 - 129.

The acquisition distance is 60 mm

When the concentration is between 25 mg/L- 100 mg/L, the value of GREEN ranges from 76 - 115.

When the concentration is between 100 mg/L- 300 mg/L, the value of GREEN ranges from 126 - 134.

The acquisition intensity is 390 mm

When the concentration is between 25 mg/L- 100 mg/L, the value of GREEN ranges from 37 - 98.

When the concentration is between 100 mg/L - 300 mg/L, the value of GREEN ranges from 112 - 125.

The acquisition intensity is 440 mm

When the concentration is between 25 mg/L- 100 mg/L, the value of GREEN ranges from 22 - 103.

When the concentration is between 100 mg/L- 300 mg/L, the value of GREEN ranges from 118 - 131.

From above analysis, analyze the concentration range of the solutions by collecting the value of GREEN in the image acquisition system can effectively distinguish the approximate range of solution concentration. (range A: 25 mg/L- 100 mg/L or range B: 100 mg/L- 300 mg/L).

5.4.3 Calculate the weight coefficient of RGB

Calculate the weight coefficient of RGB from experimental data.

When the intensity of UV lights is at 440 nm and the distance is at 250 mm

RGB values are 0.3：77.7：252.7 at 25 mg/L — 100 mg/L concentration.

RGB values are 20.5：125：253 at 100 mg/L — 300 mg/L concentration.

Table 14 When the intensity of UV lights is at 440nm and the distance is at 250 mm

Sample concentrations	R	G	B
25 mg/L — 100 mg/L	0.3	77.7	252.7
100 mg/L — 300 mg/L	20.5	125	253

When the intensity of UV lights is at 440 nm and the distance is at 70 mm

RGB values are 10.3：62.3：248.3 at 25 mg/L — 100 mg/L concentration.

RGB values are 0：122：254 at 100 mg/L — 300 mg/L concentration.

Table 15 When the intensity of UV lights is at 440nm and the distance is at 70 mm

Sample concentrations	R	G	B
25 mg/L — 100 mg/L	10.3	62.3	248.3
100 mg/L — 300 mg/L	0	122	254

When the intensity of UV lights is at 440nm and the distance is at 60 mm

RGB values are 0：95.3：253 at 25 mg/L — 100 mg/L concentration.

RGB values are 5：130：254 at 100 mg/L — 300 mg/L concentration.

Table 16 When the intensity of UV lights is at 440nm and the distance is at 60 mm

Sample concentrations	R	G	B
25 mg/L — 100 mg/L	0	95.3	253
100 mg/L — 300 mg/L	5	130	254

When the distance is at 60 mm and the intensity is at 390 nm

RGB values are 5.3：69.7：242.3 at 25 mg/L — 100 mg/L concentration.

RGB values are 6：118.5：253 at 100 mg/L — 300 mg/L concentration.

Table 17 When the distance is at 60 mm and the intensity is at 390nm

Sample concentrations	Values		
	R	G	B
25 mg/L — 100 mg/L	5.3	69.7	242.3
100 mg/L — 300 mg/L	6	118.5	253

When the distance is at 60 mm and the intensity is at 440 nm

RGB values are 21.7：67：230 at 25 mg/L — 100 mg/L concentration.

RGB values are 0：124.5：254 at 100 mg/L — 300 mg/L concentration.

Table 18 When the distance is at 60 mm and the intensity is at 440nm

Sample concentrations	Values		
	R	G	B
25 mg/L — 100 mg/L	21.7	67	230
100 mg/L — 300 mg/L	0	124.5	254

5.5 Design image processing module

By analyzing RGB curve of the solutions, it can be found that they are basically conforms to the linear law, so the RGB function of images can be analyzed according to the linear law. As shown in Figure 74 is algorithm flow of the system, first set acquisition proportion of RGB according to the external acquisition environment, then determine the range of solutions by RGB ratio, finally calculate the concentration value according to the different algorithms and RGB value.

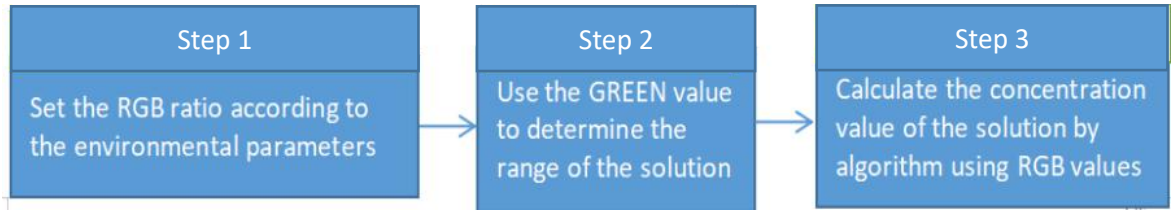


Figure 74 The algorithm design of the system

Step 1 Set the RGB ratio according to the environmental parameters

$$Blue\_ratio = \frac{Blue}{total\_colour}$$

$$Green\_ratio = \frac{Green}{total\_colour}$$

$$\mathrm{Re}d\_ratio = \frac{\mathrm{Re}d}{total\_colour}$$

Step 2 Use the GREEN value to determine the range of the solution

$$con = \begin{cases} 25 < con < 100: \\ \min\_green < green\_value < \max\_green \\ 100 < con < 300: \\ \min\_green < green\_value < \max\_green \end{cases}$$

Step 3 Calculate the concentration value of the solution by algorithm using RGB values

$$Blue = conL + \frac{conH - conL}{blueH - blueL} \times \mathrm{read}\_blue\_value$$

$$Green = conL + \frac{conH - conL}{greenH - greenL} \times \mathrm{read}\_green\_value$$

$$\mathrm{Re}d = conL + \frac{conH - conL}{redH - redL} \times \mathrm{read}\_red\_value$$

5.5.1 Configure RGB weight values according to different experimental environments

Analyze RGB color through experimental data:

$$Blue\_ratio = \frac{Blue}{total\_colour}$$

$$Green\_ratio = \frac{Green}{total\_colour}$$

$$\mathrm{Re}d\_ratio = \frac{\mathrm{Re}d}{total\_colour}$$

As different concentrations of testing solutions will cause different changes in color, it is necessary to perform weighting calculation according to the reading range of RGB value. The specific weighting method is shown in Table 19 and Table 20.

Table 19 The weighting method

	25 mg/L- 100 mg/L			
Intensity	red	green	blue	Total_colour
390nm	5.3/(5.3+69.7+242.3) =1.67%	69.7/(5.3+69.7+242.3) =21.97%	242.3/(5.3+69.7+242.3) =76.36%	5.3+69.7+242.3 =317.3
440nm	21.7/(21.7+67+230) =6.81%	67/(21.7+67+230) =21.02%	230/(21.7+67+230) =72.17%	21.7+67+230 =318.7
Distance	red	green	blue	Total_colour
250mm	0.3/(0.3+77.7+252.7) =0.09%	77.7/(0.3+77.7+252.7) =23.50%	252.7/(0.3+77.7+252.7) =76.41%	0.3+77.7+252.7 =330.7
70mm	10.3/(10.3+62.3+248.3) =3.21%	62.3/(10.3+62.3+248.3) =19.41%	248.3/(10.3+62.3+248.3) =77.38%	10.3+62.3+248.3 =320.9
60mm	0/(0+95.3+253) =0	95.3/(0+95.3+253) =27.36%	253/(0+95.3+253) =72.64%	0+95.3+253 =348.3

Table 20 The weighting method

	100 mg/L- 300 mg/L			
Intensity	red	green	blue	Total_colour
390nm	6/(6+118.5+253) =1.59%	118.5/(6+118.5+253) =31.39%	253/(6+118.5+253) =67.02%	6+118.5+253 =377.5
440nm	0/(0+124.5+254) =0	124.5/(0+124.5+254) =32.89%	254/(0+124.5+254) =67.12%	0+124.5+254 =378.5
Distance	red	green	blue	Total_colour
250mm	20.5/(20.5+125+253) =5.14%	125/(20.5+125+253) =31.37%	253/(20.5+125+253) =63.49%	20.5+125+253 =398.5
70mm	0/(0+122+254) =0	122/(0+122+254) =32.45%	254/(0+122+254) =67.55%	0+122+254 =376
60mm	5/(5+130+254) =1.29%	130/(5+130+254) =33.42%	254/(5+130+254) =65.30%	5+130+254 =389

When the acquisition distance is at 250 mm and intensity is at 440 nm

$$con = \begin{cases} 25 < con < 100: \\ 48 < green\_value < 102 \\ 100 < con < 300: \\ 112 < green\_value < 128 \end{cases}$$

When the acquisition distance is at 70 mm and intensity is at 440 nm

$$con = \begin{cases} 25 < con < 100: \\ 34 < green\_value < 88 \\ 100 < con < 300: \\ 115 < green\_value < 129 \end{cases}$$

When the acquisition distance is at 60 mm and intensity is at 440 nm

$$con = \begin{cases} 25 < con < 100: \\ 76 < green\_value < 115 \\ 100 < con < 300: \\ 126 < green\_value < 134 \end{cases}$$

When the acquisition intensity is at 390 nm and distance is at 70 mm

$$con = \begin{cases} 25 < con < 100: \\ 37 < green\_value < 98 \\ 100 < con < 300: \\ 112 < green\_value < 125 \end{cases}$$

When the acquisition intensity is at 440 nm and distance is at 70 mm

$$con = \begin{cases} 25 < con < 100: \\ 22 < green\_value < 103 \\ 100 < con < 300: \\ 118 < green\_value < 131 \end{cases}$$

By weighting calculation, the effect of different colors changes at different concentrations on the linear recognition curve is reduced, therefore the calculation equation for linear recognition curve is shown below.

$$Blue = conL + \frac{conH - conL}{blueH - blueL} \times \text{read}\_blue\_value$$

$$Green = conL + \frac{conH - conL}{greenH - greenL} \times \text{read}\_green\_value$$

$$\text{Re}\,d = conL + \frac{conH - conL}{redH - redL} \times \text{read}\_red\_value$$

$$con = \begin{cases} 25 < con < 100: \\ [Blue] \times Blue\_ratio + [Green] \times \text{Green}\_ratio + [\text{Re}\,d] \times \text{Re}\,d\_ratio \\ 100 < con < 300: \\ [Blue] \times Blue\_ratio + [Green] \times \text{Green}\_ratio + [\text{Re}\,d] \times \text{Re}\,d\_ratio \end{cases}$$

When the acquisition distance is at 60 mm and intensity is at 440 nm

$$con = \begin{cases} 25 < con < 100: \\ [25 + \dfrac{100-25}{254-252} \times \text{read}\_blue\_value] \times 72.64\% + [25 + \dfrac{100-25}{115-76} \times \text{read}\_green\_value] \times 27.36\% \\ \\ 100 < con < 300: \\ [100 + \dfrac{300-100}{254-254} \times \text{read}\_blue\_value] \times 65.3\% + [100 + \dfrac{300-100}{134-126} \times \text{read}\_green\_value] \times 33.42\% \\ + [100 + \dfrac{300-100}{10-0} \times \text{read}\_red\_value] \times 1.29\% \end{cases}$$

When the acquisition distance is at 70 mm and intensity is at 440 nm

$$con = \begin{cases} 25 < con < 100: \\ [25 + \dfrac{100-25}{254-242} \times \text{read}\_blue\_value] \times 77.38\% + [25 + \dfrac{100-25}{88-34} \times \text{read}\_green\_value] \times 19.41\% + \\ [25 + \dfrac{100-25}{21-0} \times \text{read}\_red\_value] \times 3.21\% \\ \\ 100 < con < 300: \\ [100 + \dfrac{300-100}{254-254} \times \text{read}\_blue\_value] \times 67.55\% + [100 + \dfrac{300-100}{129-115} \times \text{read}\_green\_value] \times 32.45\% \end{cases}$$

When the acquisition distance is at 250 mm and intensity is at 440 nm

$$con = \begin{cases} 25 < con < 100: \\ [25 + \dfrac{100-25}{251-102} \times \text{read}\_blue\_value] \times 76.41\% + [25 + \dfrac{100-25}{102-48} \times \text{read}\_green\_value] \times 23.5\% + \\ [25 + \dfrac{100-25}{1-0} \times \text{read}\_red\_value] \times 0.09\% \\ \\ 100 < con < 300: \\ [100 + \dfrac{300-100}{253-128} \times \text{read}\_blue\_value] \times 63.49\% + [100 + \dfrac{300-100}{128-122} \times \text{read}\_green\_value] \times 31.37\% \\ + [100 + \dfrac{300-100}{21-20} \times \text{read}\_red\_value] \times 5.14\% \end{cases}$$

When the acquisition intensity is at 390 nm and distance is at 70 mm

$$con = \begin{cases} 25 < con < 100: \\ [25 + \frac{100-25}{253-220} \times \text{read}\_blue\_value] \times 76.36\% + [25 + \frac{100-25}{98-37} \times \text{read}\_green\_value] \times 21.97\% + \\ [25 + \frac{100-25}{16-0} \times \text{read}\_red\_value] \times 1.67\% \\ \\ 100 < con < 300: \\ [100 + \frac{300-100}{253-253} \times \text{read}\_blue\_value] \times 67.02\% + [100 + \frac{300-100}{125-112} \times \text{read}\_green\_value] \times 31.39\% \\ + [100 + \frac{300-100}{12-0} \times \text{read}\_red\_value] \times 1.59\% \end{cases}$$

When the acquisition intensity is at 440nm and distance is at 70 mm

$$con = \begin{cases} 25 < con < 100: \\ [25 + \frac{100-25}{246-210} \times \text{read}\_blue\_value] \times 72.17\% + [25 + \frac{100-25}{103-22} \times \text{read}\_green\_value] \times 21.02\% + \\ [25 + \frac{100-25}{43-0} \times \text{read}\_red\_value] \times 6.81\% \\ \\ 100 < con < 300: \\ [100 + \frac{300-100}{254-254} \times \text{read}\_blue\_value] \times 67.12\% + [100 + \frac{300-100}{131-118} \times \text{read}\_green\_value] \times 32.89\% \end{cases}$$

5.5.2 Determine the range of solution concentration based on GREEN pixel value

Table 21 Determine the range of solution concentration based on GREEN pixel value

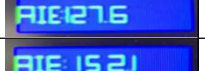
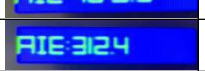
	If GREEN Value	Algorithms
Distance		
60 mm	$76 < green\_value < 115$	$[25 + 37.5 \times read\_blue\_value] \times 72.64\% + [25 + 1.92 \times read\_green\_value] \times 27.36\%$
	$126 < green\_value < 134$	$[100 + 25 \times read\_green\_value] \times 33.42\% + [100 + 20 \times read\_red\_value] \times 1.29\%$
70 mm	$34 < green\_value < 88$	$[25 + 6.25 \times read\_blue\_value] \times 77.38\% + [25 + 1.39 \times read\_green\_value] \times 19.41\% + [25 + 3.57 \times read\_red\_value] \times 3.21\%$
	$115 < green\_value < 129$	$[100 + 14.29 \times read\_green\_value] \times 32.45\%$
250 mm	$48 < green\_value < 102$	$[25 + 0.5 \times read\_blue\_value] \times 76.41\% + [25 + 1.39 \times read\_green\_value] \times 23.5\% + [25 + 75 \times read\_red\_value] \times 0.09\%$
	$112 < green\_value < 128$	$[100 + 1.6 \times read\_blue\_value] \times 63.49\% + [100 + 33.33 \times read\_green\_value] \times 31.37\% + [100 + 200 \times read\_red\_value] \times 5.14\%$
Intensity		

390 mm	$37 < green\_value < 98$	$[25+2.27\times read\_blue\_value]\times 76.36\%+[25+1.23\times read\_green\_value]\times 21.97\%$ $+[25+4.69\times read\_red\_value]\times 1.67\%$
	$112 < green\_value < 125$	$[100+15.38\times read\_green\_value]\times 31.39\%+[100+16.67\times read\_red\_value]\times 1.59\%$
440 mm	$22 < green\_value < 103$	$[25+2.08\times read\_blue\_value]\times 72.17\%+[25+0.93\times read\_green\_value]\times 21.02\%$ $+[25+1.74\times read\_red\_value]\times 6.81\%$
	$118 < green\_value < 131$	$[100+15.38\times read\_green\_value]\times 32.89\%$

5.6 Verify the accuracy of the entire system

According the previous algorithm design, the concentration value of testing solutions can be identified within a certain range. As shown in Table 23, the concentration value of testing solutions configuration and solution concentration value recognized by FPGA identification system found that the concentration of solution does not change much. Meanwhile, the change of RGB value with the concentration of solution is small, so FPGA system cannot accurately recognize the change in the solution. Each group of solutions has been tested twice. After testing, it can be found that the concentration range of the solution is recognized by FPGA identification system, so the concentration range is the accuracy of FPGA identification system.

Table 23 The identification system

Solution concentration	Actual solution concentration	VGA show result	R	G	B
25 mg/L	21.4 mg/L		40	21	212
	25.9 mg/L		38	18	219
75 mg/L	63.2 mg/L		25	17	234
	43.2 mg/L		31	15	226
100 mg/L	127.6 mg/L		0	99	239
	152.1 mg/L		0	102	247
200 mg/L	221.4 mg/L		0	121	255
	189.3 mg/L		0	113	255
300 mg/L	321.4 mg/L		0	135	254
	298.2 mg/L		0	12	254

Thus, the recognition range of the testing solution recognition system is shown in Table 24.

When testing solution is 25 mg/L, the accuracy of the image recognition system is 3.6.

When testing solution is 75 mg/L, the accuracy of the image recognition system is 31.8.

When testing solution is 100 mg/L, the accuracy of the image recognition system is 52.1.

When testing solution is 200 mg/L, the accuracy of the image recognition system is 21.7.

When testing solution is 300 mg/L, the accuracy of the image recognition system is 21.4.

It can be found that when the range of testing solution is between 75 mg/L - 200 mg/L, the recognition degree of the system is low, and significant recognition error will occur.

When the range of testing solution is less than 75 mg/L or greater than 300 mg/L, the recognition of the system is higher, and the recognition degree of the system is about 25. The main reason is that the experiment solutions are too white in the low concentration, which the image system cannot be accurately identified.

Table 24 The accuracy of recognition

Solution concentration	Recognition range	Accuracy of recognition
25 mg/L	21.4 mg/L - 25.9 mg/L	3.6
75 mg/L	43.2 mg/L - 63.2 mg/L	31.8
100 mg/L	127.6 mg/L - 152.1 mg/L	52.1
200 mg/L	189.3 mg/L - 221.4 mg/L	21.7
300 mg/L	298.2 mg/L - 321.4 mg/L	21.4

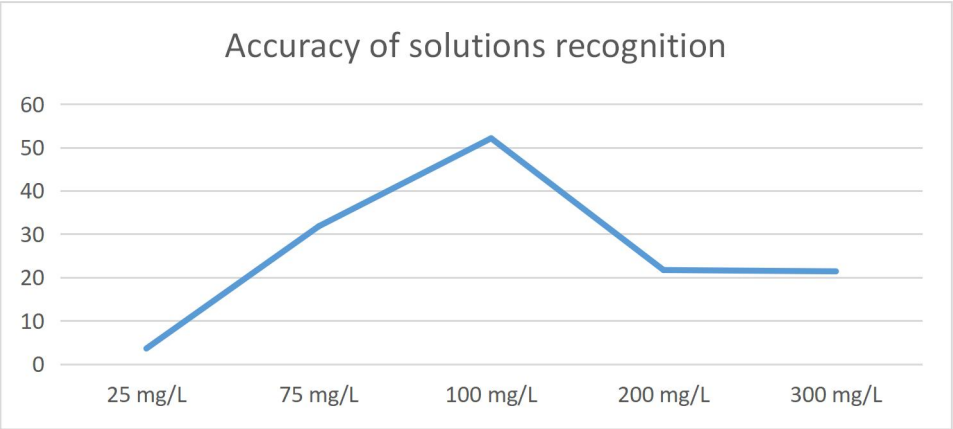


Figure 75 Linear diagram of the accuracy of recognition

6. Future work

6.1 Change the AMP value of design to reduce the overexposure problem

In the image acquisition system, the setting of the color gain is a necessary acquisition parameter. Image acquisition process is to convert analog signals to digital signals, and setting reasonable value can ensure that the image does not appear distorted in the display system.

It can be found through experiments that when the concentration of the solution is greater than 100 mg / L, the image system will be in an overexposed state. Because the noise of the light source caused by overexposure will affect the display quality of the image. The color gain can be adjusted through the internal registers of camera module. This reduces the impact of overexposure on the image acquisition system.

According to the RGB curve of the experimental solution, it can be found that the blue value has the largest influence on the concentration, and the red value has the smallest influence on the concentration. In this experiment, the light intensity of the ultraviolet light emitting device is between 390 nm and 470 nm. Because the absorption frequencies of blue light and red light are between 450-495 nm and 620-750 nm, thus, by adjusting the internal registers in camera module, the gain of blue light can be increased and the gain of red light can be reduced. When the gain of blue light is increased, the change of the blue curve is more significant, but the change of the red curve is not significant. The color gain can be adjusted effectively by adjusting the color gain, but this will obviously reduce the display quality of the image in the display system. For example, when the gain of blue light is increased, the VGA display will tend to be blue.

6.2 Add the optical filter to eliminate the unwanted light.

In this experiment, light source noise and salt and pepper noise caused relatively large interference to the image acquisition system. By adding a filter, it is indeed possible to effectively reduce the interference of external environmental noise on the image system, but how to distinguish whether the signal in the image is a noise signal or an effective solution signal has become a major problem in design.

It can be found through experiments that a certain recognition rate has been achieved through the image recognition system, although a black box was designed to avoid the influence of external light sources on the entire experiment. However, the instability of the external environment will still cause certain data fluctuations. By adding a filter in front of the camera, the effect of external light source noise on the experiment can be effectively reduced. In actual experiments, a filter provided by the laboratory was used to remove external noise, but because this filter would cause a certain loss of the image signal of the actual solution, it was not used in the entire design.

6.3 Place the image acquisition system in a 0 ° C storage environment to prevent the solution from evaporating and change the concentration of the solution

The solution in this experiment is Ethanol solution, which has a certain volatility. I usually put the solution in a laboratory refrigerator and at a temperature of zero degrees to prevent the Ethanol solution from volatilizing, and avoid leading to errors in the solution concentration. During the acquisition process, the acquisition method can be used on demand, which reduce the interference of the external environment on the overall solution concentration.

Although this experiment reduced the exposure time of the solution at room temperature as much as possible, it will inevitably have a certain impact, because the entire imaging system needs to collect data for the concentration of each group of solutions multiple times, so it is inevitable to introduce additional Error, that is, because the solution is exposed to the external environment for too long, this will result in a decrease in the concentration of the solution. I suppose after the entire image system is established, both the solution and image processing system can be placed in a laboratory refrigerator at 0 degrees to prevent the solution volatilization and reduce the affect on the experimental results.

6.4 Increase the number of samples in the image recognition system and improve the stability of the entire system

In this experiment, our team designed an acquisition box for image acquisition to reduce the external environment's interference to the acquisition system. Therefore, fixing the solution in the middle of the acquisition box can ensure that the acquisition center of the image acquisition system is the center point of the solution.

Because the interference of external noise will cause certain instability of pixels, it is possible to increase the image collection points to reduce the impact of the external noise on the image recognition system.

The method of collecting more image data to obtain the average value can effectively improve the stable value of data, but it requires more processing resources. So this experiment did not involve that.

6.5 Redesign the image acquisition module

According to the RGB curves of the experiment solutions, it can be found that blue value has the greatest influence on the concentrations, and red value has the smallest influence on the concentrations. In this experiment, UV lights emission device has a transmitting frequency of 300Mhz, as the absorption frequency of blue and red light is 300Mhz and 200Mhz, the gain of blue light can be enhanced and also the gain of red light can be reduced by modifying the internal registers in camera module. When the gain of blue light is increased, the change of the blue curve is more significant, however the change of the red curve is not significant.

Redesign interpolation algorithm (Single colour weighting algorithm)

According to the change trend of the solutions in this experiment, green and red colour are the most significant. Single colour weighting algorithm is able to significant green colour, which can get more effective data, and also more resources will be taken for calculate green colour in image system. As

Figure 75 shows.

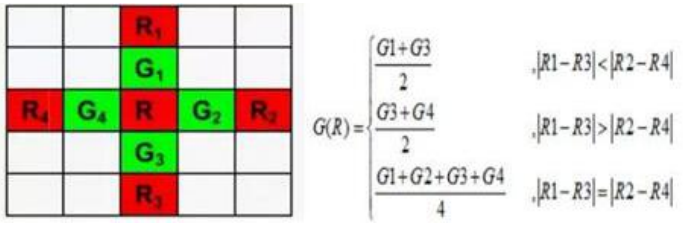


Figure 75 Single colour weighting algorithm

The linear interpolation algorithm in this experiment can only be used when image quality does not require high. However, single colour weighting algorithm can increase the effective value of RGB.

6.6 Improve the algorithm of the image processing module

Through experiments, it can be found that the accuracy of FPGA identification system cannot reach 1 mg/L, the main reason is that camera module first performs filtering processing after collecting the image information of Bayer format, then FPGA processing unit performs algorithm. Because of the limitations of RGB algorithm, the complete information of image cannot be represented. By using YUV format to capture image is an optimized design in future work.

The advantage of YUV format is that it does not have significant fluctuation in the overall experimental results due to the effects of light intensity. Therefore, YUV format in image processing may be better than RGB format in image processing. In addition, collecting color components of RED, GREEN, and BLUE by designing three different cameras, then transfer them to FPGA processing unit through these three different camera modules, so that FPGA identification system can acquire more effective information of solution images, thereby increasing the accuracy of the system

6.7 Optimize user interface to complete the image system

When no button is pressed, FPGA identification system is in image acquisition state, which camera module collects RGB value and outputs it to display through VGA port. When a button is pressed, FPGA identification system is in solution concentration recognition state, which FPGA processing unit analyzes and calculates the concentration of solution by RGB value collected from camera.

It can be found that FPGA identification system has no other functions. There are also no sufficient information provided to user in display interface. By improving display system of FPGA, add user

prompts in display, and guide user to operate FPGA solution identification system can be improve in future work.

Through the analysis of the experiment, it can be found that many parameters of camera and external light source have a certain influence on RGB value. It is better that users are able to change some important parameter settings about camera module, such as exposure, gain and aperture settings by pressing the button, instead of pre-setting according to the laboratory environment. When laboratory environment or external environment changes, user can directly adjust parameters of camera by pressing buttons to obtain the best image quality and improve FPGA identification system.

Because the image acquisition system needs certain portability and includes image acquisition, processing and display. Therefore, in the early stage of the experiment, I used the Quarts software software to verify whether the data of the image acquisition system was accurately recorded in the processor. When the test is completed, I can directly observe the RGB data at different concentrations through the VGA display module. The method of displaying the solution image by software is not involved in this experiment. The main reason is that additional programming is required, also it does not meet the requirements of system portability.

The display module of the image acquisition system in this experiment was processed by VGA display module. The main advantage of using Dell series of VGA displays is the ease of image display. In a portable image acquisition system, LCD display module has better display performance and can be perfectly compatible with a portable image acquisition system

6.8 Design PCB board to remove unnecessary modules on the FPGA to increase portability

The system has certain limitations. Firstly, the image information is output to display system through VGA interface, this operation method is simple but obviously takes up a lot of CPU resources and also poor in portability. However, replace VGA display screen by using an LCD is an optimized design. User can modify parameter configuration of camera and the identification of the concentration of solution by touching LCD display. This can increase the portability of the system.

7.Conclusions

This experiment developed a potable, convenient and affordable home-based medical devices for CKD monitoring. In the black box experiment environment, use ultraviolet light to excite the testing cuvette, the solution of urine mixed with Human Serum Albumin (HSA) will generate fluorescent light after being excited by UV light. Then use camera to record the level of fluorescence. After image processing of micro controller FPGA, the correlation between UV light intensity and HSA concentration will be determined. The medical device in this project is low cost, efficiently, reliably, sensitive, fast, user-friendly, and is expected to help users to monitor early stage of chronic kidney disease.

In the image processing system, the processed data is large, and the processing speed is required to be fast, which is suitable for FPGA to achieve. The biggest feature of FPGA structure is its flexible structure and strong versatility. It is suitable for modular design, which can improve the efficiency of calculation and processing. Moreover, the development cycle is short, easy to maintain and expand, and suitable for image processing.

Due to the parallel processing capabilities of FPGA, its advantages in image processing are becoming more and more obvious. Therefore, the image acquisition and processing system with FPGA as core device can make full use of parallel processing capability of FPGA. Thus, this project achieved camera image acquisition and processing technology based on FPGA. The main work contents are as follows:

1) FPGA based image acquisition platform was designed.

2) The corresponding hardware logic design was implemented for image acquisition platform, real-time capture, storage, VGA display and serial communication of camera images.

3) Algorithm design divide pixel values of GREEN and calculate the concentration of the solutions by RGB value.

Although adapting the desirable feature - ASSURE in terms of Affordable material and accessible manufacturing methods, remarkable Sensitivity and Selectivity to human serum albumin, User

friendly without or with minimal steps for training and utilisation, Rapid and robust for providing result, and Deliverable to end-user, the current prototype still has some weakness and requires further examination to guarantee the precision of the final results, as well as to find out whether the design would encounter any other failure. Furthermore, this project has shown the promising future with many options for improvement to bring the device into practical utilisation.

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Appendix 1

Camera D5M feature set is listed below [14]:

1. High frame rate

2. Superior low-light performance

3. Low dark current

4. Global reset release, which starts the exposure of all rows simultaneously

5. Bulb exposure mode, for arbitrary exposure times

6. Snapshot mode to take frames on demand

7. Horizontal and vertical mirror image

8. Column and row skip modes to reduce image size without reducing field-of-view

9. Column and row binning modes to improve image quality when resizing

10. Simple two-wire serial interface

11. Programmable controls: gain, frame rate, frame size, exposure

12. Automatic black level calibration

13. On-chip PLL

Key Performance Parameters:

Parameter		*Value*
Active pixels		2,592H x 1,944V
Pixel size		2.2µm x 2.2µm
Color filter array		RGB Bayer pattern
Shutter type		Global reset release (GRR),
Maximum data rate/master		96 Mp/s at 96 MHz
Frame rate	Full resolution	Programmable up to 15 fps
	VGA (640 x 480)	Programmable up to 70 fps
ADC resolution		12-bit
Responsivity		1.4 V/lux-sec (550nm)
Pixel dynamic range		70.1dB
SNRMAX		38.1dB
Supply Voltage	Power	3.3V
	I/O	1.7V～3.1V

Appendix 2

FEATURES[14]:

330 MSPS throughput rate

Triple 10-bit digital-to-analog converters (DACs)

SFDR

−70 dB at fCLK = 50 MHz; fOUT = 1 MHz

−53 dB at fCLK = 140 MHz; fOUT = 40 MHz

RS-343A-/RS-170-compatible output

Complementary outputs

DAC output current range: 2.0 mA to 26.5 mA

TTL-compatible inputs

Internal reference (1.235 V)

Single-supply 5 V/3.3 V operation 48-lead LQFP package

Low power dissipation (30 mW minimum @ 3 V)

Low power standby mode (6 mW typical @ 3 V)

Industrial temperature range (−40° C to +85° C)

Pb-free (lead-free) package

VGA CMOS, 330 MHz Triple 10-Bit High Speed Video DAC (ADV7123):

Appendix 3

DE1-SoC board (FPGA) [14]

Altera Cyclone® V SE 5CSEMA5F31C6N device

Altera Serial Configuration device – EPCQ256

USB Blaster II (on board) for programming; JTAG Mode

64MB SDRAM (16-bit data bus)

4 Push-buttons

10 Slide switches

10 Red user LEDs

Six 7-segment displays

Four 50MHz clock sources from clock generator

24-bit CD-quality audio CODEC with line-in, line-out, and microphone-in jacks

VGA DAC (8-bit high-speed triple DACs) with VGA-out connector

TV Decoder (NTSC/PAL/SECAM) and TV-in connector

PS/2 mouse/keyboard connector

IR receiver and IR emitter

Two 40-pin Expansion Header with diode protection

A/D Converter, 4-pin SPI interface with FPGA

HPS (Hard Processor System) [14]

800MHz Dual-core ARM Cortex-A9 MPCore processor

1GB DDR3 SDRAM (32-bit data bus)

1 Gigabit Ethernet PHY with RJ45 connector

2-port USB Host, Normal Type-A USB connector

Micro SD card socket

Accelerometer (I2C interface + interrupt)

UART to USB, USB Mini-B connector

Warm reset button and cold reset button

One user button and one user LED

LTC 2x7 expansion header