Towards a Polymeric Vertical Transistor

by

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Declaration

I certify that this thesis does not incorporate without acknowledgment any material previously submitted for a degree or diploma in any university; and that to the best of my knowledge and belief it does not contain any material previously published or written by another person except where due reference is made in the text.

Signature_____

Daniel Gruszecki

November 2016

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I am blessed to have some exceptional women in my life who need my dearest thanks, like my sister, Eliza who always believed and wanted to know more. My mother, Grazyna who has done all I could ever hope for. And finally Bonnie, for all your encouragement and belief, this really would have been impossible without you.

I feel so fortunate to be here, science is an incredible adventure and ultimately I'm left excited about all that has been done and all that is still to come.

Abstract

The role and purpose of this work is to investigate a new vertical transistor structure that does not require the use of lithography and can be fabricated in ambient conditions using solution processed active layers. Towards this, planar transistor structures are studied featuring organic semiconducting active layers. Solution processed films are seen to produce devices with comparable or improved device behaviour in comparison to physically deposited active layers. Showing solution processed devices are capable of producing/being used in high performance field effect devices. However, inherent shortcomings in planar structures such as parasitic contact resistances and device scaling due to lithographic resolutions ultimately limit the performance of planar devices. This result provides motivation to develop a vertical transistor structure that features dimensions controlled by the thickness of a solution processed film and large operational areas, in an effort to improve the prospects of organic transistor devices.

Essential to the structure is fabrication of two terminal vertical devices on plastic substrates. The unique mechanical properties of plastic allow non-traditional device architectures to be investigated. A UV-NVS protective layer is required to protect the underlying substrate from solvent induced stress cracking allowing the deposition of polymeric films out of solvent solution on polycarbonate substrates. The yield of devices was seen to be dependent on the electrode composition, deposition method and area of the electrode. Optimised devices were produced featuring the p-type semiconducting material P3HT. Formed at the interface between P3HT/Al Schottky diode devices were investigated and seen to display variation in current-voltage behaviour with respect to time. Devices that were stored under vacuum for 20 hours were seen to have significantly less variation in current-voltage behaviour. Ultimately, device yields of at least 75% were obtained for optimised thin film polymeric devices on polycarbonate.

Cutting methods capable of commercial scale fabrication such as hot scalpel scoring, scissor cutting, ion beam milling and machine cutting were investigated to

introduce a vertical wall into two terminal device substrates. The resulting architecture can be used to create an interface between the semiconducting polymer and a dielectric film allowing for a vertical transistor structure to be realised. CNC machine cutting shows the most promise as a methodology allowing for a 45° angle cut surface to be formed in the device. A limitation in the method is delamination between the polymeric film and the electrode, and the electrode and substrate due to the lateral forces caused in the cutting action. The adhesion failures are seen to increase with feed rate velocity. With the tears resulting from cutting extending into the device operational area up to 5µm. Conductive mapping of the cut edge shows conduction through the polymer extending to the cut edge.

The solution processing of dielectrics over the machine cut edge was investigated. The failure rate of spin coated films was determined by the resistance measurements between the gate-source and gate-drain circuits. Spin speed was seen to play a key role in the formation of insulating films, with 1000RPM UV-NVS resin identified as an ideal choice due to the high resistance and ambient room temperature processing possible with the UV cured film. The fabrication of P3HT vertical transistor structures using UV-NVS was studied. Electrical performance was seen to degrade shifting to lower currents with higher diode on voltages. This degradation in performance was attributed to the ambient processing of the P3HT polymer. An encapsulating electrode was employed that greatly improved the stability of devices across fabrication.

Machine cut vertical organic field effect transistors were fabricated and electrically characterised for two modes of operation. Enhancement operation produced through the penetration of a lateral electric field into the active layer and Schottky barrier lowering at the P3HT/Al interface. Both methods of operation were simulated and were expected to see an increase in device drain current. Output characterisation did not resolve any enhancement current in the structure with the change in current falling within the standard deviation of control devices. The structure was probed for a time based enhancement formation using two time changing gate signals. The drain current during the application of the signal was measured and showed a general trend of reducing drain current with no

enhancement current observed. This trend is consistent with the device performance across fabrication and repeat testing of P3HT devices in ambient conditions. An alternative p-type polymer, PCDTBT with low intrinsic conductivity and high ambient stability was introduced into the structure to help resolve enhancement current. The changes resulted in a highly stable device capable of resolving an enhancement current on the order of nanoamps. However, electrical characterisation showed no enhancement current in the device structure suggesting the lateral field penetration depth did not meet simulated expectation.

Contents

Chapter 1

1. The Organic Field Effect Transistor

Introduction

The organic field effect transistor (OFET) is a three electrode device, whereby a capacitive electric field at the gate electrode, (G) effectively acts as a switch, determining the ability for current to pass between the source (S) and drain (D) electrodes. This function is controlled through modulation of the voltage at the gate which forms a conducting channel, an area of dense charge carriers between the source and drain throughout the organic semiconducting active material. The channel has dimensions denoted width, W and length, L labelled in Figure 1.1 with charge injection occurring from the source electrode into the semiconductor. The common arrangement of these electrodes with respect to a substrate and a dielectric functional film (necessarily paired with the gate electrode to form the capacitive field effect) is shown in Figure 1.1.

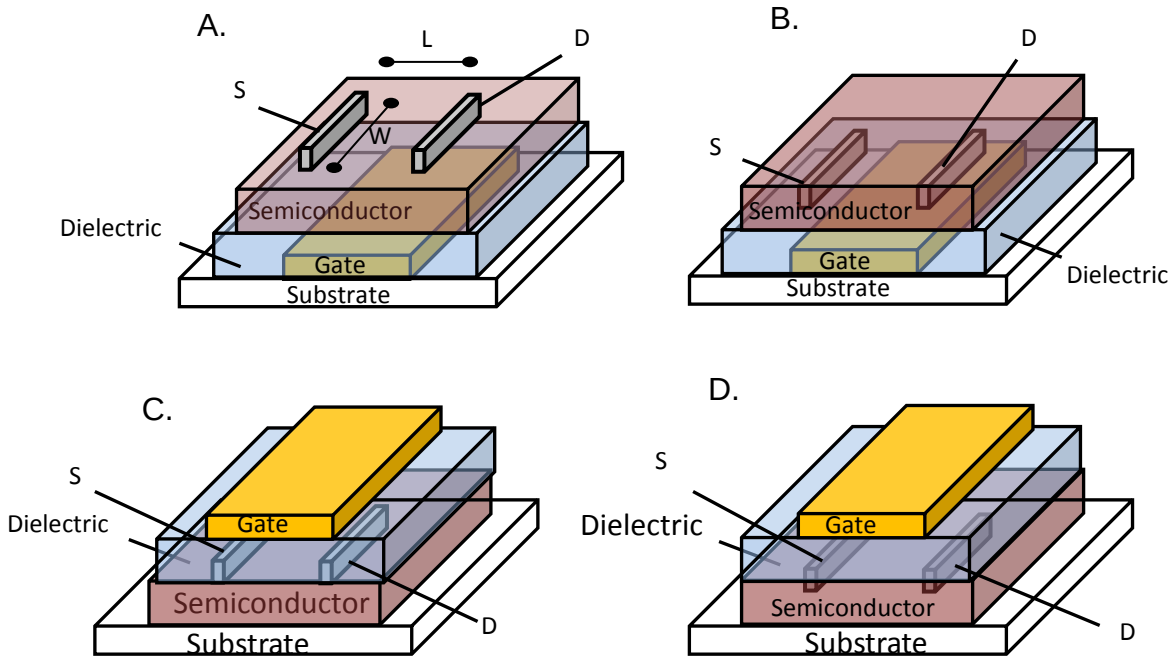

Figure 1.1. Schematic of planar OFET device geometries. The geometry of the device is described through the position of the S-D contacts relative to the gate electrode (described as either top contact or bottom contact) and the positioning of the source drain electrodes relative to the active channel (described as either co-planar or staggered) A. Staggered top contact, bottom gate device B. Coplanar bottom contact, bottom gate C. Coplanar bottom contact, top gate device D. Staggered top contact, top gate device.

It's the switching property of field effect transistors that provides an essential function in complementary metal oxide semiconductor (CMOS) circuits. CMOS circuits feature in microprocessors and random access memory (RAM).[4, 5] These circuits operate at fixed voltage levels corresponding to two values 0 (low) or 1 (high) creating a binary value system.[6] Essential for digital logic is the CMOS inverter circuit seen in Figure 1.2. The circuit contains a PMOS (p-type metal oxide semiconductor FET) and NMOS (n-type metal oxide semiconductor FET) connected at the gate and drain terminals such that If the applied input is high(1) the output will be low(0) and vice versa.[6] The inverter circuit forms the basis for NAND flash memory which will be discussed later.

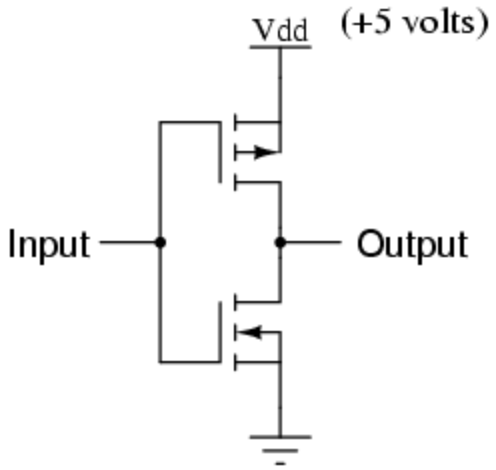

Figure 1.2.CMOS Inverter logic circuit. The logic circuit operates utilising an p-type FET (top) and an n-type FET (bottom). The circuit is the basis for digital logic circuits. The power usage and speed of transistors in the circuit is a key performance criteria in logic applications determining

Key to the operation of the circuit is the semiconducting material which under applied gate bias reduces in electrical resistance and produces a conduction path which allows for effective switching of the device from the OFF state to the ON state under an applied gate potential.[7] High purity silicon is commonly selected due to its ability to be doped providing control over its electrical properties and has created an electronics industry all to itself.[8] In recent years devices featuring organic semiconductor active layers have gained significant interest in circuit applications, with the performance metric, μ, the field effect mobility performance exceeding silicon with the highest being the p-type rubrene, a small vacuum-evaporated molecule with $\mu = 20 cm^2.V^{-1}$ at room temperature.[2, 9] and the solution

processable n-type polymer (NDI2OD-T2) with mobility μ= 0.85cm^2.V^{-1}.[10] These values compare favourably with amorphous silicon which has μ= 1.0cm^2.V^{-1}.[11] And provides commercial interest in pursuing devices such as RFID,[12, 13] electronic paper displays,[14], LEDs,[15] bioanalysers[16] and complimentary circuits,[17-19] featuring organic semiconducting materials. Organic semiconductor technology is a new and exciting field with many fundamental questions on the nature of organic semiconductor materials and the governing physics of devices containing organics. In order to establish governing theory of semiconductors and devices based on semiconductors density of states theory and metal-semiconductor junction theory will be presented.

1.1 Semiconductor Materials

Semiconductor materials are amorphous or crystalline solids providing electrical properties between that of an insulator or conductor. The description of semi conduction relies on the packing of electronic charge carriers, electrons and holes in energy levels with respect to the Fermi level of the bulk material. With the Fermi level the energy level with a 50% probability of being occupied at a given temperature.[20] With increasing atom density, energy states converge to a band structure model due to the superposition of electron wave functions for a solid material.[21] The band structure of a solid has an infinite amount of bands, with the density of states (DOS) providing a measure of the number of states per energy, per volume of a given solid system. A high DOS of states means a large number of states at an available energy level.

Many energy bands are of high energy and are metastable, just as some energy bands are of low energy and associated with core electrons. The electronic properties of materials are described by the bands nearest the Fermi level of a solid and labelled the valence and vacuum band, respectively. The energy difference between the top of the valence band and the conduction band is known as the bandgap, E_g. In insulators (Figure 1.3A) their generally exists a significant band gap

energy preventing promotion of electrons into the conduction band resulting in insulating properties.[21]The Fermi level for semiconducting materials resides within a band gap. Which, dependent on the position of the Fermi level with respect to the valence and vacuum band a semiconductor can be further described as, either p-type (Figure 1.3B) or n-type(Figure 1.3C).[21]With electrons referred to as the minority carrier in p-type devices and holes the minority carrier in n-type devices. In comparison conductors feature an overlap between the conduction band and valence band (Figure 1.3D).

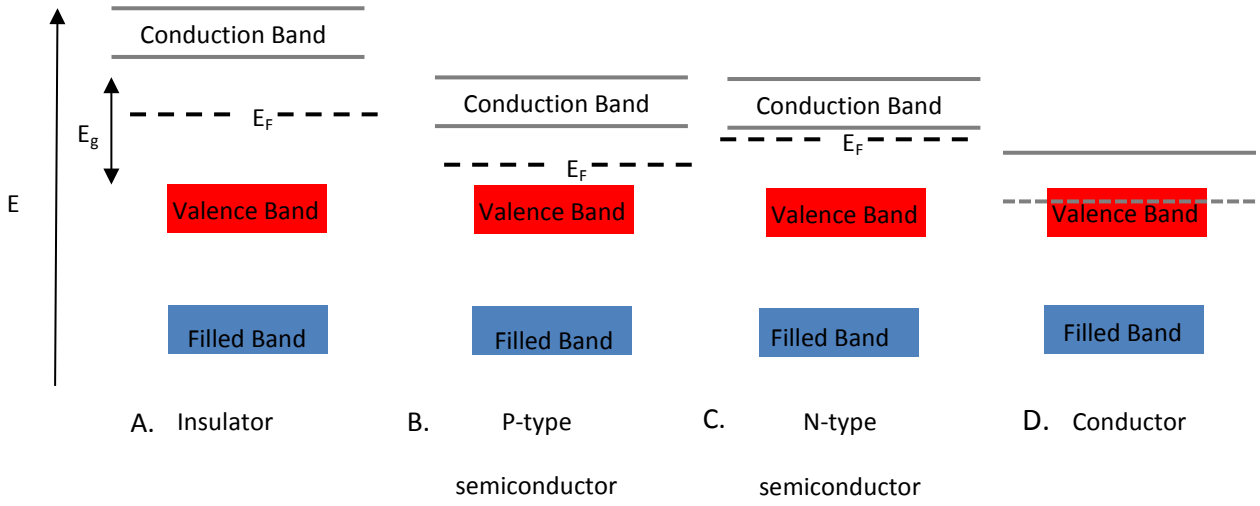

Figure 1.3. Energy band diagram describing the valance band and conductions bands in solid materials. A. Insulator material with a large band gap. B. Semiconductor with a small band gap and the Fermi energy situated mid gap and C. Conductor material with an overlap of valence and electron bands.

1.1.1 P-N Junction

To understand the behaviour of semiconductor devices it is necessary to study the behaviour of charges near a surface or interface. When two semiconductor materials, a p-type and an n-type form an interface, a P-N junction is formed. P-N junctions see extensive use in diodes, solar cells and CMOS technology and are formed at the interface between a p-type and n-type semiconductor when they are brought into contact. The chemical potential drives majority charge carriers to diffuse across the interface with positive charges from the p-type material

recombining with negative charges from the n-type material. This creates a region deplete of charge carriers known as the depletion zone seen in Figure 1.4A at thermal equilibrium. The depletion zone creates a built in potential across the junction that can be controlled under applied external potential creating a rectifying junction. A junction that allows current to pass under forward biasing but not under reverse biasing conditions.

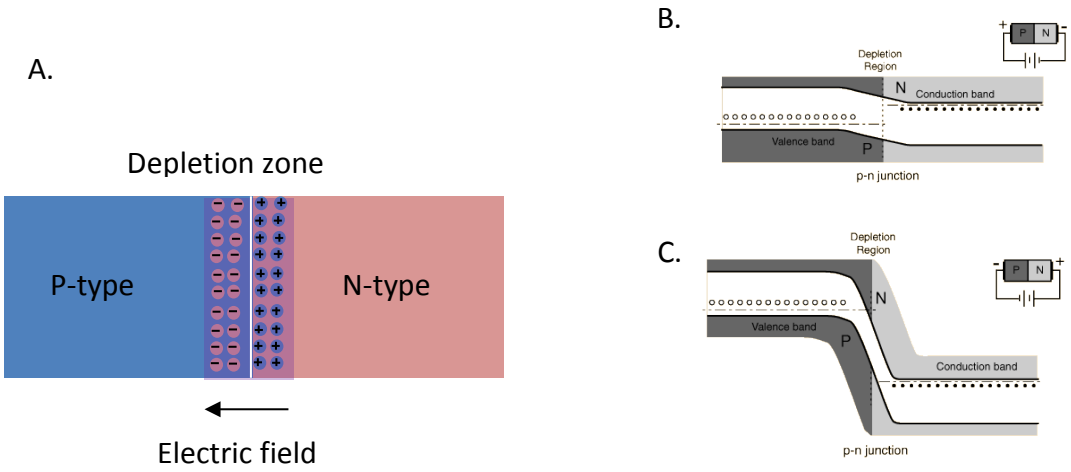

Figure 1.4. A. P-N junction between a p-type and n-type semiconductor material and the resulting rectifying junctions under applied biases. B. Under forward biasing the depletion zone contracts and produces a reduced potential resulting in a lower resistance. C. Under reverse biasing the depletion zone expands increasing the internal potential and increasing the resistance across the junction.

Under forward biasing conditions (Figure 1.4B) the p-type material is biased with a positive charge, and the n-type material a negative charge. The electromotive force increases the flow of carriers into the junction reducing the size of the depletion zone and the potential barrier at the junction. This reduction in potential reduces the resistance across the junction and increases the diffusion of majority carriers across the junction i.e. electrons crossing the junction into the p-type material and holes crossing the junction into the n-type material. However, the diffused charges do not penetrate indefinitely as recombining is energetically favourable. The flux and recombination distance for carriers ultimately determines the current and dimensions possible for the rectifying junction. Under reverse biasing (Figure 1.4C) the p-type material is connected to a negative bias and the n-type material a positive bias. The reverse biasing conditions draw charge carriers away from the junction increasing the size of the depletion zone as bias magnitude increases.

Increasing the potential barrier created at the junction and increasing the resistance across the junction and reducing current flow.[22]

1.2 Field Effect Transistor Device Operation

FETs generally function as enhancement mode devices meaning the conduction channel is created through a gate bias. Conversely a depletion mode device uses the capacitive field to close an existing conduction channel. In a p-type material as an example, current is produced by the majority charge carrier in the device charge holes (with electrons the majority charge carrier in n-type materials).[23]When a negative bias is at the gate the voltage drop over the insulator allows a conduction path to open in the semiconductor (a positive gate voltage is applied to produce a conduction channel in an n-type material). The dielectric-semiconductor interface can be visualised as two capacitor plates with equal and opposite charge. As charge carriers from the bulk semiconductor migrate to the dielectric the system is no longer in an energetic equilibrium with induced charges at the dielectric-semiconductor interface changing the Fermi level at the metal contact-semiconductor interface as a result.[23]The band bending that occurs at this interface is due to localised charge transfer over the metal electrode-semiconductor interface and is commonly described using the Mott-Schottky model.[21] This can be visualised as per Figure 1.5.

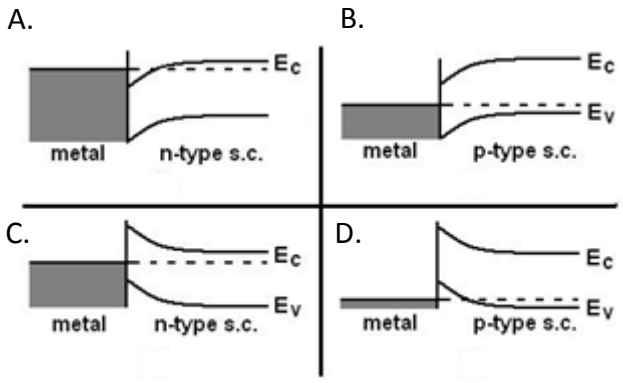

Figure 1.5. Energy level diagrams describing charge injection at the source electrode under varied electrical conditions. A. n-type material at 0 gate bias, B. p-type at 0 gate bias, C. n-type material at positive gate bias, D. p-type at negative gate bias

Charge is needed to be injected into the material from the contact to allow current flow. This injection requires an ideally ohmic contact to be formed with favourable (lower to higher work function) band bending from the metal to the semiconductor. The selection of material for contacts is as such important. With most organic ionisation potentials (energy required to remove an electron from a neutral atom) in the range 4.1- 5.5eV for p-type material the metal needs a similar work function.[24] Gold, with its work function of 5.1 eV and anti-corrosive properties is a popular choice as an electrode material. [25-27]

Therefore, at a negative gate bias charge carriers will be available at the interface between dielectric-semiconductor forming a conduction channel. At low drain voltages this charge will be uniform and evenly spaced with an increase in drain voltage resulting in a direct increase in drain current. Once $V_{DS} > V_{GS}$ and the potential at the drain becomes increasingly negative, the potential drop with respect to the gate changes and pinch off results. The current past this point remains constant under increasing drain potential and the device is in the saturated regime with the net flow of charge carriers from the source being constant.[28] These properties are visualised and examined through electrical characterisation of the device.

1.2.1 Device Characterisation

Common characterisation of devices revolves around I-V measurements. The output plot generates mobility values and is a graph of current measured at the drain, I_{DS} with respect to applied voltage, V_{DS} with a curve generated at several discrete gate biases as shown in Figure 1.6. With physical properties: mobility, threshold voltage (the point at which an accumulation channel has formed) and ON/OFF ratio (ratio of change in current magnitude between the ON and OFF states of the device) extracted from this data. The mobility is a fundamental physical property of a semiconductor material, describing the majority charge carriers ability to migrate through the material with respect to the field effect and is a regularly reported quantity, taking the role of a benchmark.[2, 29-31]

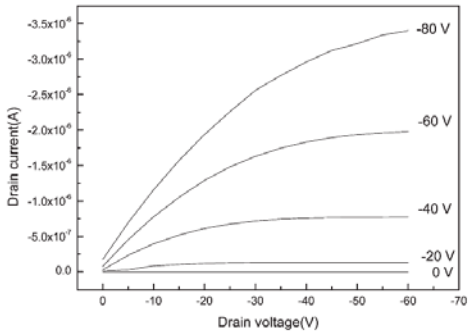

Figure 1.6. Typical output plot for a p-type accumulation device with drain voltage (V_{DS}) being swept and that gate voltage (V_{GS}) being stepped in 20V increments.[1]

A typical output curve for a p-type charge carrier will sweep the drain voltage from 10V to -80V and step the gate from 0 to -80V. The exact magnitude of the potentials depends on the capacitance ability of the dielectric and the system being investigated. It should also be noted that in the case of an n-type material the situation is the same just with a reversal of potential sign (negatives become positives) when devices feature symmetric geometry and electrode composition. The plot itself is characterised into two sections: linear regime and saturation. With saturation being the point of drain current plateau and linear describing the current behaviour near the origin. Before current saturation is a period of sub threshold behaviour as the channel pinches off and reaches constant current.[7]Although there have been several models used to describe these devices, the most common model used to describe the performance is the gradual channel approximation proposed by Shockley.[32] The charge density, $Q_S(x)$ accumulated along the channel at the spatial position, x follows the potential profile $V(x)$ at the position in the channel.

$$Q_S(x) = C_G V(x) \qquad \text{Equation 1.1}$$

Where C_G is the capacitance produced by the dielectric material. The output current, I_{DS} is therefore derived by,

$$I_{DS} = \frac{1}{L}\int_0^L E Q_s(x)\mu dx \qquad \text{Equation 1.2}$$

Where E the lateral is electric field and $Q_s(x)\mu$ represents the conductivity. Substitution of equation 1.1 into equation 1.2 leads to the output current equation for OFETs. In the linear regime where $V_{DS} << V_G - V_T$ the current is described by,

$$I_{DS} = \frac{W}{L} C_G \mu_{FE} [(V_{GS} - V_T) - \frac{V_{DS}}{2}] V_{DS} \qquad \text{Equation 1.3}$$

Where W is the width of the channel, L the length of the channel and μ the field effect mobility. In the saturation regime where $V_{DS} \geq V_{GS} - V_T$ the current is described by,

$$I_D = \frac{W}{L} C_G \mu_{SAT} [(V_{GS} - V_T)]^2 \qquad \text{Equation 1.4}$$

The field effect mobility of a material is dependent on gate and drain voltages, V_{GS} and V_{DS} respectively and is calculated through measurements in the linear regime. The field effect mobility is given by re-arranging and substitution in Equation 1.3.

$$\mu_{FE} = \frac{2L}{W C_G V_{DS}} [\frac{\delta \sqrt{I_{DS}}}{\delta V_{GS}}]^2 \qquad \text{Equation 1.5}$$

It follows that by knowing the physical parameters (L and W) and theoretical capacitance at your gate C_G of your device that a graph of $\sqrt{I_d}$ vs. V_{GS} will have a slope that is a V_{DS} dependent mobility.

The second characterisation is the transfer plot. A graph of the drain current I_{DS} with respect to the gate voltage V_{GS} this result is acquired by sweeping the voltage applied to the gate, measuring the drain current and is taken at several discrete drain voltages. Seen in Figure 1.7 this plot contains information on the switch on voltage of the device, V_o, which is an interpretive value at which the device shows function.[7]

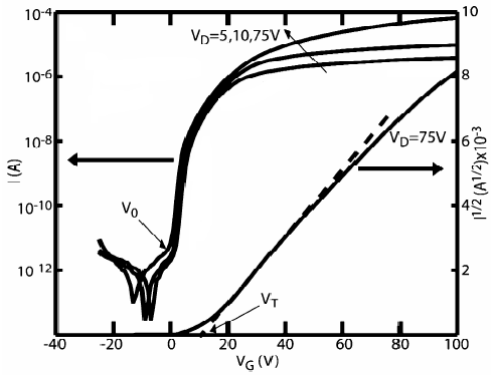

Figure 1.7.Typical transfer curve with the gate voltage Vg being swept and the drain voltage being swept from -40 to 100V [2]

And the threshold voltage (V_T) the traditional parameter which is refers to the voltage at which a conduction channel has formed. An extrapolated straight line graph of $\sqrt{I_d}$ vs. V_{GS} through the x intercept will give you the value of the threshold voltage. Finally to compute an ON/OFF ratio a leakage current in the order of 10pA needs to be measured. All these properties are analysed using a source-meter unit (SMU) these devices offer the necessary control over voltage and the necessary resolution in meter measurements. Typically software to interface with a PC is created that allows the generation of these graphs. An overview of the measurement requirements are shown in Table 1.1.

Table 1.1.Instrumentation range required for planar FET characterisation.

Physical characteristic	Requirement
V_{GS}	-100V to 100V
V_{GS} ramp	V steps satisfactory
V_{DS}	-100V-100V
V_{DS} ramp	V steps satisfactory
I_{DG}	10pA detection resolution
I_{DS}	10^{-7}A resolution required

1.3 Organic Electronics

Flexible, revolutionary and offering processing properties not possible with silicon, the scientific field of organic electronics focuses on developing devices and circuits fabricated with organic macromolecules as active materials.[13]Organic electronics are earmarked in low cost printable electronics and offer a change in fabrication scale and rate through reel to reel mass printing of electronic circuits, potentially filling a market complimentary to silicon and inorganic electronic technologies.[33]

The unique properties of plastics to be solution processed provides unique possibilities dependent on the device aims.[34] These include traditional printing methods of scale including flexographic,[35] gravure,[33] and offset printing. Digitally controlled techniques include methods such as inkjet printing,[36-38] and spray coating.[39] Further processing advantages include patterning,[40-42] and soft lithography[40, 43] techniques. Many of these technologies involve low temperature processing and are capable of increases in scale, leading to potential commercialisation of devices. With completed functioning circuits being demonstrated using this technology.[44-46] Furthermore, organic transistors and circuits have been shown on flexible substrates.[47-49] With these technologies it is possible for organic electronics to produce electronics on a large scale, effectively reducing the cost of resulting products and revolutionising consumers lives.

1.3.1 Energy level Alignment at Organic/Metal Interfaces

Despite being successfully used in optoelectronic devices. The operating physics of organic based devices is not clearly understood.[50] With the underlying equations and analysis based on the Shockley equation and the resulting metal-semiconductor interface described by the Mott-Schottky model. The Mott-Schottky model assumes (i) a vacuum level alignment at the interface and (ii) Band bending in the space charge layer.[20] When two solids with different Fermi levels are brought into contact they reach a thermal equilibrium through the exchange of charge carriers creating a common Fermi level and vacuum level.[23] Recent studies focusing on photoemission spectra of metal-organic systems obtained under ultra-high vacuum have shown that this may not be the case with organic systems. With the formation of an interface dipole resulting in a shift in vacuum energy level not predicted to occur in the Mott-Schottky model. The findings suggest more research is needed to determine the nature of organic semiconductors and whether band bending does indeed occur in organic systems.

1.3.2 Polymers

Possessing a large molecular weight, polymers are long chain macromolecules, of smaller repeating molecular units, monomers.[28] Whether it is one, two or three monomers in homo or hetero arrangement can lead to further classification of the polymer as an organic macromolecule, and is depicted visually in Figure 1.8.

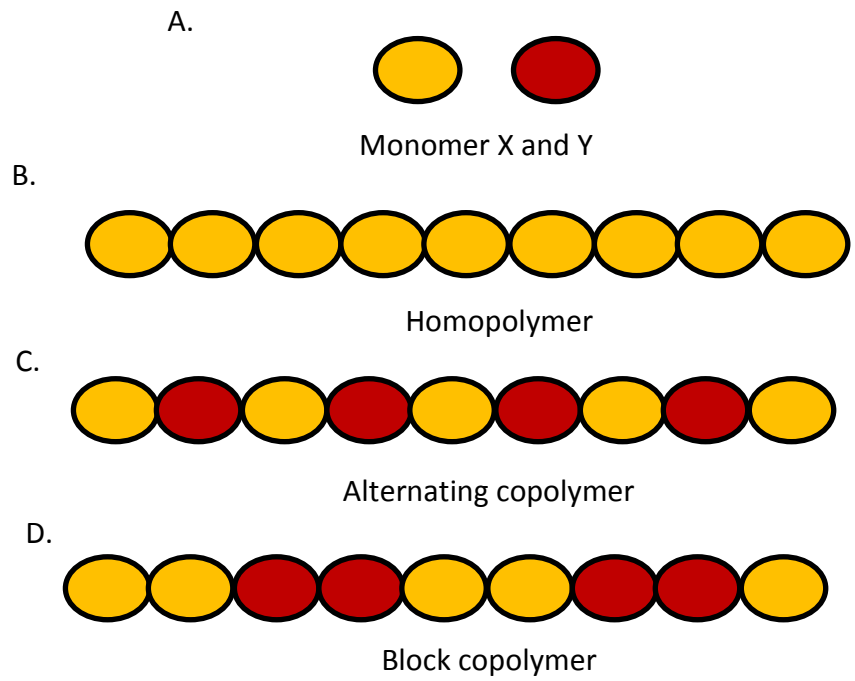

Figure 1.8. Schematic representation of polymer classification and the resulting polymer matrice A. Discrete monomers X. and Y. Monomers are individual molecules that may bond to create a polymer with the arrangement of monomers classifying the polymers. B. Homopolymers comprised of a discrete monomer repeating unit. C. Alternating co-polymers comprised of alternating monomers. D. Block co-polymers comprised of blocks of monomer units.

Carbon and carbon-carbon bonds are dominant in polymers and directly responsible for some polymers ability as an electrical material. When a molecule possesses alternating double and single carbon-carbon bonds the polymer is considered to be a conjugated polymer.[51] Conjugated polymers exhibit an overlap of pi-bonds across an intervening sigma bond allowing for the delocalisation of pi-electrons across all adjacent aligned pi-bonds allowing for electron conduction down the length of the polymer chain. This property was first observed in the conjugated polymer, polyacetylene in 1977.[52, 53] And the first field effect transistor device based on a conjugated polymer shown in 1987 using a polythiophene polymer.[54]

High performance devices seek to maximise electron transport which is dependent on accurate alignment of energy levels between materials at interfaces, in polymeric materials these energy levels are referred to as highest occupied molecular orbital (HOMO) or lowest unoccupied molecular orbital (LUMO). When attempting to select or develop a material for an application it is important to note, the use of HOMO/LUMO energy levels is a theoretical one, with HOMO/LUMO energy values not obtainable experimentally. Rather, what is measured is the amount of energy required to remove an electron, the ionisation potential (IP) which is related to the HOMO and the energy required to add an electron, the electron affinity (EA) of a polymer, which is related to the LUMO. Due to electronic correlations that can occur during the removal and/or addition of an electron these values do not show agreement with HOMO/LUMO levels. Furthermore, the specific orientation and geometry of a molecule with respect to its neighbours will affect the IP and EA resulting in further disparity between the obtained IP, EA energy and HOMO/LUMO energy expectations. This can result in the measurement of different IP and EA when using different methodologies for a sample and even across a sample being measured. [55]

Due to the spatial alignment required, optimisation of film morphology is critical in the development of optimised devices.[56-60] Cast polymer films have been shown to exhibit both amorphous characteristics[61] and ordered structures.[62] However, the significant variability in polymer microstructure and conduction based on molecular weight, synthesis and processing conditions leads to various transport models in the same polymer making a general polymeric model of conductivity elusive. Two working models are used in the discussion of polymeric conduction.

1.3.1 Multiple Trappings and Release Model

Adapted from amorphous silicon, multiple trappings and release(MTR) works under the presumption a density of localised states exist within reach of the delocalised states.[63] The carriers in localised states are bound by an activation energy governed by its proximity that is thermally activated.[63] The behaviour is Arrhenius like with respect to distance and temperature. Due to the innate differences

between solid band structure and polymer HOMO and LUMO this modelling is only applicable and descriptive of highly ordered polymer films.

1.3.2 Variable Range Hopping

Based on localised state hopping/ tunnelling through the polymeric backbone variable range hopping (VRH) applies to localised state hopping.[64] Temperature dependence is incorporated and weak electron-lattice coupling is assumed (and true when studying amorphous polymeric films).[65] However, this is limited by not defining the charge carrier species and not meeting experimental results completely.[64] As it stands there is a need for an appropriate charge transport model in polymers.[66-68]

1.4 Applications for Organic Transistors and Device Requirements

1.4.1 Organic CMOS (Complementary Metal Oxide Semiconductor) Circuits

Complimentary metal-oxide semiconductor circuit technology utilises complimentary transistor devices with p-type and n-type transistor behaviour to create integrated circuits that perform specific functions.[69] Through the application of the operating principle of the CMOS inverter circuit logic gate functions AND, NAND, NOR and OR can be performed. Figure 1.9 shows the NAND electronic gate logic function. The NAND gate is unique in that it can be used to create all the other logic functions. A property referred to as functional completeness.[6]

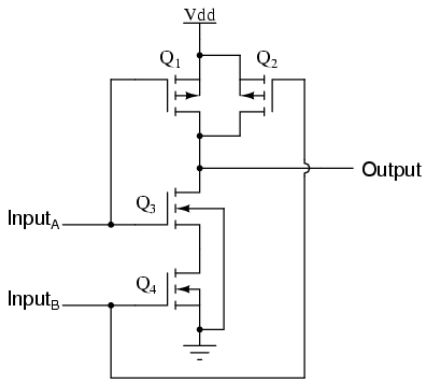

Figure 1.9. CMOS NAND logic circuit. The logic circuit operates utilising an inverter logic circuit with devices Q_1 and Q_3 on input A and devices Q_2 and Q_4 on input B. The resulting output will be high for all cases where either Q_1 and Q_2 saturate and will only go low if both Q_3 and Q_4 saturate.

Devices Q1 and Q3 are controlled using Input A and resemble the series connected pair in an inverter circuit. With Q1 turning off and Q3 turning on during a high input signal and with a low input signal the opposite is true with Q1 saturated and a high signal observed at the output. Devices Q2 and Q4 are controlled using the second input B and will exhibit the same logic output as Q1 and Q2. Transistors Q1 and Q2 have their source and drain terminals connected in parallel while Q3 and Q4 are connected in series. The resulting output will be high for all cases where either Q1 or Q2 saturate. A low output is only possible if both Q3 and Q4 saturate. CMOS circuits further feature low power dissipation, speed and greater tolerance to individual device variability.[6]

In DRAM memory applications the ability to go to from an on state to an off state is the limiting factor in read and writes speeds. This switching limit is determined through passing a high to low square wave gate bias at high frequency and observing at which point the current loses its ability to communicate on (1) or off (0).[70] The switching frequency, f is directly proportional to $\frac{\mu}{L^2}$. The current I_d is directly proportional to μ/L these important relations govern a transistors possible application scope as memory in information technology.[71, 72]

1.4.2 Electronic Paper

Electronic paper has been seen as a potential application for flexible organic electronics.[73]With the scope to utilise the large scale production and flexibility capable of solution processing electronic paper has been earmarked for application in price tags, electronic billboards, mobile phone displays and e-readers. First demonstrated through a 5” x5” active matrix back pane consisting of 256 pixels with a pentacene active layer in 2001.[73] Electronic paper revolves around the use of a voltage-controlled display being driven by a backplane featuring organic transistors. Commonly an electrophoretic display element is used with an electric field being used to turn on specific pixels. The technology has a memory effect resulting in active pixels offering low power draw due to drive circuitry only consuming power during refresh cycles. The drive currents are often lower than active matrix displays featuring OLEDs and the requirement of performance stability across the array less

stringent. Furthermore, the ability to produce flexible arrays is a key performance factor of electronic paper which sees organic electronics well positioned to meet.

1.4.3 OLED Active Matrix Displays

OLED displays featuring full-colour video capabilities on flexible substrates are a high performance application utilising organic field effect transistors. OLED displays on glass substrates are currently incorporated in smart phone and PDA devices and are displacing LCD screens in the small display sector.[11] Devices are set to enter the market featuring mid to large displays incorporated into tablets and TVs. A challenge in realising this technology are the high mobility requirements required for the control and drive transistors in the active matrix backplanes which cannot be met using traditional amorphous silicon.[11] OLED active matrix displays are current driven devices with the emission of OLED devices controlled by the current passing through the OLED. Active matrix displays require a continuous application of current unlike e-paper displays over the course of the entire frame time. Individual pixels may be driven for several hours at a time and requires more demanding OFET performance, stability and uniformity requirements to meet the technology demands. A two transistor one capacitor active matrix pixel is shown in Figure 1.10.

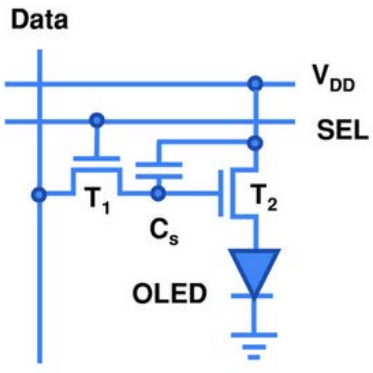

Figure 1.10.Two transistor- one capacitor pixel circuit operating via p-type transistor devices. [3]

The circuit comprises two pixel transistors, T_1 and T_2 and a storage capacitor C_s integrated with an OLED. An electronic driver applies a bias on the row electrode turning the transistor T_1 from the non-conducting state to the conducting state.

Across this transistor the voltage of the column electrode is provided and stored onto the storage capacitor, C_s this voltage is applied to the gate of T_2 and provides a programmed drive current to the OLED supplied by T_2 providing the necessary current for the image. This current maintains supplied when the transistor T_1 is switched off to address the next row in the display. The programmed drive current is such that the transistor T_2 operates in the saturation regime so that fluctuations in the voltage do not lead to fluctuations in the OLED pixel intensity. The transistor T_2 requires device performance such that a sufficient current density is supplied to the OLED to produce the desired brightness. The incorporation of planar OFETs into the active matrix results in device limitations placed on the W/L ratio (W= channel width, L= channel length) in order to produce high resolution displays but with necessary drive currents needing to be produced. Moving to architectures capable of large drive currents with reduced surface areas and W/L ratio has the scope to improve the state of active matrix displays featuring OFETs.[11]

1.4.4 RFID Tags

Radio frequency identification (RFID) tags are expected to be used on a per product basis to allow inventory management and point of purchase security in a range of industries including automotive, retail, cash security and pet protection. RFID tags allow for the chip less transfer and storage of simple information. Figure 1.11 shows a block diagram of an RFID device. [74]

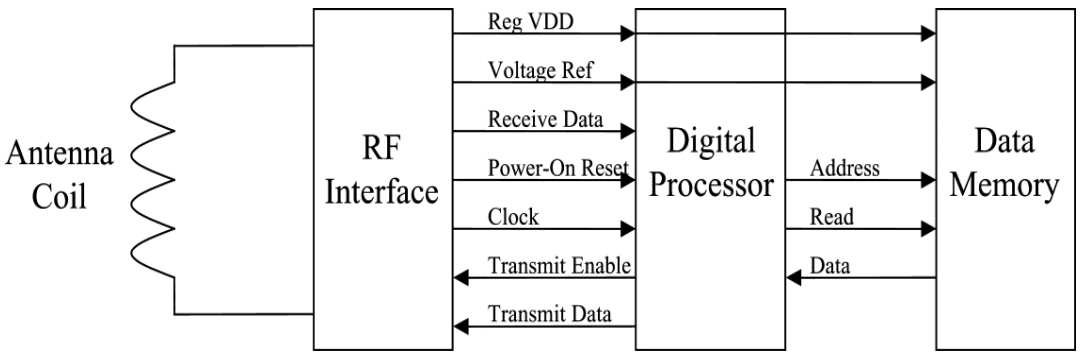

Figure 1.11. Block diagram of an RFID device. The critical components in reading, writing and erasing data are described. Critical to the implementation of the FRID is the antenna coil capable of turning the radio frequency data from a RFID reader into computable information.

Key to the operation of the RFID tag is the antenna coil which couples transmitted data into a DC power supply. An RF rectifier in the RF interface provides a supply of DC power to the entire RFID device. With the frequency of the rectifier required to operate at the frequency of the incident signal. Operating frequencies for RFID devices are either 125KHz or 13.56 MHz.[74] A capacitor is used in the RF interface and stores power from the rectifier and powers the additional circuitry in the tag. Figure 1.12 shows a circuit diagram of the rectifiers used in RFID technology.[74]

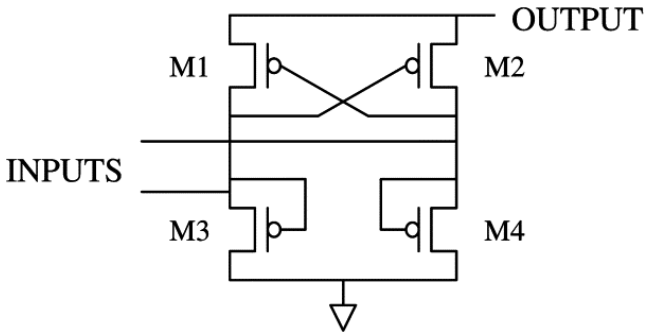

Figure 1.12. Circuit diagram for a wave rectifier required in the function of RFID technology.

In order for transistors to rectify at higher frequency the transient dynamics of the field effect transistors used to create the rectifier circuit need to be such that they saturate in response to the applied frequency with devices constantly operating in the quasi static regime.[17, 75] As such the frequency characteristics of these devices improve with reduction in the W/L ratio. With a key barrier to market penetration being the price point of these devices, with RFID featuring silicon technology proving costly to manufacture and preventing market up take. The increased financial viability of solution processed organic semiconductors sees a possibility to establish RFID technology based on organic electronics.

1.4.5 Organic Transistors in Commercial Devices

Microelectronics and displays incorporating OFETs show strong promise, offering the benefits of solution processing technologies and the demonstrated ability to fabricate working circuits on flexible substrates. Improving the prospect of OFETs in commercial applications is application specific but broadly centres on the improvement of device performance and associated cost of achieving the performance. Research investigation for improved performance has focussed on the improvement of organic semiconducting material properties through the synthesis

of improved materials.[72, 76-83] And the optimisation of planar OFET devices through which has seen research in a broad range of areas. From interface engineering leading to improved device performance,[84-91] optimisation of active layers,[58, 60, 92, 93] improved dielectric materials,[94-100] and optimisation of parasitic resistances.[24, 42, 101-106] With solution processed methodologies developed to take advantage of fabrication methods with the ability to adapt to increases in production scale.[34, 36, 37, 44, 107, 108] Independent of the material properties or architectural optimisation improved device performance also focuses on design and improvement of the W and L scale and field effect propagation through the channel.[109-114] Scaling of the channel/gate length of organic field effect devices offers several key advantages:

- Improvement of switching characteristics.
- Decrease in Power Usage.
- Packing and chip density improvements.

The scaling of planar OFET devices is ultimately limited by the lateral resolution of the process used to fabricate the device. A methodology capable of commercial scale up is required to meet the requirements of short channel lengths in market devices. One approach of interest in increasing the feasibility of transistors from organics and polymers is the development of a vertical transistor. Vertical transistors offer one approach to scaling and improving the scope of performance from transistor devices fabricated from organics and polymers. Vertical transistors are novel architectures with potentially improved performance.

1.5 Vertical OFETs

Vertical transistors offer the possibility to increase device performance through unique device architectures. By having a channel perpendicular to the substrate the gate length can potentially be determined by the thickness of a deposited film improving device performance through decreased gate length and presenting structures that are not dependent on the lateral resolution of a master mask. The

realisation of vertical organic field effect transistors (VOFETs) is a relatively new field in comparison to planar OFETs. Figure 1.13 shows the publications of international VOFET research 2004-2015.

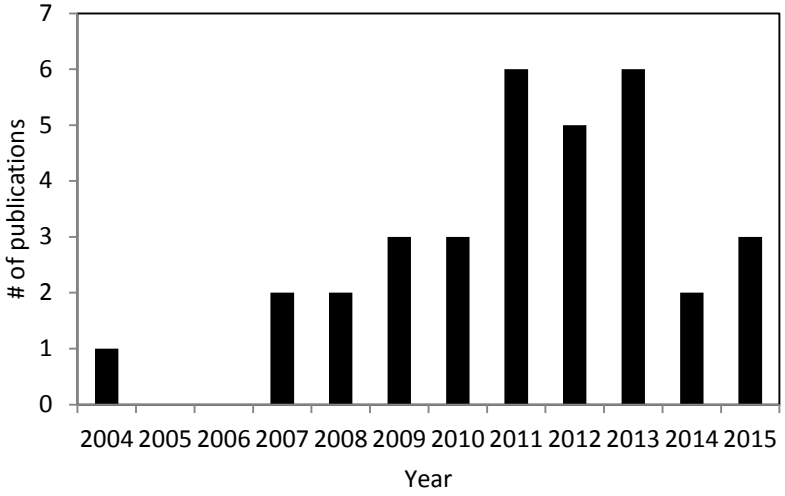

Figure 1.13. Organic vertical transistor publications by year from 2004,[115]2007,[116, 117] 2008,[118, 119]2009,[120] 2010,[121, 122]2011,[11, 123-129]2012,[130-133]2013,[134-140]2014,[141, 142] and 2015.[143-146]

Despite a strong international research focus on traditional planar OFET technology, VOFETs are a new field to organic electronics and present exciting opportunities to develop novel architectures. The current state of literature is broadly categorised into vertical wall VOFETs and Schottky barrier VOFETS.

1.5.1 Vertical OFETs Featuring Vertical Wall Architecture

The gate length and width directly affect the maximum current through the channel, and the switching capabilities, such as response time and shape of the devices.[115, 116, 118, 147-154] Traditionally, silicon vertical transistors require the formation of clean sidewalls achieved predominantly through photolithography.[155, 156] These traditional metal-base structures have been shown using organic materials.[125, 157] With the arrival of organic electronics and paradigm shift of solution processing of semiconducting small molecules and polymers with unique material properties, the relatively new field of VOFET fabrication has the scope to further revolutionise the scope of vertical wall architectures in microelectronics. In 2003 Sirringhaus *et al.*[158] published the first

research work on VOFETs with a scalable wall technology. The device architecture, fabricated using a solid state embossing technique is shown in Figure 1.14. The solid state embossing technique is a non-lithographic process featuring a silicon cutting tool with an array of sharp protruding wedges that is used to emboss a multi-layer polymer stack. Through an applied pressure action the silicon cutter was used to emboss an electrode-insulator-electrode stack on PET substrate patterning a groove into the material and creating a trench which introduced a vertical wall in the structure.

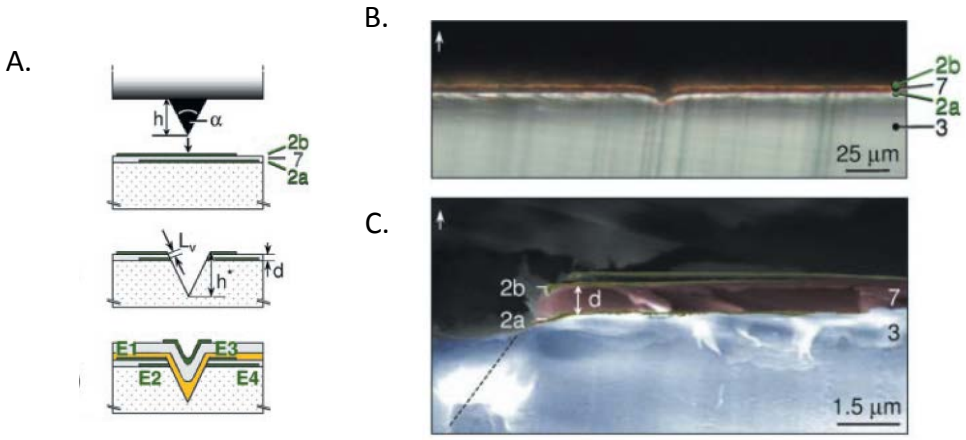

Figure 1.14. A. VOFET device as fabricated by Sirrinnghaus *et al*. The VOFET is fabricated on poly(ethylene terephtatale) (PET) substrate. PEDOT:PSS electrodes are used in the configuration featuring a P3HT active layer(gold material). An electrode-insulator-electrode multilayer film (2a, 7 and 2b respectively) are mechanically embossed allowing for the deposition of the P3HT active layer over the vertical wall. In the architecture the gate length is defined by the interlayer insulating film (7). B. Optical image of the cross-section of embossed devices. C. Transmission electron microscopy of device cross-section.

Through this process the gate length is controlled by the thickness of the insulating film between the electrodes. The micro-cutting trench is seen to be approx. 1.5µm in width over which the Poly(3-hexylthiophene-2,5-diyl) (P3HT) active layer is spun cast creating an electron path between the two electrodes and then a Poly(methyl methacrylate) (PMMA) gate dielectric is spin coated. In order for a poly(3,4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS) gate electrode to be deposited a self-alignment procedure featuring a plasma treatment on the PMMA dielectric to render it hydrophilic was necessary. In combination with an octyltrichlorosilane (OTS) monolayer the wetting properties were tailored as such that PEDOT:PSS was selectively deposited in the trench and only the trench. The

outcomes of this work were vertical walled devices; with gate lengths of 0.7µm studied in comparison to planar devices using the same process with gate lengths of 2 µm. Using P3HT as the semiconductor material output characteristics of the devices were measured and can be seen in Figure 1.15. The maximum current was seen to be greater in the vertical structures reaching 6.0µA at a gate voltage of 20V and 0.3 µA for the planar device showcasing that shorter gate lengths offer increased viability in applications where current is a factor, i.e. active matrix displays and memory cells.[159]

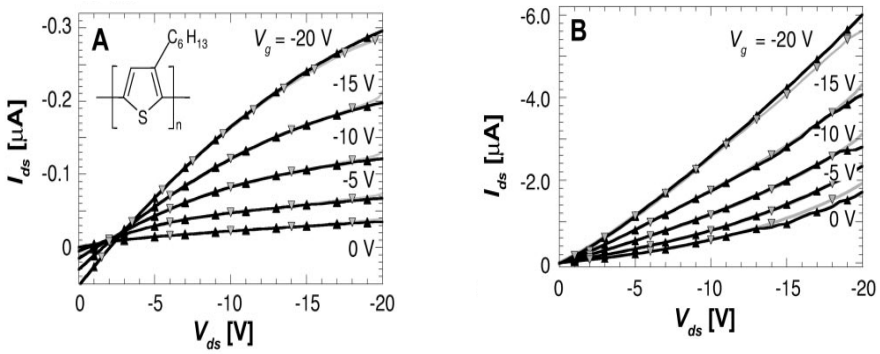

Figure 1.15. A. Obtained output electrical characteristics of planar OFET devices fabricated through solid state embossing. B. Obtained output plot of VOFET devices. A lack of saturation is observed in output plot for vertical devices.

The pioneering work of Sirringhaus *et al.* establishes the potential of VOFET device architectures to offer shorter gate length structures without the use of lithographic processing. Through the use of an inter-layer spacer, gate length is controlled by the resolution of a solution processed thin film. Sirringhaus *et al*. claim further downscaling of the channel is possible but limited by the leakage current to the gate electrode (becoming significant at interlayer spacer thicknesses = 500nm) and topography roughness of the substrate another factor. Key limitations to the structure include the necessity of PEDOT:PSS electrodes in order for the cutting technique to adequately introduce a vertical wall. Whether the solid state embossing technology can be adapted to thin film metal electrodes is unclear as PEDOT:PSS has been show to induce etching due to its acidic nature,[160] and reduced performance over the lifetime of a device changing performance of fabricated devices with PEDOT:PSS.[161] The necessary exposure to oxygen plasma

in the deposition of a functioning gate electrode has been shown to greatly degrade polymer devices leading to the scission of C-C bonds and degradation of properties.[162]

Defining the gate length through a spacer material in combination with a vertical wall as shown by Sirringhaus *et al*. has been a crucial methodology in the development of VOFETs featuring a vertical wall. Parashkov *et al.*[148, 150] and Bergrren *et al.*[152] adapted this methodology to realise VOFETS with vertical walls and gate lengths controlled through a photo resist spacer layer to define the device channel length. The methodology and resulting structures are shown in Figure 1.16.

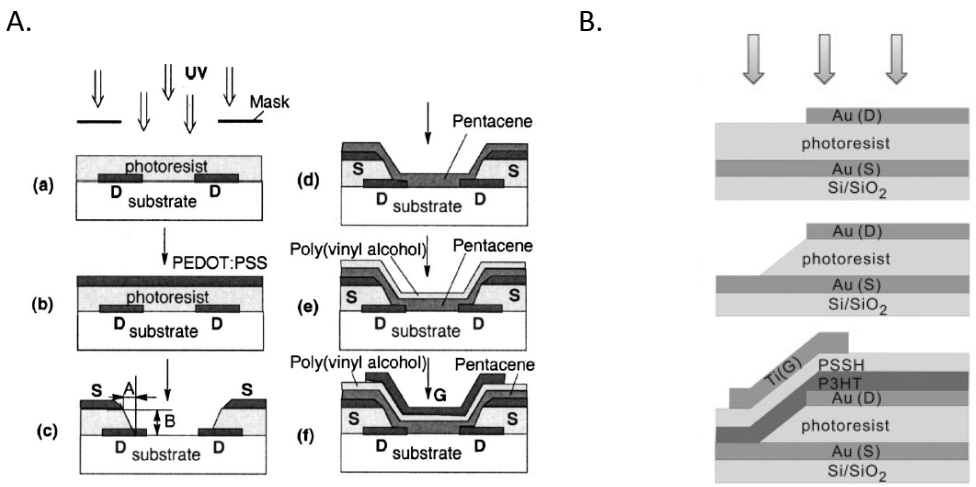

Figure 1.16. A. Fabricated VOFET device by Parashkov et al. fabricated on glass substrate. UV lithography is used to introduce a vertical wall into a photoresist layer with patterned source electrode by defining the gate length of the pentacence active layer deposited over the photoresist. A PEDOT:PSS source electrode is used in combination with a Polyvinylpyrrolidone (PVP) dielectric and evaporated gate electrode.B. Fabricated VOFET device by Bergrren et al. fabricated on silicon with silicon dioxide dielectric utilising a photoresist spacer layer. UV lithography is used to etch a vertical wall into the structure.

The fabricated pentacene channel devices of Parashkov *et al.* had gate lengths of 2µm, an order of magnitude increase in channel length over the work of Sirringhaus *et al.*[158]. With a current output of 0.16 µA at -32V gate bias the presence of significant leakage currents and poor pentacene mobility= 1.0 x 10^{-4} cm^2/V is reported. Although not an optimised device, the 3 orders of magnitude discrepancy of the known pentacene mobility (~40 cm^2/V) indicates the structure has reduced lateral field propagation into the channel which may not be overcome through material selection and device optimisation. In 2004 Parashkov *et al.*[148, 150]

showed an analogous device structure fabricated using excimer laser tuned to 248mm to etch vertical walls into photo resist creating pentacene devices. Beyond this, the incorporation of vertical wall structures has largely been defined via lithographic or silicon etching methods to date.[153, 163]

The current state of vertical wall VOFETs shows a dependence on devices featuring advanced lithographic fabrication techniques adapted from silicon technology. This method of fabrication is costly with the associated devices fabricated largely for fundamental documentation with limited scope for production or incorporation into products. Beyond the work of Sirringhaus *et al.* no scalable technology has been pursued for the incorporation of vertical walls in multi-layer polymer stacks. As such the specific focus on the introduction of vertical wall architectures through new methodologies is an exciting prospect for the maturation of the technology. The successful technology will be ultimately be closely linked with the device architecture and mechanism of operation with consideration to the composition of the electrodes and the active and functional materials being processed leading to the possibility of stable devices that can be incorporated into circuits.

1.5.2 Schottky Barrier Vertical OFETS

Fabrication of Schottky barriers involves the formation of an electrically rectifying interface between the deposited electrode and semiconducting polymeric material. Aluminium and P3HT are commonly reported materials to form a Schottky barrier junction seen in Figure 1.17. Due to a mismatch in work functions between Al (W_f = 4.2eV) and P3HT (HOMO= 4.9eV) when the two materials are brought into contact, charges diffuse across the interface from higher energy levels to lower energy levels (with respect to a vacuum level, defined as the energy required to remove an electron into surrounding vacuum) reaching a thermodynamic equilibrium across the interface driven by the Fermi energy of the materials brought together. [23] The transfer of charge forms a p-n junction due to the diffusion of electrons (donated from the aluminium metal) combining with hole charges present in the P3HT HOMO orbital. Due to this a depletion region is produced resulting in an interface dipole creating an opposing electric field that acts as a potential barrier balancing the work

function mismatch. In 2001 Kaneto *et al.*[164] reported that the depletion width from the P3HT/Al interface extended up to 150nm into the polymer.[23]

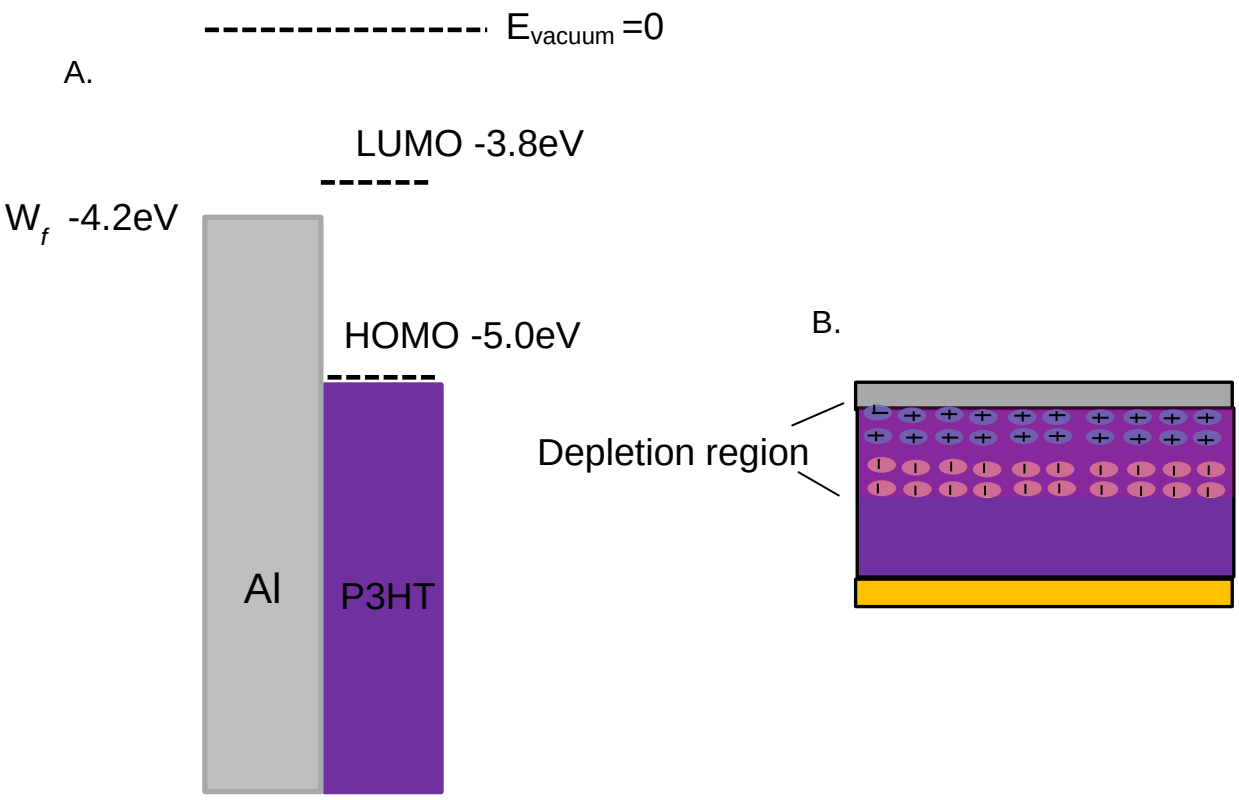

Figure 1.17. A. Energy level schematic of the aluminium-organic interface. B. Depletion region sketch within a two terminal schottky barrier device.

The formation of this interface is highly reliant on temperature, roughness and processing conditions with the exact barrier height known to vary across the surface by as much as ±0.4eV.[165] Understanding the physical vapour deposition of aluminium and the consequences on the resulting devices is critical in the fabrication of reliable polymeric Schottky barrier devices.

Without the use of a vertical sidewall Yang *et al.*[115] demonstrate a VOFET featuring the modulation of a Schottky barrier as the operating principle. Using a common source in a sandwich configuration as seen in Figure 1.18A the design is advantageous in that it provides a large cross sectional area (defined by the cross section of the source and drain electrodes) without requiring any sidewalls to be introduced into the structure. A mismatch of energy levels is intentionally selected between source electrode and semiconducting material at zero gate bias, forming a Schottky barrier to minimise off state and reverse currents. Featuring the n-type

active material C_{60} , the gate is positively biased and sees a polarisation of the charges throughout the source. Typically in this configuration the field produced by the capacitor would be shielded by the aluminium electrode. However, the large surface roughness (comparable to the thickness) at the source-organic interface sees electrons induced at this interface resulting in a reduction in the Schottky barrier potential, Δ_{SBH} allowing charge injection which can be visualised in Figure 1.18B.

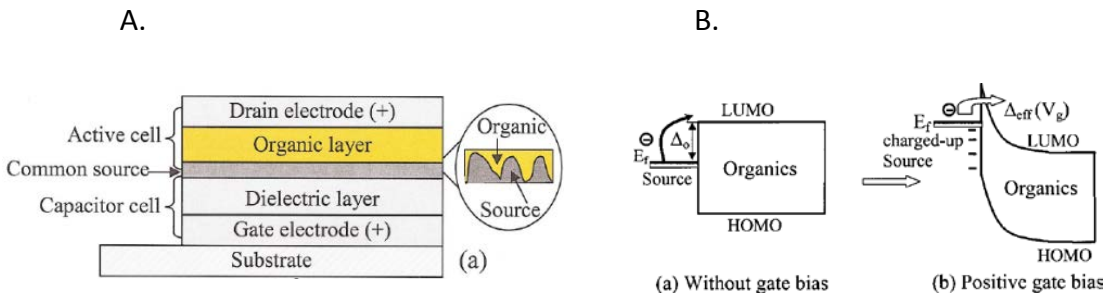

Figure 1.18. A.Fabricated VOFET device by Yang et al. on glass substrate. Copper is used as the gate electrode and in combination with 240nm lithium fluoride dielectric forms a capacitor cell. An aluminium source electrode and n-type C_{60} is used as the active layer B. Visualisation of the energetic barrier at the metal- semiconductor interface, key operating principle of the stacked architecture operating using an n-type semiconductor.

This unique approach allows for short channel lengths and large cross-sectional areas, providing means to achieve high currents at low operating voltages. The output plot indicates high current in the order of milliamps at low drain and gate biases of 5V. Subsequent work by Yang *et al.*[118] revolves around introducing buffer layers between the source and dielectric, to allow control and adjustment over the work function mismatch using metal oxides and lithium fluoride respectively. Furthermore, the change in capacitance with respect to humidity and the effect it has on device performances in these devices has been reported.[118] Recent work has focused on using the p-type material P3HT and optimising their device configuration and further understanding of the mechanisms of their architectures function. This work is an extension of their original sandwich architecture transferred to a p-type material, presented alongside with an investigation of V_2O_5 as a buffer layer between source and semiconductor channel.

Potentially entirely solution processed the results is some of the highest currents reported for P3HT transistor devices.

The work of Yang *et al.* shows the possibility of gate controlled Schottky barrier VOFETS. The key to the proliferation of the novel structure is the low off state currents between the source and drain electrodes. Allowing for large area, large current devices to be realised with greatly reduced reverse and off state currents. The mechanism of operation has since been incorporated in devices featuring perforated electrodes,[142, 166] patterned electrodes,[134, 138] bilayer source electrodes,[140] carbon nanotube electrodes,[119, 133, 135] metallic nanowire electrodes,[143] and a barrier tunnelling operation mechanism[137] with the perpendicular propagation of an electric field into a novel source architecture resulting in a distribution of induced charges lowering Δ_{SBH}. An approach of soft lithography processing of patterned source electrodes has been shown[139] and provides the only work on a potentially scalable process for this architecture. The incorporation of this novel thin film source electrode technology provides limitations around the uniformity and long term stability due, either to the randomly distributed network produced by metallic nanowires and carbon nanotubes through to the high resolution patterning providing scope for interface traps and inconsistencies. The ability to scale the processing of these devices and retain device performance has not been established. The current state of Schottky barrier devices as such is largely for fundamental interest as it stands. Despite the exciting electrical performance of these devices they remain laboratory scale devices using precision methodology with no scope to be integrated into a commercial process. As the industry stands, there is scope to further leverage polymeric technologies in the development of VOFET devices and incorporate vertical wall and Schottky barrier devices into a truly novel architecture with the scope for commercial application.

1.5.3 Schottky Three Terminal Device Considerations

In 2012 Chung *et al.*[167]demonstrated a three terminal device functioning through a gate controllable Schottky barrier. The device, a graphene barristor was fabricated using silicon as the the active channel with a graphene source electrode and can be

seen in Figure 1.19A. A capacitive couple between the gate electrode and the graphene allows for an electrostatic induction of charges across the graphene effectively modulating the Schottky barrier height, ϕ_B at the graphene-silicon interface between and OFF state seen in Figure 1.19B. to an ON state seen in Figure 1.19C. in the ON state.

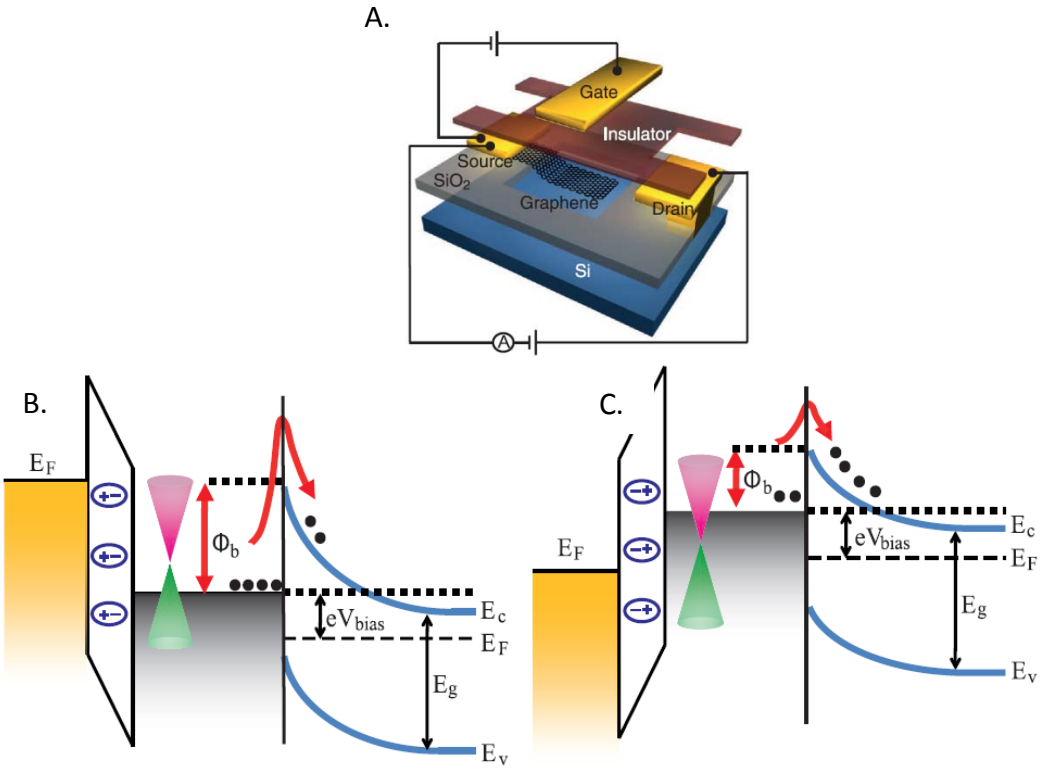

Figure 1.19.Three terminal graphene barristor as fabricated by Cheng et al.[1] A. Device schematic. The device is a planar structure structure on silicon wafer with silicon acting as the active channel with graphene- silicon interface at the source electrode. . B. Energy level in the OFF state with the Fermi energy of the graphene producing a schottky barrier at the graphene-silicon interface, ϕ_B. C. The ON state (under applied gate pontential) the gate-dielectric capacitive couple induce charge at the graphene-dielectric couple resulting in a polarisation in charge resulting in a shift in the fermi level and resulting in a reduced ϕ_B at the graphene silicon interface and increase in measured drain current.

Cheng *et al.*[167] describe the operating principle of the device. Under applied bias across the gate electrode the Fermi level of the graphene can be controlled. Induced charges at the gate-graphene interface shift the electrical equilibrium at the graphene silicon interface. The resulting decrease in Fermi level reduces the potential barrier, ϕ_B to injection at the graphne-silicon interface. The resulting decrease in ϕ_B reduces the barrier of injection resulting in an increase in the measured drain current as described by the thermionic emission model. Cheng *et*

al. fabricate an atomically pristine interface between graphene and silicon via controlled chemical vapour deposition of graphene on silicon. The resulting pristine interface has reduced energetic trap states across the interface allowing for effective modulation of the Schottky barrier. N-type and p-type operation was demonstrated through the use of silicon with different majority carriers with this operating principle with output curves captured under both forward bias regimes for both materials and presented in Figure 1.20.

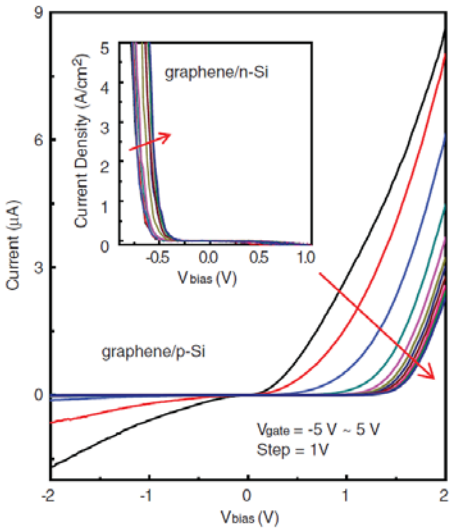

Figure 1.20. Three terminal graphene barristor output plot A. P-type silicon output plot. Potential voltage V_{ds}= ±2V whilst gate potential, V_{GS} is swept -5V to 5V in 1V increments. INSET- N-type silicon out put plot. Potential voltage V_{ds}= ±1V whilst gate potential, V_{GS} is swept -5V to 5V in 1V increments.

Cheng *et al.*[167]are able to achieve an ON/OFF ratio on the order of 10^5 for the device. Furthermore, Cheng *et al.*[167]fabricate a functional 2000 device array on silicon using the technology. Several types of basic logic are shown to work. The capabilities of the device in a switching circuit are shown, along with a half-adder logic configuration featuring 10 graphene barrister devices. An inverter circuit is produced showing performance of V_{DD}= 2V with a gain of 1.2. The work of Cheng *et al.[*1] shows the potential of a barrier controlled Schottky device in fast logic applications.

The potential of a polymeric three terminal vertical device operating through the modulation of barrier height is as such an area of considerable interest to commercial electronics. Schottky two terminal devices can feature channel length

on the order of nm the same order of magnitude as depletion widths created at the polymer-metal interface. An enhancement channel device could potentially induce deep energy state charges and adjust the potential barrier under device operation and would be of great interest as a potential organic barristor transistor. Understanding the operation and feasibility of such a structure would be a key step in developing the technology.

1.6 Proposed Vertical Architecture

The fabrication of vertical transistors to date has involved expensive fabrication procedures including the use of lithography to pattern substrates, additional surface chemistry to functionalise surfaces, through to materials and methodology, which may reduce the lifetime and performance of devices. In this thesis, a novel approach has been taken, which, if successful, may result in an easier path to multiple device structures in which high resolution lithography is not critical. This device structure must firstly be developed and proof of performance obtained.

In an effort to add to this knowledge and improve the commercial feasibility of vertical transistor technology a hypothesised device structure is proposed in Figure 1.21. The architecture proposes a semiconducting channel between two metal electrodes to create a two terminal vertical channel. Through the incorporation of a vertical wall a general functional material (for example a dielectric material) can be used to create an interface with the semiconductor. A third electrode (intended to work as a transistor gate electrode) coupled to the functional material provides the scope for a three terminal vertical structure.

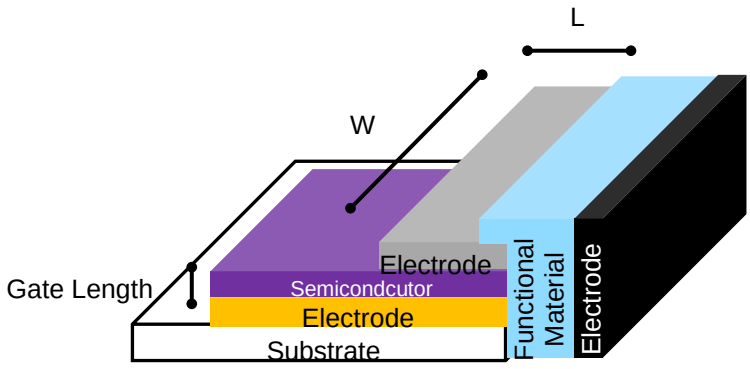

Figure 1.20. Schematic for a general vertical electrical platform. With physical parameters width (W), length(L) and gate length labelled.

Such a platform has the potential for operation through a range of different operating mechanisms dependent on the selection of physical parameters (electrode, polymer, substrate and functional material). The composition of which can be altered and optimised for scientific investigation and optimisation of vertical organic transistors. The proposed structure offers the possibility to utilise cost effective technologies by solution processing of semiconducting and functional materials providing the possibility of short channel device architectures with commercial applications.

1.7 Aim and Scope of This Research

This work aims to understand polymer physical properties for the purpose of creating a vertical transistor device with a focus on commercially viable technologies. As such this thesis is working towards the following goals.

i) Understanding of planar transistor architectures for the purpose of understanding planar architectural limitations.
ii) Development of a polymeric two terminal device platform on plastic substrate towards realising a vertical device structure.
iii) Investigate methodologies to introduce vertical wall architecture into a plastic substrate featuring polymeric thin films.
iv) Understand the requirements of active materials and limitations of the proposed device architecture in the development of a vertical organic field effect transistor device.

References

1. Sun, *Advances in organic field-effect transistors.* Journal of Materials Chemistry, 2005. **15**: p. 12.
2. Facchetti, A., *Semiconductors for organic transistors.* Materials Today, 2007. **10**(3): p. 28-37.
3. Sirringhaus, H., *25th Anniversary Article: Organic Field-Effect Transistors: The Path Beyond Amorphous Silicon.* Advanced Materials, 2014. **26**(9): p. 1319-1335.
4. Martins, R., et al., *Complementary Metal Oxide Semiconductor Technology With and On Paper.* Advanced Materials, 2011: p. n/a-n/a.
5. Luan, S. and G.W. Neudeck, *An experimental study of the source/drain parasitic resistance effects in amorphous silicon thin film transistors.* Journal of Applied Physics, 1992. **72**(2): p. 766-772.
6. *The CMOS Inverter: Analysis and Design*, in *CMOS Logic Circuit Design*. 2001, Springer US: Boston, MA. p. 103-154.
7. Valizadeh, P., *Traditional Planar MOSFETs*, in *Field Effect Transistors, A Comprehensive Overview*. 2016, John Wiley & Sons, Inc. p. 231-294.
8. Clemens, J.T., *Silicon microelectronics technology.* Bell Labs Technical Journal, 1997. **2**(4): p. 76-102.
9. Zeis, R., et al., *Field Effect Studies on Rubrene and Impurities of Rubrene.* Chemistry of Materials, 2005. **18**(2): p. 244-248.
10. Yan, H., et al., *A high-mobility electron-transporting polymer for printed transistors.* Nature, 2009. **457**(7230): p. 679-686.
11. McCarthy, M.A., et al., *Low-Voltage, Low-Power, Organic Light-Emitting Transistors for Active Matrix Displays.* Science, 2011. **332**(6029): p. 570-573.
12. P. F. Baude, D.A.E., M. A. Haase, T. W. Kelley, D. V. Muyres, S. D. Theiss, *Pentacene-based radio-frequency identification circuitry.* Applied Physics Letters, 2003. **82**(22): p. 3964-3966.
13. Myny, K., et al., *Organic RFID transponder chip with data rate compatible with electronic product coding.* Organic Electronics. **In Press, Accepted Manuscript**.
14. Choi, M.-C., Y. Kim, and C.-S. Ha, *Polymers for flexible displays: From material selection to device applications.* Progress in Polymer Science, 2008. **33**(6): p. 581-630.
15. Dinelli, F., et al., *High-Mobility Ambipolar Transport in Organic Light-Emitting Transistors.* Advanced Materials, 2006. **18**(11): p. 1416-1420.
16. Son, H.J., et al., *Poly(3, 4-Ethylenedioxythiophene): Poly(Styrenesulfonate) (PEDOT: PSS) Films for the Microbolometer Applications.* IEICE Transactions on Electronics, 2009. **E92.C**(5): p. 702-707.
17. Anthopoulos, T.D., et al., *Air-Stable Complementary-like Circuits Based on Organic Ambipolar Transistors.* Advanced Materials, 2006. **18**(14): p. 1900-1904.
18. Baeg, K.-J., et al., *Organic Non-Volatile Memory Based on Pentacene Field-Effect Transistors Using a Polymeric Gate Electret.* Advanced Materials, 2006. **18**(23): p. 3179-3183.

19. Yoo, B., et al., *High-mobility bottom-contact n-channel organic transistors and their use in complementary ring oscillators.* Applied Physics Letters, 2006. **88**(8): p. 082104.
20. Brutting, W., *Physics of Organic Semiconductors* ed. Wiley. 2006. 554.
21. Neaman, D., *Semicondcutor Physics and Devices*. 1992: Irwin Publishing. 746.
22. Valizadeh, P., *Junctions*, in *Field Effect Transistors, A Comprehensive Overview*. 2016, John Wiley & Sons, Inc. p. 119-230.
23. Natali, D. and M. Caironi, *Charge Injection in Solution-Processed Organic Field-Effect Transistors: Physics, Models and Characterization Methods.* Advanced Materials, 2012: p. n/a-n/a.
24. Gundlach, D.J., et al., *An experimental study of contact effects in organic thin film transistors.* Journal of Applied Physics, 2006. **100**(2).
25. Giancoli, *Physics for scientists and engineers*. Third Edition ed. 2003.
26. Huang, B.-C., et al., *Contact resistance in top-gated graphene field-effect transistors*. Vol. 99. 2011: AIP. 032107.
27. Darmawan, P., et al., *Reduction of charge injection barrier by 1-nm contact oxide interlayer in organic field effect transistors.* Applied Physics Letters, 2012. **100**(1): p. 013303.
28. Hadziioannou G, M.G., *Semiconducting Polymers: Chemistry, Physics and Engineering, 2nd Edition, Two-Volume Set*. Polymer Science and Technology. 2006: Wiley. 768.
29. Klauk, H., et al., *High-mobility polymer gate dielectric pentacene thin film transistors.* Journal of Applied Physics, 2002. **92**(9): p. 5259-5263.
30. Babel, A. and S.A. Jenekhe, *High Electron Mobility in Ladder Polymer Field-Effect Transistors.* Journal of the American Chemical Society, 2003. **125**(45): p. 13656-13657.
31. Sirringhaus, H., *Device Physics of Solution-Processed Organic Field-Effect Transistors.* Advanced Materials, 2005. **17**(20): p. 2411-2425.
32. Shockley, W., *A Unipolar "Field-Effect" Transistor.* Proceedings of the IRE, 1952. **40**(11): p. 1365-1376.
33. Kang, H., et al., *High-Performance Printed Transistors Realized Using Femtoliter Gravure-Printed Sub-10 µm Metallic Nanoparticle Patterns and Highly Uniform Polymer Dielectric and Semiconductor Layers.* Advanced Materials, 2012: p. n/a-n/a.
34. Moonen, P.F., I. Yakimets, and J. Huskens, *Fabrication of Transistors on Flexible Substrates: from Mass-Printing to High-Resolution Alternative Lithography Strategies.* Advanced Materials, 2012: p. n/a-n/a.
35. Lorenz, A., et al., *Evaluation of Flexographic Printing Technology for Multi-busbar Solar Cells.* Energy Procedia, 2015. **67**: p. 126-137.
36. Kwak, D., et al., *Self-Organization of Inkjet-Printed Organic Semiconductor Films Prepared in Inkjet-Etched Microwells.* Advanced Functional Materials, 2013: p. n/a-n/a.
37. Zhang, L., et al., *Inkjet Printing High-Resolution, Large-Area Graphene Patterns by Coffee-Ring Lithography.* Advanced Materials, 2012. **24**(3): p. 436-440.

38. Zhang, J., et al., *Inkjet-Printed Organic Electrodes for Bottom-Contact Organic Field-Effect Transistors.* Advanced Functional Materials, 2011. **21**(4): p. 786-791.
39. Fischer, K. and R. Suss. *Spray coating - a solution for resist film deposition across severe topography*. in *Electronics Manufacturing Technology Symposium, 2004. IEEE/CPMT/SEMI 29th International*. 2004.
40. Chou, W.Y., et al., *Application of nanoimprinting technology to organic field-effect transistors.* Applied Physics Letters, 2010. **96**(8).
41. Cho, J., K.-H. Shin, and J. Jang, *Micropatterning of conducting polymer tracks on plasma treated flexible substrate using vapor phase polymerization-mediated inkjet printing.* Synthetic Metals, 2010. **160**(9-10): p. 1119-1125.
42. Smith, J.T., et al., *Reducing Contact Resistance in Graphene Devices through Contact Area Patterning.* ACS Nano, 2013.
43. Thornton, M.J., et al., *Nanoimprinted lithography high performance in-plane organic diodes*. Vol. 99. 2011: AIP. 173301.
44. Fukuda, K., et al., *Fully-printed high-performance organic thin-film transistors and circuitry on one-micron-thick polymer films.* Nat Commun, 2014. **5**.
45. Gili, E., M. Caironi, and H. Sirringhaus, *Organic integrated complementary inverters with ink-jet printed source/drain electrodes and sub-micron channels.* Applied Physics Letters, 2012. **100**(12): p. 123303.
46. Zhao, Y., et al., *All-Solution-Processed, High-Performance n-Channel Organic Transistors and Circuits: Toward Low-Cost Ambient Electronics.* Advanced Materials, 2011. **23**(21): p. 2448-2453.
47. Hong, K., et al., *Printed, sub-2V ZnO Electrolyte Gated Transistors and Inverters on Plastic.* Advanced Materials, 2013: p. n/a-n/a.
48. Kim, S.-J. and J.-S. Lee, *Flexible Organic Transistor Memory Devices.* Nano Letters, 2010: p. null-null.
49. Fujisaki, Y., et al., *Air-stable n-type organic thin-film transistor array and high gain complementary inverter on flexible substrate.* Applied Physics Letters, 2010. **97**(13): p. 133303.
50. Horowitz, G., et al., *The Concept of "Threshold Voltage" in Organic Field-Effect Transistors.* Advanced Materials, 1998. **10**(12): p. 923-927.
51. Harun, M.H., et al., *Conjugated conducting polymers: A brief overview.* UCSI Academic Journal: Journal for the Advancement of Science & Arts, 2007. **2**: p. 63-68.
52. Chiang, C.K., et al., *Electrical Conductivity in Doped Polyacetylene.* Physical Review Letters, 1977. **39**(17): p. 1098-1101.
53. MacDiarmid, A.G. and A.J. Heeger, *Symposium on the Structure and Properties of Highly Conducting Polymers and GraphiteOrganic metals and semiconductors: The chemistry of polyacetylene, (CH)x, and its derivatives.* Synthetic Metals, 1980. **1**(2): p. 101-118.
54. Koezuka, H., A. Tsumura, and T. Ando, *FIELD-EFFECT TRANSISTOR WITH POLYTHIOPHENE THIN-FILM.* Synthetic Metals, 1987. **18**(1-3): p. 699-704.
55. Bredas, J.-L., *Mind the gap!* Materials Horizons, 2014. **1**(1): p. 17-19.

56. Bielecka, U., et al., *Effect of solution aging on morphology and electrical characteristics of regioregular P3HT FETs fabricated by spin coating and spray coating.* Organic Electronics. **In Press, Uncorrected Proof**.
57. Chang, P.C., et al., *Film Morphology and Thin Film Transistor Performance of Solution-Processed Oligothiophenes.* Chemistry of Materials, 2004. **16**(23): p. 4783-4789.
58. Kline, R.J., et al., *Dependence of Regioregular Poly(3-hexylthiophene) Film Morphology and Field-Effect Mobility on Molecular Weight.* Macromolecules, 2005. **38**(8): p. 3312-3319.
59. Majewski, L.A., et al., *Influence of processing conditions on the stability of poly(3-hexylthiophene)-based field-effect transistors.* Applied Physics Letters, 2006. **88**(22): p. 222108.
60. Tsao, H.N., et al., *The Influence of Morphology on High-Performance Polymer Field-Effect Transistors.* Advanced Materials, 2009. **21**(2): p. 209-212.
61. Meijer, E.J., et al., *Scaling behavior and parasitic series resistance in disordered organic field-effect transistors.* Applied Physics Letters, 2003. **82**(25): p. 4576-4578.
62. Ullah, M., et al., *Electrical response of highly ordered organic thin film metal-insulator-semiconductor devices.* Journal of Applied Physics, 2009. **106**(11): p. 114505.
63. Horowitz, G., R. Hajlaoui, and P. Delannoy, *Temperature Dependence of the Field-Effect Mobility of Sexithiophene. Determination of the Density of Traps.* Journal de Physique III, 1995. **5**(4): p. 355-371.
64. Colson, R. and P. Nagels, *The electrical properties of amorphous polymers described by a modified variable-range hopping model.* Journal of Non-Crystalline Solids, 1980. **35**: p. 129-134.
65. Maddison, D.S. and T.L. Tansley, *Variable range hopping in polypyrrole films of a range of conductivities and preparation methods.* Journal of Applied Physics, 1992. **72**(10): p. 4677-4682.
66. Tripathi, A.K., et al., *Charge transport in solution processable polycrystalline dual-gate organic field effect transistors*. Vol. 98. 2011: AIP. 202106.
67. Sirringhaus, H., et al., *Two-dimensional charge transport in self-organized, high-mobility conjugated polymers.* Nature, 1999. **401**(6754): p. 685-688.
68. Valizadeh, P., *Electronic Materials and Charge Transport*, in *Field Effect Transistors, A Comprehensive Overview*. 2016, John Wiley & Sons, Inc. p. 1-118.
69. Crone, B., et al., *Large-scale complementary integrated circuits based on organic transistors.* Nature, 2000. **403**(6769): p. 521-523.
70. Lian, K., et al., *DC and AC Analyses of a Printed Flexible Memory Device.* Organic Electronics. **In Press, Accepted Manuscript**.
71. Ong, B.S., et al., *High-Performance Semiconducting Polythiophenes for Organic Thin-Film Transistors.* Journal of the American Chemical Society, 2004. **126**(11): p. 3378-3379.
72. McCulloch, I., et al., *Liquid-crystalline semiconducting polymers with high charge-carrier mobility.* Nat Mater, 2006. **5**(4): p. 328-333.

73. Rogers, J.A., et al., *Paper-like electronic displays: Large-area rubber-stamped plastic sheets of electronics and microencapsulated electrophoretic inks.* Proceedings of the National Academy of Sciences, 2001. **98**(9): p. 4835-4840.
74. Dodabalapur, A., *Organic and polymer transistors for electronics.* Materials Today, 2006. **9**(4): p. 24-30.
75. Gelinck, G., et al., *Organic Transistors in Optical Displays and Microelectronic Applications.* Advanced Materials, 2010. **22**(34): p. 3778-3798.
76. Soeda, J., et al., *High Electron Mobility in Air for N,N'-1H,1H-Perfluorobutyldicyanoperylene Carboxydi-imide Solution-Crystallized Thin-Film Transistors on Hydrophobic Surfaces.* Advanced Materials, 2011. **23**(32): p. 3681-3685.
77. Liang, Z., et al., *Soluble and Stable N-Heteropentacenes with High Field-Effect Mobility.* Advanced Materials, 2011: p. n/a-n/a.
78. Jiang, H., et al., *Organic Field-Effect Transistors: High-Performance Organic Single-Crystal Field-Effect Transistors of Indolo[3,2-b]carbazole and Their Potential Applications in Gas Controlled Organic Memory Devices (Adv. Mater. 43/2011).* Advanced Materials, 2011. **23**(43): p. 5074-5074.
79. Ha, T.-J., P. Sonar, and A. Dodabalapur, *High mobility top-gate and dual-gate polymer thin-film transistors based on diketopyrrolopyrrole-naphthalene copolymer*. Vol. 98. 2011: AIP. 253305.
80. Sonar, P., et al., *Synthesis, characterization and comparative OFET behaviour of indenofluorene-bithiophene and terthiophene alternating copolymers.* Synthetic Metals, 2010. **160**(5-6): p. 468-474.
81. Li, Y., S.P. Singh, and P. Sonar, *A High Mobility P-Type DPP-Thieno[3,2-b]thiophene Copolymer for Organic Thin-Film Transistors.* Advanced Materials, 2010: p. n/a-n/a.
82. Oh, J.H., et al., *Air-stable n-channel organic thin-film transistors with high field-effect mobility based on N,N[sup [prime]]-bis(heptafluorobutyl)-3,4:9,10-perylene diimide.* Applied Physics Letters, 2007. **91**(21): p. 212107.
83. Jones, B.A., et al., *High-Mobility Air-Stable n-Type Semiconductors with Processing Versatility: Dicyanoperylene-3,4:9,10-bis(dicarboximides)13.* Angewandte Chemie, 2004. **116**(46): p. 6523-6526.
84. Kim, J.H., et al., *Remarkable Mobility Increase and Threshold Voltage Reduction in Organic Field-Effect Transistors by Overlaying Discontinuous Nano-Patches of Charge-Transfer Doping Layer on Top of Semiconducting Film.* Advanced Materials, 2013. **25**(5): p. 719-724.
85. Kim, F.S., et al., *Enhanced carrier mobility and electrical stability of n-channel polymer thin film transistors by use of low-k dielectric buffer layer*. Vol. 99. 2011: AIP. 173303.
86. Tsukagoshi, K., et al., *Interface modification of a pentacene field-effect transistor with a submicron channel.* Applied Physics Letters, 2006. **89**(11): p. 113507.
87. Zhang, H., et al., *Interface Engineering of Semiconductor/Dielectric Heterojunctions toward Functional Organic Thin-Film Transistors.* Nano Letters, 2011.
88. Wang, S.D., Y. Yan, and K. Tsukagoshi, *Understanding contact behavior in organic thin film transistors.* Applied Physics Letters, 2010. **97**(6).

89. Stadler, P., et al., *The role of the dielectric interface in organic transistors: A combined device and photoemission study.* Organic Electronics, 2010. **11**(2): p. 207-211.
90. Horowitz, G., *Interfaces in Organic Field-Effect Transistors*, in *Organic Electronics*, T. Grasser, G. Meller, and L. Li, Editors. 2010, Springer Berlin / Heidelberg. p. 113-153.
91. Yildirim, F.A., et al., *Gate insulators and interface effects in organic thin-film transistors.* Organic Electronics, 2008. **9**(1): p. 70-76.
92. Yang, H., et al., *Effect of Mesoscale Crystalline Structure on the Field-Effect Mobility of Regioregular Poly(3-hexyl thiophene) in Thin-Film Transistors.* Advanced Functional Materials, 2005. **15**(4): p. 671-676.
93. Mas-Torrent, M., et al., *Correlation between Crystal Structure and Mobility in Organic Field-Effect Transistors Based on Single Crystals of Tetrathiafulvalene Derivatives.* Journal of the American Chemical Society, 2004. **126**(27): p. 8546-8553.
94. Panzer, M.J. and C.D. Frisbie, *High charge carrier densities and conductance maxima in single-crystal organic field-effect transistors with a polymer electrolyte gate dielectric.* Applied Physics Letters, 2006. **88**(20): p. 203504.
95. Baeg, K.-J., et al., *Remarkable Enhancement of Hole Transport in Top-Gated N-Type Polymer Field-Effect Transistors by a High-k Dielectric for Ambipolar Electronic Circuits.* Advanced Materials, 2012: p. n/a-n/a.
96. Wang, C.-H., C.-Y. Hsieh, and J.-C. Hwang, *Flexible Organic Thin-Film Transistors with Silk Fibroin as the Gate Dielectric.* Advanced Materials, 2010: p. n/a-n/a.
97. Walser, M.P., et al., *Stable complementary inverters with organic field-effect transistors on Cytop fluoropolymer gate dielectric.* Applied Physics Letters, 2009. **94**(5): p. -.
98. Ortiz, R.o.P., A. Facchetti, and T.J. Marks, *High-k Organic, Inorganic, and Hybrid Dielectrics for Low-Voltage Organic Field-Effect Transistors.* Chemical Reviews, 2009. **110**(1): p. 205-239.
99. Facchetti, A., M.-H. Yoon, and T.J. Marks, *Gate Dielectrics for Organic Field-Effect Transistors: New Opportunities for Organic Electronics.* Advanced Materials, 2005. **17**(14): p. 1705-1725.
100. Chua, L.-L., et al., *High-stability ultrathin spin-on benzocyclobutene gate dielectric for polymer field-effect transistors.* Applied Physics Letters, 2004. **84**(17): p. 3400-3402.
101. Rapisarda, M., et al., *Analysis of contact effects in fully printed p-channel organic thin film transistors.* Organic Electronics, 2012. **13**(10): p. 2017-2027.
102. Valletta, A., et al., *Contact effects in high performance fully printed p-channel organic thin film transistors.* Applied Physics Letters, 2011. **99**(23): p. 233309.
103. Gruber, M., et al., *Impact of Materials versus Geometric Parameters on the Contact Resistance in Organic Thin-Film Transistors.* Advanced Functional Materials, 2013: p. n/a-n/a.
104. Ante, F., et al., *Contact Resistance and Megahertz Operation of Aggressively Scaled Organic Transistors.* Small, 2012. **8**(1): p. 73-79.

105. Richards, T.J. and H. Sirringhaus, *Analysis of the contact resistance in staggered, top-gate organic field-effect transistors.* Journal of Applied Physics, 2007. **102**(9): p. 094510.
106. Natali, D., L. Fumagalli, and M. Sampietro, *Modeling of organic thin film transistors: Effect of contact resistances.* Journal of Applied Physics, 2007. **101**(1): p. 014501.
107. Nakahara, R., et al., *Flexible Three-Dimensional Organic Field-Effect Transistors Fabricated by an Imprinting Technique.* Advanced Materials, 2012. **24**(38): p. 5212-5216.
108. Tseng, H.-Y., et al., *High-speed organic transistors fabricated using a novel hybrid-printing technique.* Organic Electronics, 2011. **12**(7): p. 1120-1125.
109. Yang, S.Y., et al., *Low-voltage pentacene field-effect transistors with ultrathin polymer gate dielectrics.* Applied Physics Letters, 2006. **88**(17): p. 173507.
110. Moradi, M., A.A. Fomani, and A. Nathan, *Effect of gate dielectric scaling in nanometer scale vertical thin film transistors.* Applied Physics Letters, 2011. **99**(22): p. 223503.
111. Haddock, J.N., et al., *A comprehensive study of short channel effects in organic field-effect transistors.* Organic Electronics, 2006. **7**(1): p. 45-54.
112. Wang, J.Z., Z.H. Zheng, and H. Sirringhaus, *Suppression of short-channel effects in organic thin-film transistors.* Applied Physics Letters, 2006. **89**(8): p. 083513.
113. Leufgen, M., et al., *Optimized sub-micron organic thin-film transistors: the influence of contacts and oxide thickness.* Synthetic Metals, 2004. **146**(3): p. 341-345.
114. Meijer, E.J., et al., *Scaling behavior and parasitic series resistance in disordered organic field-effect transistors.* Applied Physics Letters, 2003. **82**(25): p. 4576-4578.
115. Ma, L. and Y. Yang, *Unique architecture and concept for high-performance organic transistors.* Applied Physics Letters, 2004. **85**(21): p. 5084-5086.
116. Li, S.H., et al., *Achieving ambipolar vertical organic transistors via nanoscale interface modification.* Applied Physics Letters, 2007. **91**(8).
117. Xu, Z., et al., *Vertical organic light emitting transistor.* Applied Physics Letters, 2007. **91**(9): p. 092911.
118. Li, S.H., et al., *Solution-processed poly(3-hexylthiophene) vertical organic transistor.* Applied Physics Letters, 2008. **93**(21).
119. Liu, B., et al., *Carbon-Nanotube-Enabled Vertical Field Effect and Light-Emitting Transistors.* Advanced Materials, 2008. **20**(19): p. 3605-3609.
120. Ben-Sasson, A.J., et al., *Patterned electrode vertical field effect transistor fabricated using block copolymer nanotemplates.* Applied Physics Letters, 2009. **95**(21): p. 213301.
121. Jiang, J., et al., *Vertical low-voltage oxide transistors gated by microporous SiO2/LiCl composite solid electrolyte with enhanced electric-double-layer capacitance.* Applied Physics Letters, 2010. **97**(5): p. 052104.
122. McCarthy, M.A., B. Liu, and A.G. Rinzler, *High Current, Low Voltage Carbon Nanotube Enabled Vertical Organic Field Effect Transistors.* Nano Letters, 2010. **10**(9): p. 3467-3472.

123. Ben-Sasson, A.J. and N. Tessler, *Patterned electrode vertical field effect transistor: Theory and experiment*. Vol. 110. 2011: AIP. 044501.
124. Ben-Sasson, A.J. and N. Tessler. *Patterned electrode vertical OFET: analytical description, switching mechanisms, and optimization rules*. 2011.
125. Chao, Y.-C., et al., *High-performance vertical polymer nanorod transistors based on air-stable conjugated polymer.* Applied Physics Letters, 2011. **99**(23): p. 233308.
126. Chao, Y.-C., et al., *High-mobility polymer space–charge-limited transistor with grid-induced crystallinity.* Organic Electronics, 2011. **12**(1): p. 78-82.
127. McCarthy, M.A., et al., *Reorientation of the High Mobility Plane in Pentacene-Based Carbon Nanotube Enabled Vertical Field Effect Transistors.* ACS Nano, 2011. **5**(1): p. 291-298.
128. Puri, M. and S. Bhanja. *13,6-N-sulfinylacetamidopentacene based Fully Encapsulated Low Voltage Vertical Short Channel OFET*. in *Renewable Energy and the Environment*. 2011. Austin, Texas: Optical Society of America.
129. Rossi, L., et al., *Low voltage vertical organic field-effect transistor with polyvinyl alcohol as gate insulator.* Journal of Applied Physics, 2011. **110**(9): p. 094508.
130. Ben-Sasson, A.J., et al., *Solution-processed ambipolar vertical organic field effect transistor.* Applied Physics Letters, 2012. **100**(26): p. 263306.
131. Ben-Sasson, A.J. and N. Tessler, *Unraveling the Physics of Vertical Organic Field Effect Transistors through Nanoscale Engineering of a Self-Assembled Transparent Electrode.* Nano Letters, 2012. **12**(9): p. 4729-4733.
132. Mehr, W., et al., *Vertical Graphene Base Transistor.* Electron Device Letters, IEEE, 2012. **33**(5): p. 691-693.
133. Wang, P.-H., et al., *N-channel carbon nanotube enabled vertical field effect transistors with solution deposited ZnO nanoparticle based channel layers.* Applied Physics Letters, 2012. **100**(17): p. 173514.
134. Ben-Sasson, A.J., et al., *Low-Temperature Molecular Vapor Deposition of Ultrathin Metal Oxide Dielectric for Low-Voltage Vertical Organic Field Effect Transistors.* ACS Applied Materials & Interfaces, 2013. **5**(7): p. 2462-2468.
135. Chen, W., A.G. Rinzler, and J. Guo, *Modeling and simulation of carbon nanotube-semiconductor heterojunction vertical field effect transistors.* Journal of Applied Physics, 2013. **113**(23): p. 234501.
136. Di Lecce, V., et al., *Graphene Base Transistors: A Simulation Study of DC and Small-Signal Operation.* Electron Devices, IEEE Transactions on, 2013. **60**(10): p. 3584-3591.
137. Georgiou, T., et al., *Vertical field-effect transistor based on graphene-WS2 heterostructures for flexible and transparent electronics.* Nat Nano, 2013. **8**(2): p. 100-103.
138. Greenman, M., et al., *Fast switching characteristics in vertical organic field effect transistors.* Applied Physics Letters, 2013. **103**(7): p. 073502.
139. Kleemann, H., et al., *High-Performance Vertical Organic Transistors.* Small, 2013: p. n/a-n/a.
140. Seidel, K., et al., *Vertical organic field effect transistor using sulfonated polyaniline/aluminum bilayer as intermediate electrode.* Journal of Materials Science: Materials in Electronics, 2013. **24**(3): p. 1052-1056.

141. Ben-Sasson, A.J., et al., *The Mechanism of Operation of Lateral and Vertical Organic Field Effect Transistors.* Israel Journal of Chemistry, 2014. **54**(5-6): p. 568-585.
142. Keum, C.M., et al., *Quasi-surface emission in vertical organic light-emitting transistors with network electrode.* Optics Express, 2014. **22**(12): p. 14750-14756.
143. Ben-Sasson, A.J., et al., *Self-Assembled Metallic Nanowire-Based Vertical Organic Field-Effect Transistor.* Acs Applied Materials & Interfaces, 2015. **7**(4): p. 2149-2152.
144. Hlaing, H., et al., *Low-Voltage Organic Electronics Based on a Gate-Tunable Injection Barrier in Vertical graphene-organic Semiconductor Heterostructures.* Nano Letters, 2015. **15**(1): p. 69-74.
145. Vaziri, S., et al., *Bilayer insulator tunnel barriers for graphene-based vertical hot-electron transistors.* Nanoscale, 2015. **7**(30): p. 13096-13104.
146. Yang, D., et al., *Pentacene-Based Photodetector in Visible Region With Vertical Field-Effect Transistor Configuration.* Ieee Photonics Technology Letters, 2015. **27**(3): p. 233-236.
147. Fujimoto, S.-y., K.-i. Nakayama, and M. Yokoyama, *Fabrication of a vertical-type organic transistor with a planar metal base.* Applied Physics Letters, 2005. **87**(13): p. 133503.
148. Parashkov, R., et al., *Vertical channel all-organic thin-film transistors.* Applied Physics Letters, 2003. **82**(25): p. 4579-4580.
149. He, J., et al., *Three-terminal organic memory devices.* Journal of Applied Physics, 2005. **97**(6).
150. Parashkov, R., et al., *Organic vertical-channel transistors structured using excimer laser.* Applied Physics Letters, 2004. **85**(23): p. 5751-5753.
151. Di, C.-a., et al., *Noncoplanar organic field-effect transistor based on copper phthalocyanine.* Applied Physics Letters, 2006. **88**(12): p. 121907.
152. Liu, J., et al., *Vertical polyelectrolyte-gated organic field-effect transistors.* Applied Physics Letters, 2010. **97**(10): p. 103303.
153. Chen, Y. and I. Shih, *Fabrication of vertical channel top contact organic thin film transistors.* Organic Electronics, 2007. **8**(6): p. 655-661.
154. Zhang, J., et al., *Organic thin-film transistors in sandwich configuration.* Applied Physics Letters, 2004. **84**(1): p. 142-144.
155. Shaw, J.G. and M. Hack, *Vertical amorphous silicon thin-film transistors.* Journal of Applied Physics, 1990. **67**(3): p. 1576-1581.
156. Fujimoto, S.-y., K.-i. Nakayama, and M. Yokoyama, *Fabrication of a vertical-type organic transistor with a planar metal base.* Applied Physics Letters, 2005. **87**(13): p. 133503-3.
157. Yi, M., et al., *Vertical n-type organic transistors with tri(8-hydroxyquinoline) aluminum as collector and fullerene as emitter.* Applied Physics Letters, 2011. **98**(7): p. 073309.
158. Stutzmann, N., R.H. Friend, and H. Sirringhaus, *Self-Aligned, Vertical-Channel, Polymer Field-Effect Transistors.* Science, 2003. **299**(5614): p. 1881-1884.
159. Yu, L.Z., H.C. Chen, and C.T. Lee, *Memory mechanisms of vertical organic memory transistors.* Applied Physics Letters, 2010. **96**(23).

160. de Jong, M.P., L.J. van IJzendoorn, and M.J.A. de Voigt, *Stability of the interface between indium-tin-oxide and poly(3,4-ethylenedioxythiophene)/poly(styrenesulfonate) in polymer light-emitting diodes.* Applied Physics Letters, 2000. **77**(14): p. 2255-2257.
161. Vitoratos, E., et al., *Thermal degradation mechanisms of PEDOT:PSS.* Organic Electronics, 2009. **10**(1): p. 61-66.
162. Chabinyc, M.L., R.A. Street, and J.E. Northrup, *Effects of molecular oxygen and ozone on polythiophene-based thin-film transistors.* Applied Physics Letters, 2007. **90**(12): p. -.
163. Khan, A.R., J. Siddique, and S.S.K. Iyer. *Advanced technique of vertical organic thin film transistor*. in *Multimedia, Signal Processing and Communication Technologies (IMPACT), 2013 International Conference on*. 2013.
164. Kaneto, K. and W. Takashima, *Fabrication and characteristics of Schottky diodes based on regioregular poly(3-hexylthiophene)/Al junction.* Current Applied Physics, 2001. **1**(4–5): p. 355-361.
165. Tung, R.T., *The physics and chemistry of the Schottky barrier height.* Applied Physics Reviews, 2014. **1**(1): p. -.
166. Kim, D., et al., *Holography and plasma oxidation for uniform nanoscale two dimensional channel formation of vertical organic field-effect transistors with suppressed gate leakage current.* Organic Electronics, 2011. **12**(11): p. 1841-1845.
167. Yang, H., et al., *Graphene Barristor, a Triode Device with a Gate-Controlled Schottky Barrier.* Science, 2012. **336**(6085): p. 1140-1143.

Chapter 2

2. Materials and Methods

Introduction

In this chapter the materials and methods associated with the fabrication, characterisation and development of devices fabricated in this thesis will be discussed. The development of the electrical platform is complimented with characterisation of various aspects of the system through contact angle measurements, atomic force microscopy and scanning electron microscopy to increase understanding of the system. These devices are further probed under various conditions through the use of AFM to determine morphological and electrical details. The methodology for current voltage characterisation is documented and the accompanying instruments to make reliable device contact and controlled atmosphere measurements detailed. Vertical wall processing of devices is described and detailed along with the methodology to fabricate a three terminal vertical wall device.

2.1 Device Preparation

Preparation of devices was undertaken primarily at Flinders University using the processes and equipment outlined below. During this dissertation the procedure for preparing individual devices will be outlined for each experiment. The instrumentation and handlings steps taken to prepare and fabricate devices generally will be discussed within this chapter.

2.1.1 Cleaning of Device Substrates

Device substrates were prepared for device fabrication through cleaning in 2% $w.v^{-1}$ pyroneg in deionised water solution. Substrates were placed in the beaker containing the pyroneg solution and heated at 50°C for 30mins on a hot plate as seen in Figure 2.1.

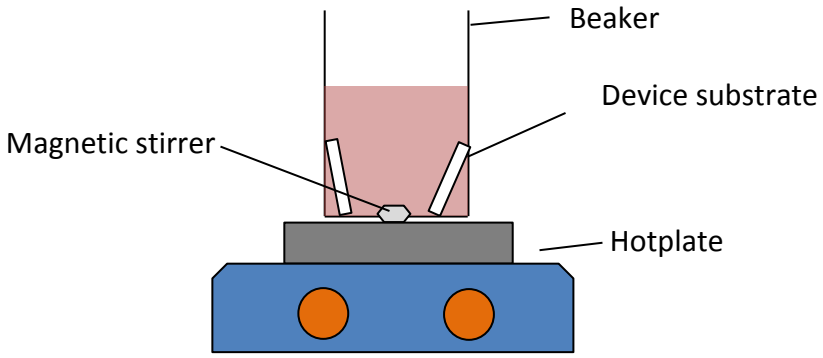

Figure 2.1. Schematic for dilute pyroneg caustic cleaning of polycarbonate substrates. Devices were immersed in the solution and heated on a low heat for 30 mins prior to device fabrication.

Substrates were handled at the edge of the substrate with tweezers and rinsed under deionised water stream for 30 seconds followed by an absolute ethanol (99.9% analytical grade, Sigma-Aldrich) rinse. Substrates are dried under a stream of nitrogen and transferred to a substrate holder until further processing.

2.1.2 Metal Evaporation

Patterned metal electrodes are deposited using a glove box installed Angstrom Covap II metal evaporation chamber. Samples are introduced into the evaporation chamber via nitrogen glove box (~0.1 ppm O_2 and H_2O) and transferred to the evaporation chamber. Substrates were mounted on a substrate holder in combination with a substrate holder mask with a top down view seen in Figure 2.2A. The substrate holder allows for a batch evaporation of seven substrates at a time. Shadow masks are created using brass metal and were designed using a CAD diagram in combination with laser cutting allowing for dimensional accuracy of ±0.01mm in pattern dimensions with an example source electrode pattern seen in Figure 2.2 B.

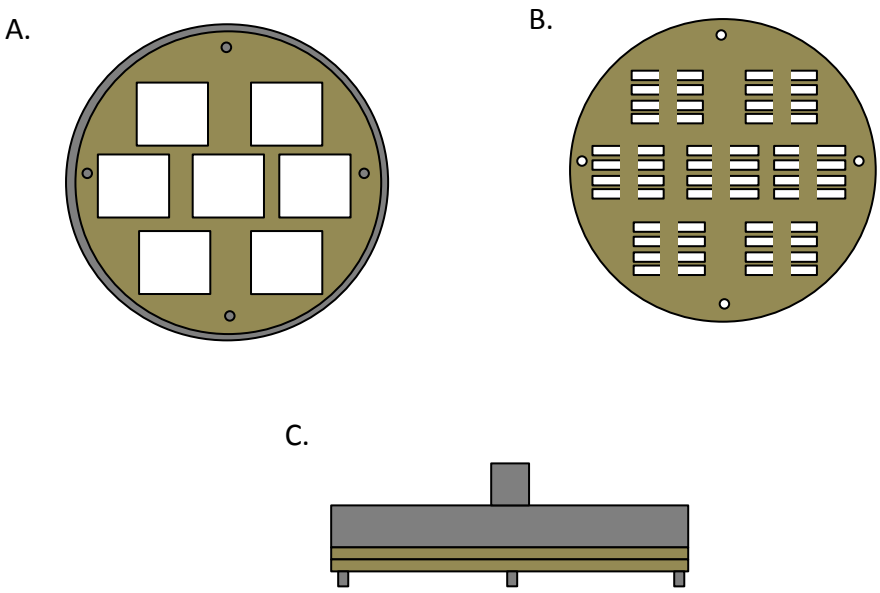

Figure 2.2. Batch metal evaporation for device substrates. A. Sample holder tray. B. Example source electrode shadow mask C. Side-on view of evaporator sample mount.

Designed shadow masks are aligned using four positioning screws that keep masks registered and aligned to the substrate holder. The resulting substrate holder and shadow mask can be seen in Figure 2.2C. The substrate holder is positioned in the evaporation chamber and evaporation is initiated. Aluminium (Angstrom, 99.999%) wire or gold pellets (Angstrom, 99.9% purity) are placed into the chamber crucible with evaporation taking place at pressure of 10^{-6} Torr with the chamber evacuated

using a turbo backing pump and rotor pump combination. Pre-programmed deposition rates were utilised in order to maintain reproducible depositions between batches. Deposition proceeded at a rate of 1Å.s^{-1} for gold and a rate of 2Å.s^{-1} for aluminium deposition.

2.1.3 Preparation of Polymer Solutions

Solutions of p-type semiconducting materials P3HT (Rieke metals, 99.9% purity, 96% regioregular, avg M_nP3HT=55,000g.mol) and Poly[*N*-9'-heptadecanyl-2,7-carbazole-*alt*-5,5-(4',7'-di-2-thienyl-2',1',3'-benzothiadiazole)], Poly[[9-(1-octylnonyl)-9H-carbazole-2,7-diyl]-2,5-thiophenediyl-2,1,3-benzothiadiazole-4,7-diyl-2,5-thiophenediyl] (PCDTBT) (Sigma-Aldrich, 99.9% purity, M_nPCDTBT= 25,500g.mol) were prepared in 15mL screw top vessels. With 1,2-dichlorobenzene (Sigma-Aldrich, 99.9% purity, analytical grade) added using a filtered syringe (PALL, 0.2µm).The chemical structures for both polymers can be seen in Figure 2.3.

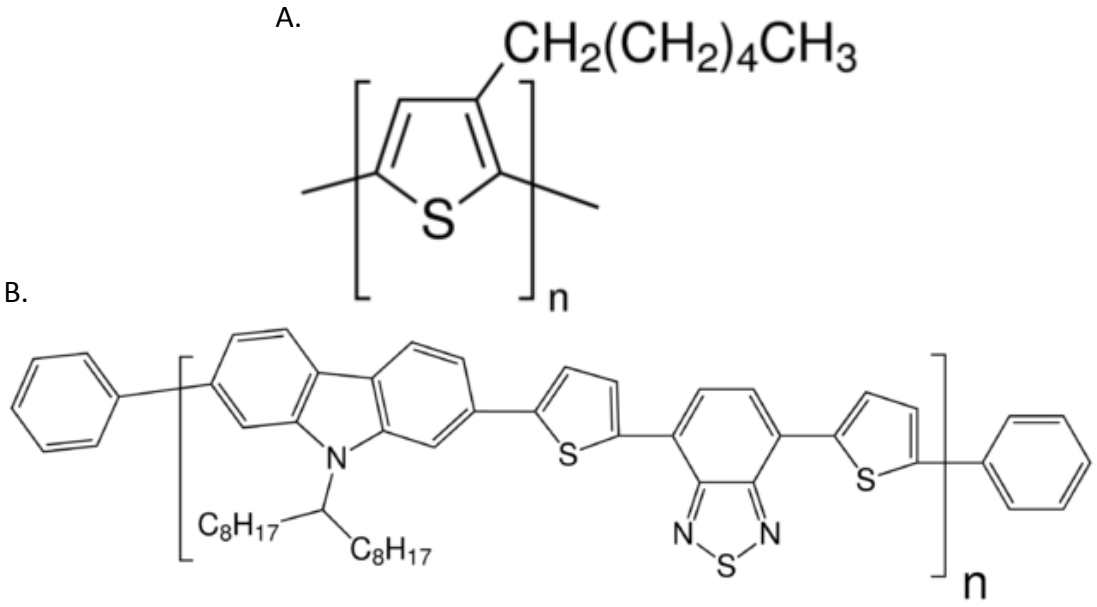

Figure 2.3. Chemical structure of semiconducting polymers. A. P3HT B. PCDTBT.

Solution vessels were first rinsed with deionised water followed by ethanol (99.9% analytical grade, Sigma-Aldrich) followed by drying under a stream of nitrogen for 10 seconds. Solutions were placed on a hot plate and heated at 50°C overnight to

ensure complete polymer dissolution. Solutions were prepared and stored in a nitrogen environment with <0.1ppm oxygen and water content.

2.1.4 Spin Coating

Thin films of polymeric and functional material were deposited onto substrates by solution processing through spin coating. The process involves an aliquot of solution being deposited onto a substrate and then rotated on the order of thousands of revolutions per minute. Centrifugal forces cause the solution to be spread across the surface forming a film of the deposited solution over the surface under advantageous surface wetting conditions. Under continuous rotation excess solution will be removed from the substrate causing a uniform reduction in the film thickness. Figure 2.4 describes the four separate stages of spin coating A. Deposition of the solution onto the substrate, B. acceleration of the substrate up to its programmed rotational speed. C. Constant rotation where film thickness is reduced by fluid viscous forces and D. Constant rotation where film thickness is reduced by solvent evaporation.[2]

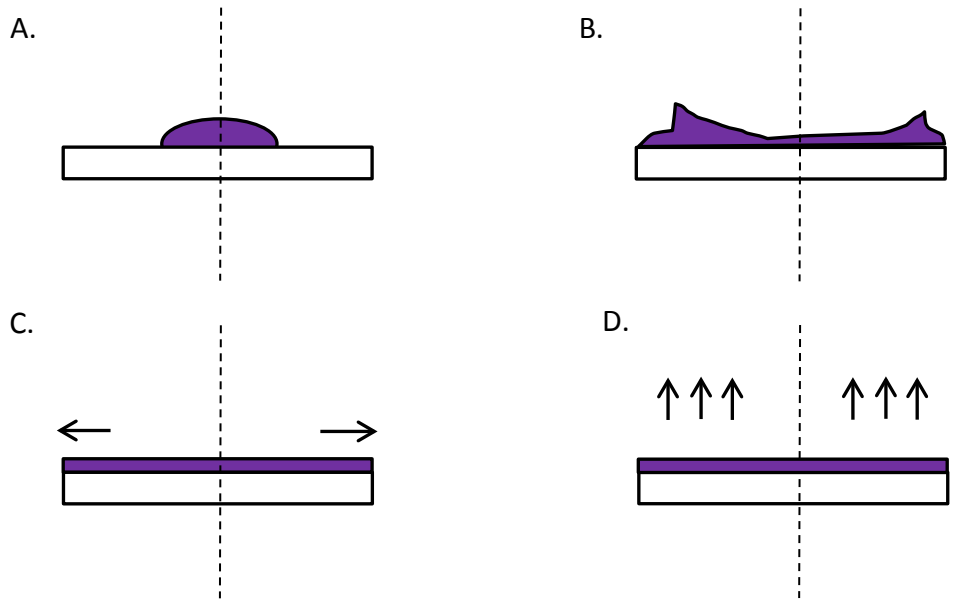

Figure 2.4. Schematic depiction of spin coating procedure. A. Deposition of solution on substrate. B. Rotation and spreading of the solution. C. Steady rotation and the removal of solution via viscous forces. D. Constant rotation where film thickness is reduced by solvent evaporation.

The substrate is secured by vacuum to a WS-400A-6nPP/LITE (Laurell Technologies, North Wales, Pennsylvania, USA) spin coater. An aliquot of solution is deposited on to the

patterned electrode area. And spin coated at various spin speeds for 30 seconds. The thickness of the resulting film is dependent on spin speed.[2]Figure 2.5 shows the programmed spin speed cycles for polymer solution spin casting.

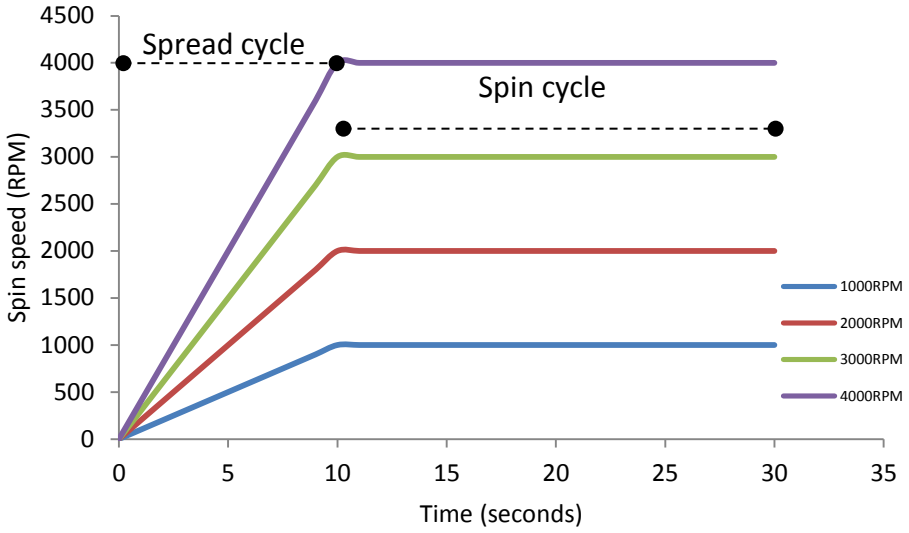

Figure 2.5. Spin coater spin speed vs. time pre-programmed deposition cycles for four recipes. 1000RPM (blue) 2000RPM (red) 3000RPM (green) 4000RPM (purple).

The programmed spin cycles feature a 10 seconds spread cycle as spin speed reaches programmed speed. During this phase solution spreads across the patterned electrode surface and excess polymer solution is removed off the surface as it reaches the programmed spin speed. Once the spin speed has been reached a 20 second spin cycle is implemented which planarises the resulting thin film. After the spin cycle is finished the substrate is transferred to a hotplate for annealing.

2.1.5. Spin Coating of Polymer Solutions

Prior to deposition of polymer solution solutions are left to equilibrate to room temperature for 30mins. A 10uL aliquot of polymer solution is pipetted onto the centre of gold patterned substrates covering electrodes in polymer solution (Figure 2.6B). Samples were then spin coated using a programmed spin cycle (Figure 2.6C). Spin coated samples were transferred to an adjacent hot plate for annealing to remove residual solvent and anneal thin films of P3HT (Figure 2.6D).

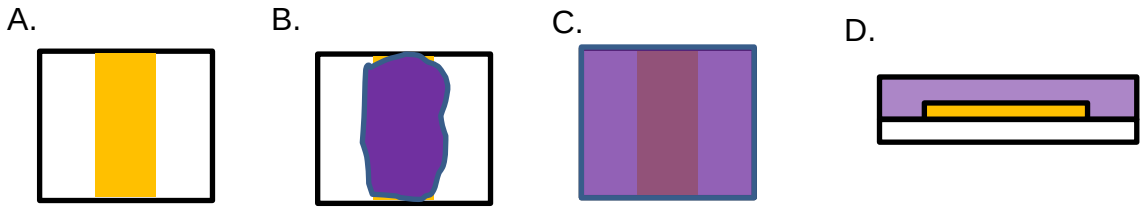

Figure 2.6. Spin coating procedure undertaken in the spin coating of thin polymeric films. A. Top view of a cleaned polycarbonate substrate with patterned electrodes. B. Top view of 10µL aliquot of polymer solution in solvent deposited across the centre of patterned electrodes .C. Top view of spin cast substrate between 500RPM-3000RPM creating a thin film. D. Side view of completed spin cast samples.

2.1.6 Planar Devices

Planar OFET devices were fabricated with the organic semiconductor Tri-isopropyl-silane - di-benzo chrysene (TIPS DBC) seen in Figure 2.7. TIPS-DBC was synthesised in house,[3] and was dissolved in chloroform (99.5% purity obtained from Merck) at a concentration of 15 $mg.mL^{-1}$. Planar devices used benzo-cyclo butane (Cyclotene 3000 BCB, obtained from DOW) as a solution processed dielectric in top contact devices with the chemical structure seen in Figure 2.7B. It was spin-coated at 1000RPM in air followed by a thermal cure at 250 °C overnight, under vacuum to give a smooth amorphous dielectric coating, with surface roughness measured at between 2-3 nm, consistent with previous reports.[4]

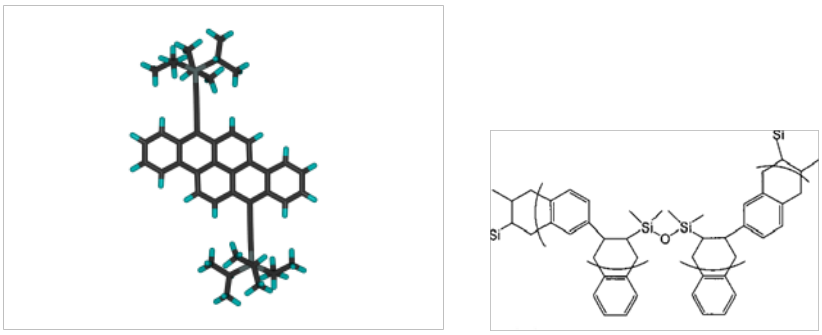

Figure 2.7. Chemical structure of materials in planar OFET structures. A. TIPS-DBC B. BCB

2.1.6.1 Top Contact Devices

Top contact devices were fabricated in a glove box by either drop casting the organic semiconductor layers or spin-coating at various speeds from chloroform solutions and annealed at 100 °C for 5 mins on glass substrates with patterned indium tin oxide (ITO) gate electrode. The top contact electrodes were thermally evaporated at a rate of 1 Å.s^{-1} under base pressure of a 1×10^{-6} mbar. Without any further treatment the completed devices were transported to another glove box fitted with a probe station to analyse the devices.

2.1.6.1 Bottom Contact Devices

Bottom-contact OFET devices were fabricated on photo lithographically patterned Au/SiO_2/Si substrates. A doped (N ~ 3×10^{17} cm^{-3}) Si wafer was used as a substrate and as the gate electrode. Thermally grown smooth silicon dioxide was used as the insulating material and had a thickness of 230nm. The SiO_2 layer was first cleaned with acetone, 2-propanol and then treated with UV ozone. After the UV ozone treatment, interdigitated source and drain electrodes were photo lithographically patterned from a 50 nm sputtered gold layer. The Au electrode was modified by immersion into 15 mM pentafluorobenzenethiol (PFBT) in ethanol for 40-60 minutes and sonication in neat ethanol before blow drying with N_2. A HMDS primer was spin-coated at 4000RPM, followed by heating at 115 ºC for 5 minutes prior to deposition of the active organic semiconductor layer.

2.1.6 Two Terminal Device Processing Methodology

A general process to fabricate two terminal electrical channels using a polycarbonate substrate and semiconducting polymer was developed and is presented in Figure 2.8. Through the sequential process the resulting structure has a vertical electrical channel through the semiconducting polymer. In this configuration the electrons are injected through either of the two working electrodes and collected at the opposing working electrode. By switching the electrode through which injection happens we are allowing for the study of current-

voltage characteristics whereby the potential across the two terminals is varied and the current response is measured. The creation of the device involves these steps:

A. The preparation of a polycarbonate substrate which was cleaned in a 5% w/v pyroneg heated to 50°C by submerging polycarbonate sample in the heated solution and leaving for 30mins.
B. A UV-NVS protective coating is applied through spin casting at 1000RPM and transferred to UV housing and irradiated by an EA-160 Spectroline 365nm broad range UV panel. The UV panel produces a broad spectrum 265 to 365 nm wavelength irradiation range operating at 6W. A 1000RPM spin cycle was employed resulting in a 10μm film according to specifications.[5]
C. An electrode pattern is applied through a shadow mask by physical sputtering or evaporative deposition of metal target under vacuum. The film thickness measured *in situ* through a quartz crystal microbalance.
D. A thin film of 3% w/v polymer is cast from solvent solution over the substrate by spin coating over a range of 1000-3000RPM. Drop casting of 3% w/v solutions was also used to produce micron thick drop cast films measured through SEM cross section. Polymeric films are then annealed up to 150°C to remove residual 1,2-dichlorobenzene solvent.
E. A second electrode is deposited through shadow mask by physical sputtering or evaporative deposition with film thickness measured *in situ* through a quartz crystal microbalance.

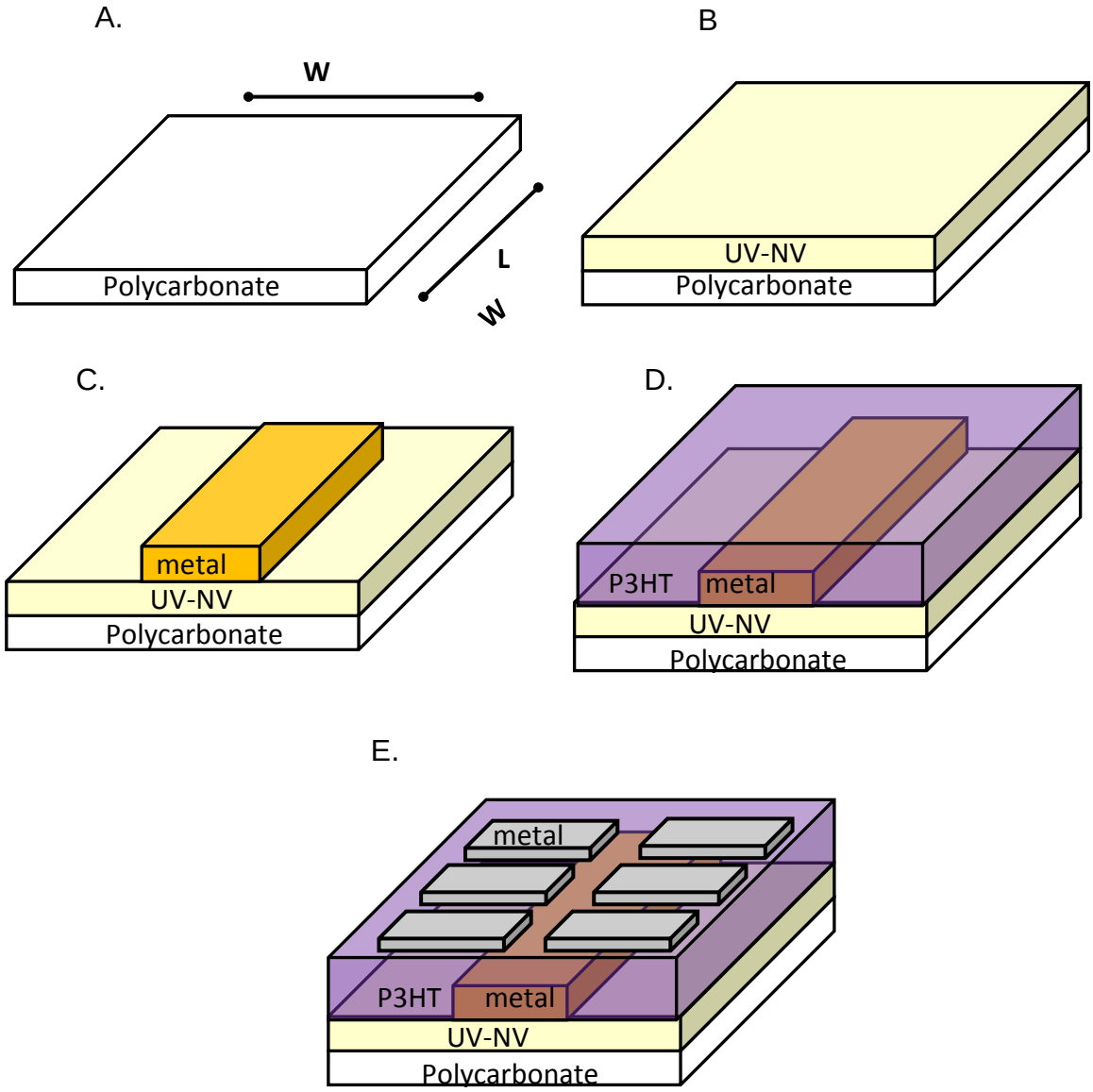

Figure 2.8. Device fabrication. A. Commercial polycarbonate sheets are laser cut to 25.4mm^2 with an accuracy of ± 0.01mm^2 and used as a working substrate. B. UV-NVS resin is spin coated onto the surface. C. A working electrode metal is deposited by means of sputtering or evaporation through a shadow mask. D. The semiconducting polymer P3HT is spin cast from solution onto working electrode and annealed. E. A second working electrode is deposited through shadow mask.

2.2 Three Terminal Device Work Flow

With two terminal device substrates fabricated using the sequential processing methodology developed in § 2.1.6. A methodology for fabricating a three terminal P3HT device was developed and is presented in Figure 2.9. The multiple step procedure includes

1. Fabrication of a two terminal electrical device on polycarbonate substrate using the sequential processing methodology for two terminal devices (described in § 2.1.5).
2. The machine cutting of two terminal device substrates using a manually aligned CNC mechanical cut. The resulting device architecture has a vertical wall introduced allowing for the deposition of a functional material.
3. A dielectric functional material is applied over the mechanical cut to provide a dielectric capacitive functional material. Dielectric functional materials were solution processed on top of two terminal device substrates at various spin speeds and different post processing for each material. UV-NVS resin was cast using the methodology described in §2.1.6B. Cytop[6] was temperature annealed at 50°C for 30mins. 1% w/v PMMA/ ethanol was heat temperature annealed at 75°C for 30mins. And $LiClO_4$: PEO electrolyte[7, 8] temperature annealed at 75°C for 30mins.
4. A conductive electrical paste is applied to function as a gate electrode across the dielectric material lateral to the two terminal conduction path.

2.2.1 Device Processing Flow Chat

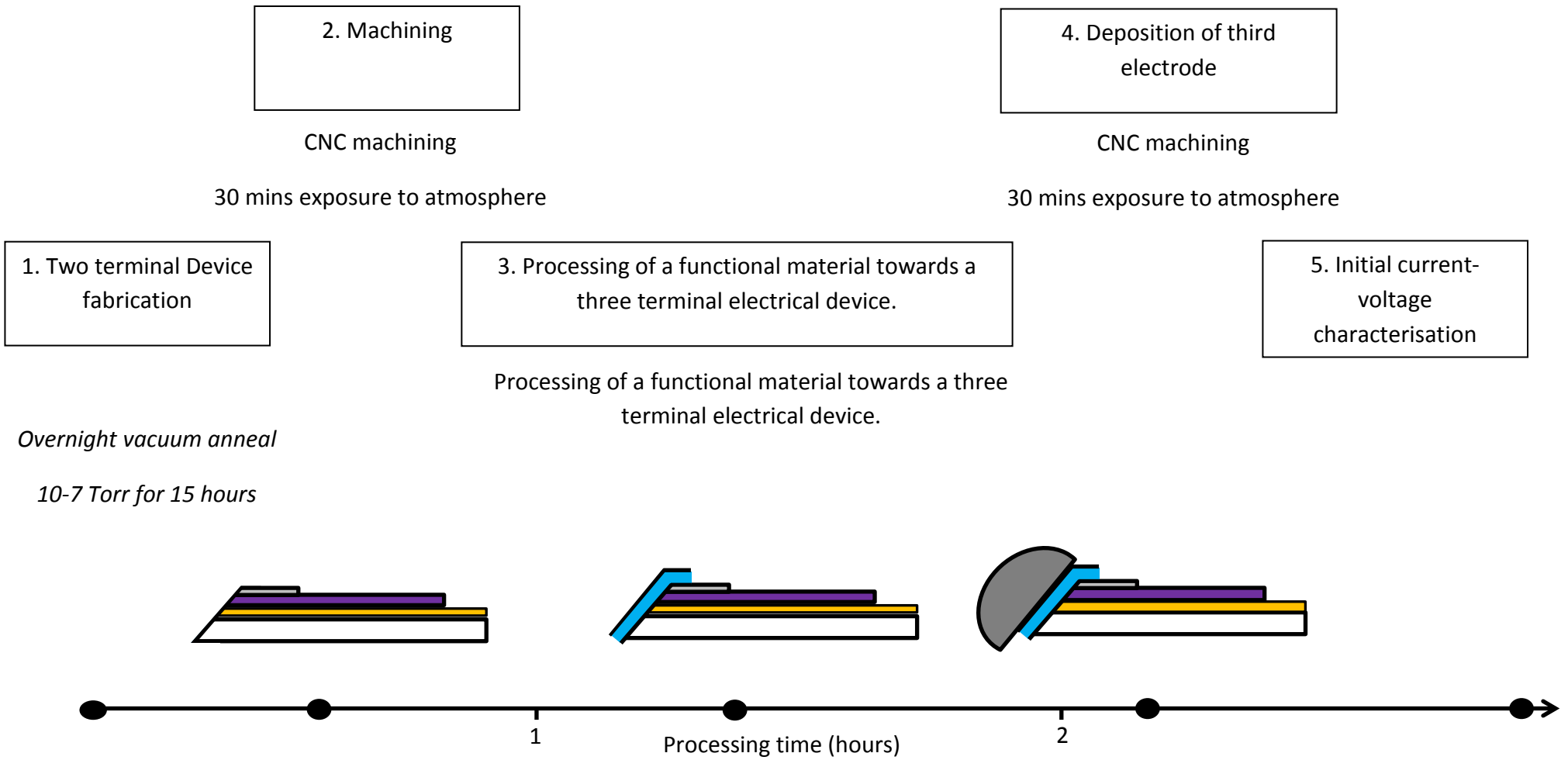

Figure 2.9. Device processing flow chart towards a three terminal device showing experimental work flow. 1. Two terminal device processing using the sequential processing methodology 2.CNC machine cut introducing a vertical wall. 3. Processing of a functional material towards a three terminal device. 4. Deposition of gate electrode. 5. Initial current-voltage characterisation.

2.3 Instrumentation

2.3.1 Contact Angle Measurements

A Sinterface PAT-1 contact angle and surface tensiometer instrument was used to measure the contact angle of surfaces to investigate the interactions between the surface and deposited materials and ensure wettability of deposited thin film solutions. Contact angle profiles were analysed using proprietary software Sinterface Profile Analysis V 3.03. For this investigation advancing contact angles are reported with a sample of five measurements taken at each point and averaged.

2.3.3 Scanning Electron Microscope

Scanning electron microscopy (SEM) produces a microscopic image of a studied surface through the interaction of a beam of electrons incident on the surface being studied. The wavelength of the incident electrons provides detail on an imaged surface beyond that of optical light due to the diffraction limit theory of optics.[9] Electron microscopy experiments are performed under vacuum in order to increase the mean free path of the incident electrons allowing for an optical path to be created. The electron beam is often produced using a tungsten filament with a high applied bias allowing for the thermionic emission of electrons. Emitted electrons are accelerated down the optical path with a potential between 500eV- 300 keV. The incident beam is focussed onto the sample through the use electromagnetic condenser lens which applies the focussed beam on a position on the surface. The beam is rastered across the surface by scanning coils.[9]During this process incident electrons may pass their energy to secondary electrons within the surface and be emitted. The secondary electrons may be ejected with a kinetic energy imparted from the interaction. The yield of secondary electrons is recorded as a function of the position of the electron beam. The secondary electrons produce an image of the surface at the position.[9] Figure 2.10A shows a schematic of a scanning electron microscope instrument.

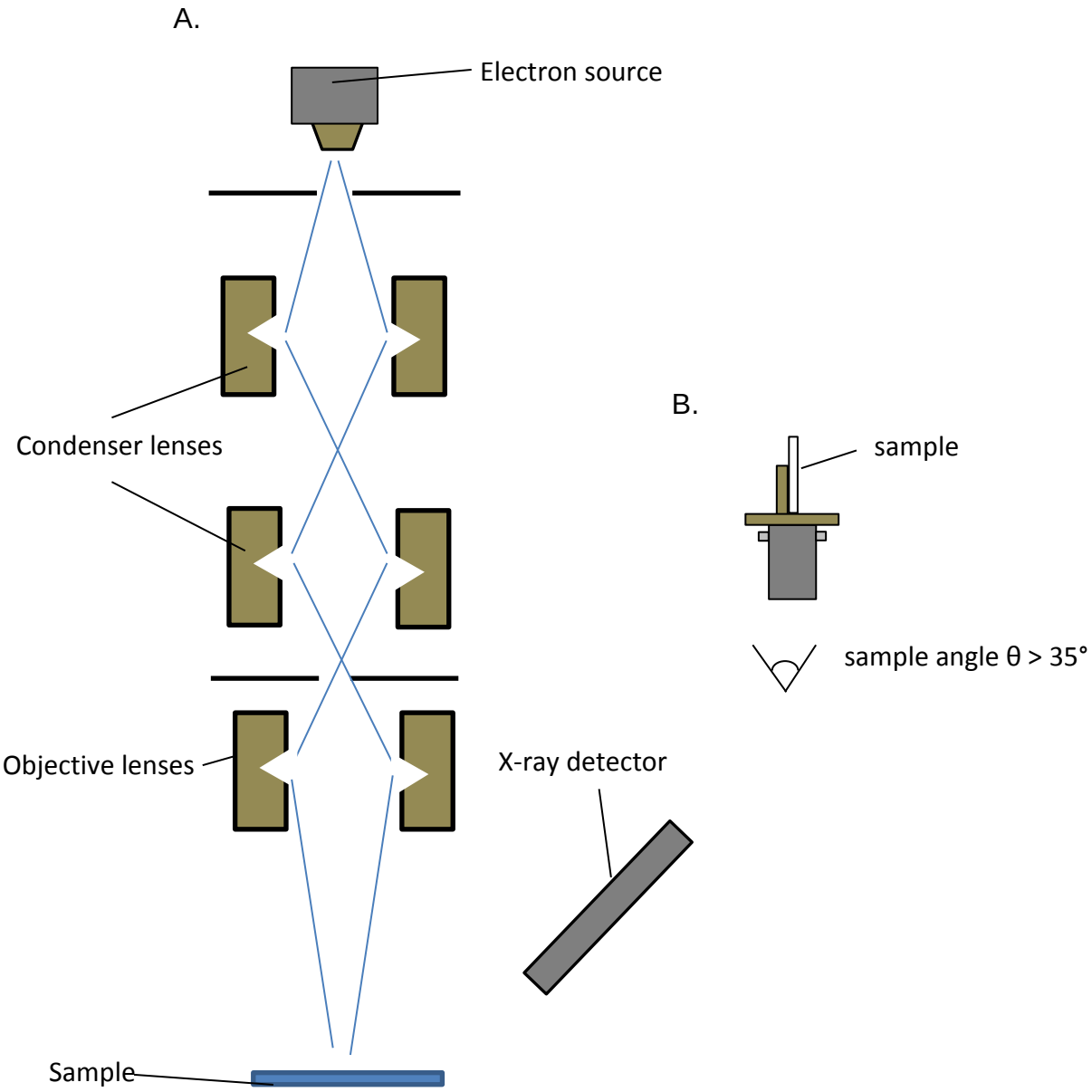

Figure 2.10. A. Schematic representation of the scanning electron microscope. An electron beam is focussed on a sample and the secondary electrons ejected from the surface and detected at a detector creating an image of the surface. B. Perpendicular sample mount stage allowing for the imaging of device cross sections.

Scanning electron microscope images in this investigation were captured using a CAMSCAN MX2500 scanning electron microscope. The microscope operated at 50 kV with an operating distance of approximately 25mm. In order to gauge the performance of various stages of the processing, a cross section view of the substrate was required. The mounting and introduction of the sample into the chamber was achieved through a modification of the SEM viewing stub and can be

seen in Figure 2.10B. The perpendicular mount allowed for the capture of SEM images of the cross section of a substrate under various degrees of device tilt relative to the detector.

2.3.3 Atomic Force Microscopy

Discovered in 1986 by Billing et al [10] atomic force microscopy (AFM) has been used extensively in the microscopy of topography in a broad range of sciences. The use of atomic force microscopy in this work allowed the effective imaging and characterisation of polymeric thin films on the near atomic scale, with sub nanometre lateral resolutions. The capabilities of AFM are in itself an evolving science, with recent developments allowing the use of conductive probe techniques to investigate the electrical properties of a surface.[11, 12] This project utilises AFM to investigate the morphological and electrical properties of thin films. It also has allowed effective measurement of thin film thicknesses through the use of step height calculations along a score in the desired film. A combination of tapping and peak force tapping mode was applied to produce images. Peak force tapping provided access to the conductive PF-TUNA module discussed below.

2.3.3.1 Instrumentation and Setup

The AFM used in this study was a commercially available Multimode Nanoscope V instrument (Digital Instruments/Veeco Metrology group CA). A schematic representation of the instrument is shown in Figure 2.11.

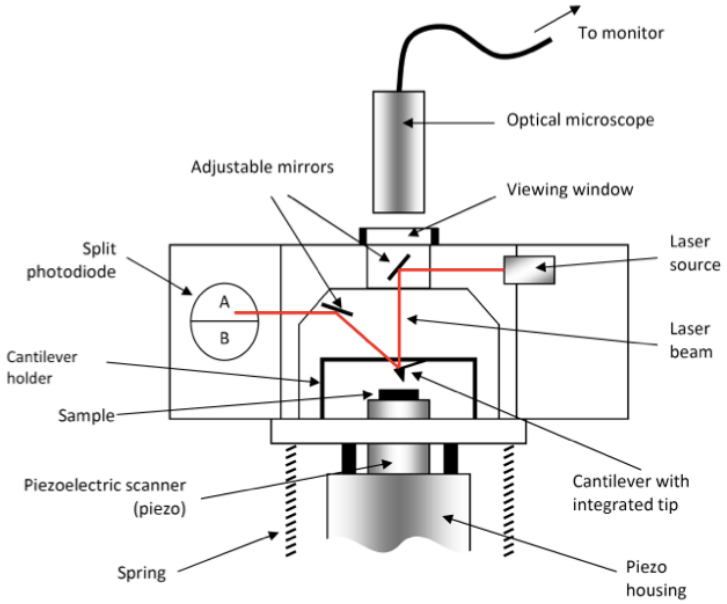

Figure 2.11. Schematic representation of atomic force microscope in operation. Surface topography is mapped through a feedback loop monitoring the oscillation of the cantilever across the surface as it undergoes chemical interactions. A piezoelectric scanner rasters across the x-y direction of the surface as the feedback loop controls the z-positioning relative to the sample[1]

Key to the operation of the atomic force microscope is the piezoelectrical scanner which allows for sample movement in the x,y and z directions. The piezoelectric scanner and accompanying machinery allows for the movement to be controlled by an applied potential with the magnitude of the potential controlling the degree of movement through the piezoelectric effect. The scanner and accompanying mechanical stage raster the position of the sample relative to the cantilever probe which acquires a 3D image of the surface. The cantilever probes in this research are between 100 µm-200µm and feature a silicon nitride Si_3N_4 pyramidal tip at the end of the probe. The probe is brought into contact of the surface and once the tip is engaged specialist feedback electronics control the position of the cantilever. The stiffness of the cantilever is a physical property that plays a role in the imaging of the surface. In order to image surfaces optimally with reduced noise a stiff spring with a high resonant frequency is required, optimising the maximum deflection whilst minimising noise. The four quadrant photodiode measures the position of the cantilever due to changes in the aligned reflected laser position, occurring due to interactions of the cantilever with the surface. Cantilevers used during this investigation featured spring constants in the range 0.06-0.6Nm^{-1}.

2.3.3.2 Imaging of Surfaces

Imaging of surfaces proceeded utilising a tapping mode of operation. In tapping mode the cantilever tip is brought into contact with the surface and tapped at or near the cantilevers resonant frequency across the substrate. As the cantilever moves across the surface it experiences interaction forces that result in variation in the amplitude of oscillation of the cantilever (typically a reduction in amplitude). A piezo electric actuator controls the height of the cantilever through a feedback loop resulting in constant amplitude as the tip is scanned across the surface. The resulting tapping mode image is the resulting changes in height caused by these forces at the surface as measured by the feedback loop.

Post-imaging a series of quantitative measurements can be undertaken utilising Nanoscope Analysis v 1.4 software suite functions. The roughness of imaged surface can be measured utilising root mean square (RMS) calculations in x, y using a plane fitting model on the image.

2.3.4 Peak Force Tapping and Conductive AFM Instrumentation

Conductive AFM allows the measurement of current-voltage traces at a point and conductive mapping across a sample surface during regular topographical imaging. Conductive AFM is an emerging technique in organic electronics and has been used in the electrical characterisation of organic photovoltaic blends,[13-15] polymeric films for thin film transistor application [12] and single crystal organic nanowires.[16] Conductive AFM images were captured using a peak force tapping PF-TUNA module attached to the Multimode Nanoscope V using a platinum iridium tip with a tip radius of 35nm. Peak force tapping is a proprietary scanning mode to Bruker Corporation and in combination with the PF-TUNA module allows for conductive imaging of studied surfaces through the measurement and regulation of tunnelling currents on the order of picoamps. Figure 2.12 describes the force-

distance curve experienced by a probe during an approach to the surface utilising a peak force tapping methodology.

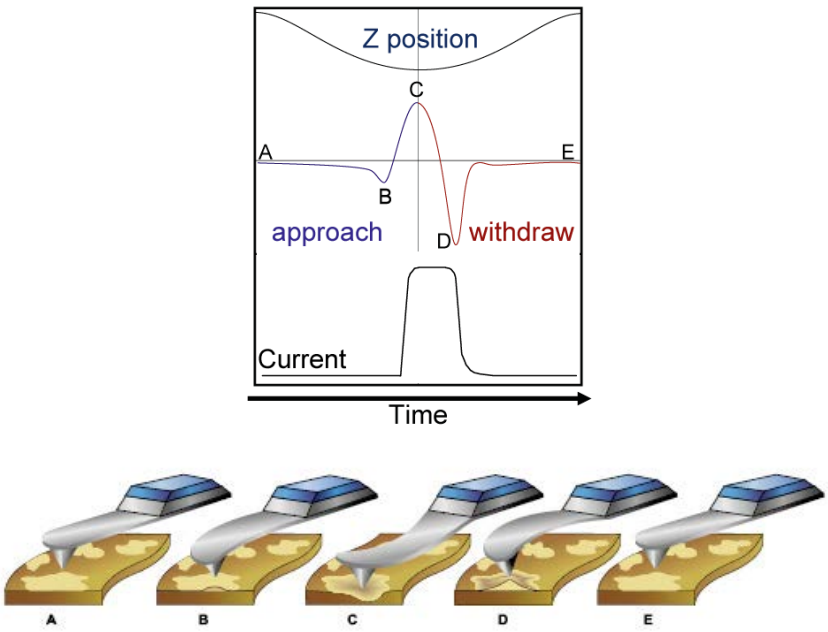

Figure 2.12 A. Force-distance forces experienced by a tapping mode probe during an approach and withdraw cycle. B. Schematic representation of probe position relative to sample surface.[1]

During peak force tapping the probe periodically taps the surface with the interaction force monitored within the Nanoscope V feedback electronics. The methodology allows for forces on the scale of a piconewton to be measured and used as the peak force output. The feedback loop keeps the peak force constant as it scans across the surface measuring the z-position of the probe and translating it into a topographical image. Traditional tapping mode forces are on the order of nanonewton and provide increased lateral forces damaging the surface. The low interaction force of the peak force methodology allows for reduced surface damage and the ability to scan sensitive surfaces. The increased control and reduction in lateral forces provides the feasibility to generate conductive maps without deformation or destruction of the surface. In this study the technology has been used to probe the electrical properties of the device operational area and the semiconductor- aluminium interface. The generation of conductive AFM maps takes place in peak force tapping modal. Utilising a platinum coated cantilever with a

probe diameter of 35nm an operating bias is applied between the sample and the cantilever and the tunnelling current measured along with topographical information. A unique sample mounting stage allows for electrical contact to be made with the substrate being examined. A schematic of the sample stage with a sample mounted and the operating biases is shown in Figure 2.13A.

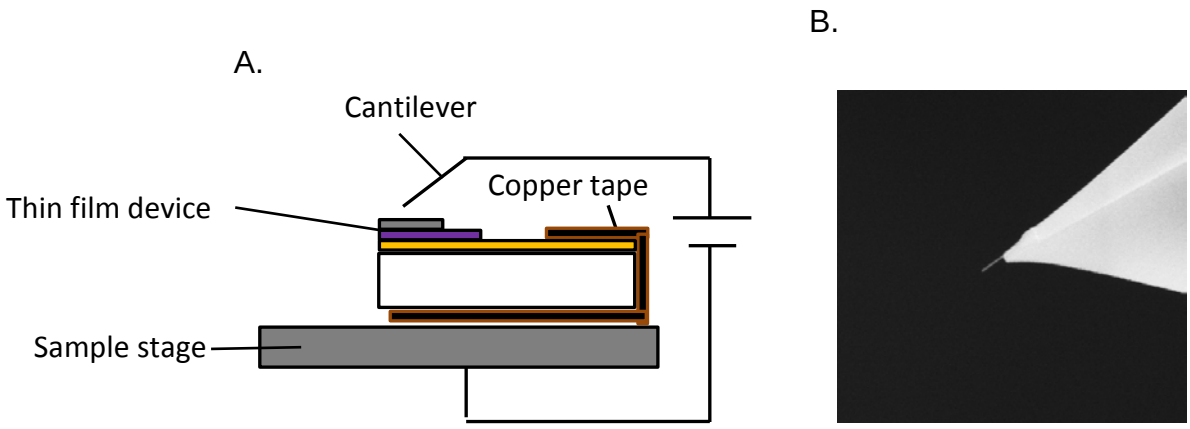

Figure 2.13. Experimental schematic for conductive AFM. A. PF-TUNA sample stage with applied biases during conductive mapping. A double sided copper tape is used to make electrical contact with the sample. A completed device is mounted with the copper tape providing a contact with a terminal in the thin film device. B. High resolution PtIR cantilever tipped with a carbon nanotube attached from the functional end of the probe as developed by Stapleton *et al*.

Individual devices are mechanically cut from processed devices and characterised in a low humidity room. An internally developed methodology developed by Stapleton *et al.*[17] in which conductive platinum iridium (PtIr) cantilevers had carbon nanotubes attached was shown to provide a 10x increase in the resolving power of conductive microscopy images and can be seen in Figure 2.13B.[18] The high resolution cantilever was used on semiconducting films in this project in order to gain information on the ordered domains of polythiophenes used in this study.

2.3.5 Optical Microscope

A Nikon D5000 optical microscope is used to provide optical insight on surface features on thin films and devices. Captured optical images are captured through a

digital 5megapixel camera attached to the optical train allowing for the capture of sample photographs.

2.4 I-V Characterisation

Electrical characterisation for fabricated devices was performed using a Keithley 2400 source meter unit (SMU) connected via serial port connection to a desktop computer. Current-voltage characteristics were measured by applying a bias potential and measuring the current response at an applied potential using the SMU in conjunction with a LabVIEW virtual instruments (VI) which allowed for the acquisition of data and programming of custom voltage sweeps. During the testing of three terminal device a second potential was applied using a Dick Smith Power Supply capable of outputting 30V. A testing schematic can be seen in Figure 2.14.

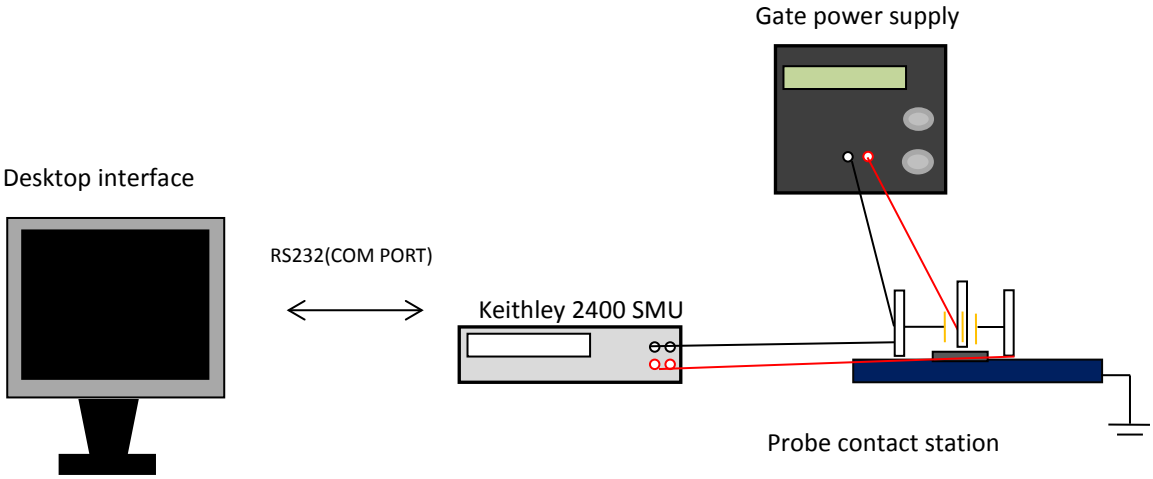

Figure 2.14 Electrical characterisation schematic. Current-voltage measurements are obtained via integration of a source-meter unit with a PC loaded GUI via an RS232 com port. A Floating source potential is applied through the source-meter unit and a secondary power supply unit can supply a floating gate potential. Electrical characterisation through this apparatus is capable of 10uA measurement accuracy of 0.1nA. Range of 2V measurement accuracy of 10uV with a voltage ramp $0.65V.s^{-1}$

A LabVIEW VI was designed to acquire measured data and program voltage sweeps. The interface was capable of programming voltage in up to 28 discrete steps with a Number of Power Line Cycles (NPLC) of 10. The NPLC is an integration time with values spanning 0.001 to 10, an NPLC of 10 using 28 data points, over a ±4V range will lead to a voltage ramp of $0.65V.s^{-1}$ for our devices- it is the slowest ramp

available. The voltage will ramp from the designated start voltage to the finish voltage the resistance/current at each point. This rate is comparable to Literature ramps- 0.050V/s,[19] and 0.1V/s[20] was selected as the ramp speed for all polymeric devices. During September 2012 an alternative testing apparatus, operating with a Keithley 2600 dual channel SMU in combination with LabVIEW VI was used for specialist experiments featuring planar device structures. The dual channel SMU was capable of increased source biases in comparison to the power supply allowing gate biases up to 80V to be applied. NPLC and voltage ramp parameters were kept consistent between the apparatus and acquisition occurred via serial port connection.

2.4.1 Probe Contact Station

An electrical testing probe contact station is commonly used to make reproducible electrical contact with fabricated devices allowing the application of electrical potential across a device. Industrial probe stations feature a testing stage with three contact probes positioned peripherally allowing for contact to be made with device electrodes. Controlling the applied pressure,[21] environmental shielding,[22] tested device accessibility,[23] and probe positioning through precision optics [24] are areas of interest in contact station development. High resolution micro positioners allow for precise *x,y,z* positioning arrangements through either manual or automatic positioning of each contact probe relative to the sample being tested. The high precision allows for reproducible contact sequentially across all devices on a fabricated substrate minimising any lateral friction damage to the electrode surface from the contact probe during experimentation encouraging reliable device performance. Full featured probe stations can be used in a nitrogen atmosphere glove box, preventing atmospheric effects and allowing precise adjustment of contacts through a microscopic positioning arrangement improving contact positioning with respect to the studied substrate. A probe contact station capable of reproducible contact that reduced lateral damage was developed at Flinders that would allow reproducible contact with devices using a manual positioning arrangement. A probe contact station schematic can be seen in Figure 2.15.

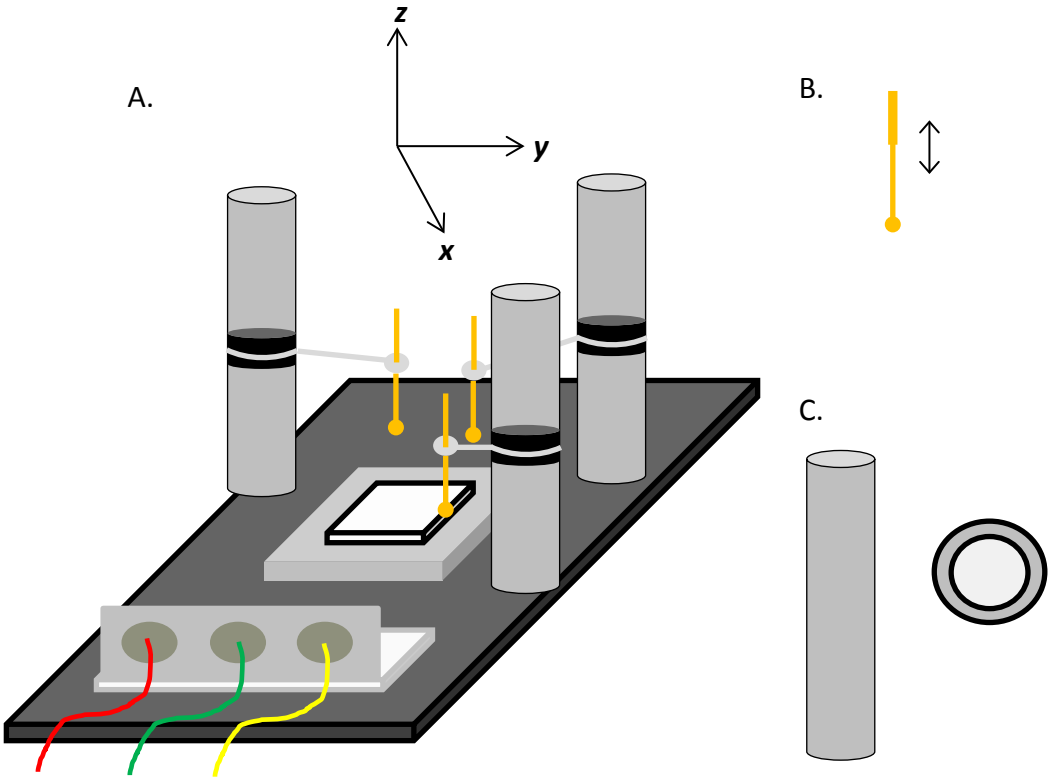

Figure 2.15. Electrical probe station. A. Probe station schematic B. Gold probe contact C. Manual positioning tower schematic featuring a magnetic base.

The design challenge for a probe contact station is making reproducible contact with device electrodes whilst avoiding damage to the electrode surface. To accomplish this stainless steel was used to make a testing stage with the substrate being loaded into a screw tightened substrate holder in the centre of the testing stage to reduce lateral movement of the sample being tested (Figure 2.15A). Probe positioners were developed featuring a magnetic bottom which allowed manual x-y positioning across the testing surface with the magnets attracting to the testing stage and locking the position of the probe with respect to the testing stage (Figure 2.15B). Two part spring loaded contact probes with a spherical head manufactured by Harwin (Part # P25-0423) were used to make contact with device electrodes and feature a spherical contact to reduce electrode damage (Figure 2.15B). The motherboard pin features a two part assembly allowing pressure depreciation minimising pressure on the electrode surface.

2.4.2 Nitrogen Environment Testing Chamber

In order to allow the testing of devices in an inert atmosphere an environmentally isolated testing chamber was designed. A graphical schematic of the inert testing chamber connected to a nitrogen source (BOC gases, >99.99% purity) can be seen below in Figure 2.16. The testing chamber allowed for the transfer of fabricated device samples directly from the nitrogen glove box to the testing chamber from within the glove box. The mobile chamber could be transferred into the glove box through a peripheral antechamber with samples transferred through to nitrogen testing chamber through the introduction hatch *in situ*. During this procedure the nitrogen testing chamber would be backfilled with pure nitrogen from the glove box, samples transferred with the introduction hatch sealing the environment through metal screws. A rubber seal placed between the introduction hatch and the chamber helped ensure an environmental seal. Glove mounts, designed to allow a pair of modified rubber gloves into the chamber provided a tight seal with O-rings being used in the glove mounts to provide similar protection from external atmosphere. Within the box a contact probe contact station was integrated. An electrical panel, fitted into the wall of the chamber facilitated electrical contact between an external SMU and the probe contact station through banana plugs.

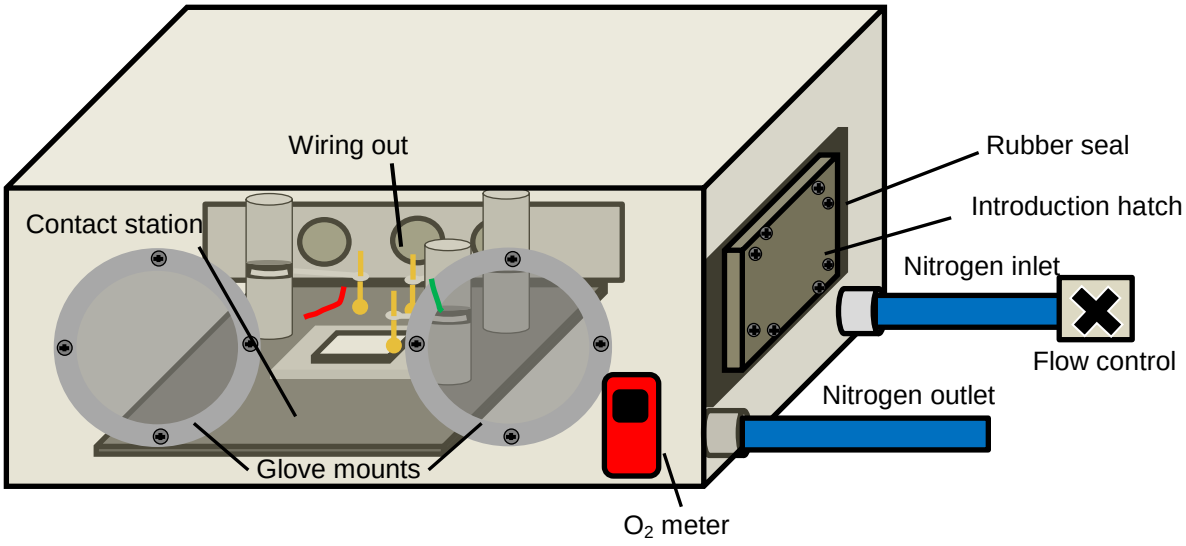

Figure 2.16. Schematic of inert testing chamber during testing procedure. The chamber allowed for testing in an inert atmosphere. An O_2 meter allowed for the monitoring of oxygen levels in the environment.

In order to maintain the integrity of the chamber a positive nitrogen pressure was employed to reduce the likelihood of atmospheric contamination. A gas inlet allowed bottled nitrogen to flow into the chamber with a flow gauge on the gas line controlling the rate of nitrogen flowing into the glove box. An outlet valve was used allowing chamber atmosphere to flow into the surrounding environment. The position of the rubber gloves during gas flow allowed for a qualitative assessment of the pressure within the box with filled pressurised gloves suggesting a positive pressure. A Scott Protègè ZM O_2 meter (Part # 096-3459-03) was positioned in the chamber and produced a digital read out showing under these conditions consistent chamber oxygen content of 0.01% was achievable. The testing chamber was utilised for the study and characterisation of electrical devices under an inert nitrogen atmosphere.

2.5 Computer Numeric Controlled Cutting

Vertical wall architectures were introduced to device substrates through means of a computer numeric controlled (CNC) mechanical cut path. An LPK40 CNC seen in Figure 2.17 was used. The cutter utilised tungsten carbide drill bits and operates at 50,000rpm. An aligning polycarbonate sheet with substrate cut out was employed to ensure accurate positioning of substrate with respect to the milling path and to reduce lateral movements to ensure the best finish possible seen in Figure 2.17B. The alignment sheet is fitted in position by two alignment stubs which allow the board to be fitted reliably and repeatedly with minimal error in repeated placement. A cut path was programmed with a controllable width which can be used to control the removed electrode area allowing for area studies to be performed. Furthermore, the sheet served to planarise the plane of cut in the *z*-axis to reduce any necessary lateral disturbances across the path of the spindle to ensure consistent depth and cut and can be seen in Figure 2.17B and C.

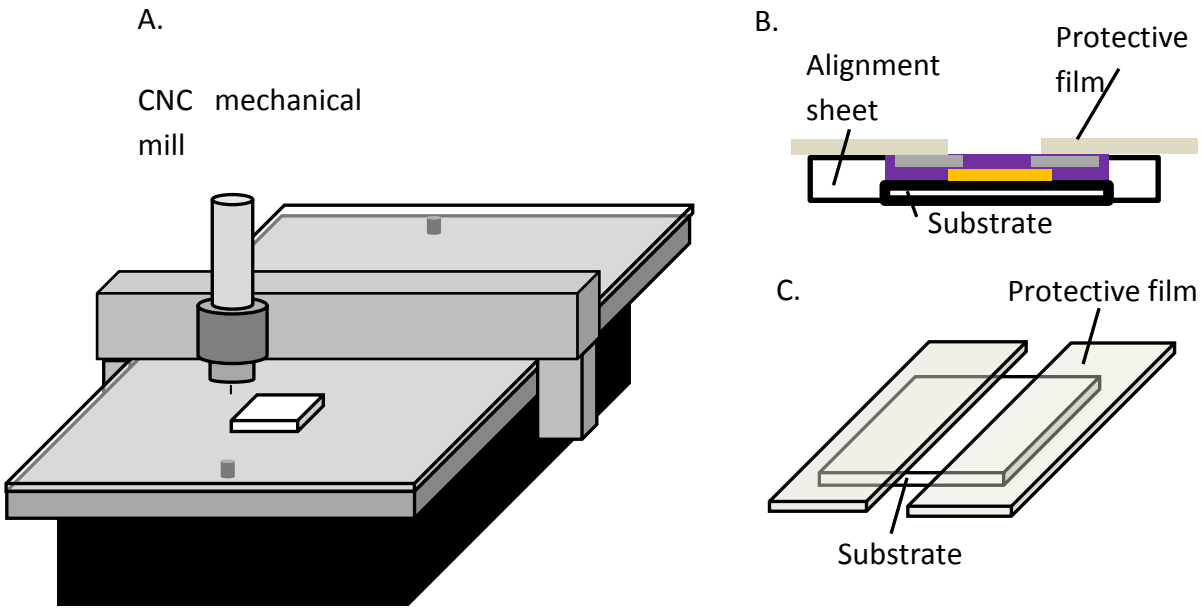

Figure 2.17. Mechanical cutter- LPK 40 A4 circuit board cutter schematic. A. Experimental schematic of the cutting procedure. B. Cross section schematic of the substrate position in the alignment sheet. C. Protective sheet cover protecting the top surface of the device surface with the cut path exposed for cutting.

References

1. Li, C., et al., *Application Note 132 Simultaneous Electrical and Mechanical Property Mapping at the Nanoscale with PeakForce TUNA.* 2011.
2. Emslie, A.G., F.T. Bonner, and L.G. Peck, *Flow of a Viscous Liquid on a Rotating Disk.* Journal of Applied Physics, 1958. **29**(5): p. 858-862.
3. Winzenberg, K.N., et al., *Dibenzo[b,def]chrysene Derivatives: Solution-Processable Small Molecules that Deliver High Power-Conversion Efficiencies in Bulk Heterojunction Solar Cells.* Chemistry of Materials, 2009. **21**(24): p. 5701-5703.
4. Singh, T.B., et al., *Fabrication and characterization of solution-processed methanofullerene-based organic field-effect transistors.* Journal of Applied Physics, 2005. **97**(8).
5. Treadway, G., alchmst@vbbn.com, 2013. coating. [E-mail] Message to DG Gruszecki (alchmst@vbbn.com). Sent 14 April 13. Available at: 14 April 13 [Accessed 15 April 13].
6. Cheng, X., et al., *Air Stable Cross-Linked Cytop Ultrathin Gate Dielectric for High Yield Low-Voltage Top-Gate Organic Field-Effect Transistors.* Chemistry of Materials, 2010. **22**(4): p. 1559-1566.
7. Carrad, D.J., et al., *Electron-Beam Patterning of Polymer Electrolyte Films To Make Multiple Nanoscale Gates for Nanowire Transistors.* Nano Letters, 2013. **14**(1): p. 94-100.
8. Kim, S.H., et al., *Electrolyte-Gated Transistors for Organic and Printed Electronics.* Advanced Materials, 2013. **25**(13): p. 1822-1846.
9. *Scanning Beam Methods*, in *Electron Microscopy*. 2007, Wiley-VCH Verlag GmbH. p. 305-497.
10. Binnig, G., C.F. Quate, and C. Gerber, *Atomic Force Microscope.* Physical Review Letters, 1986. **56**(9): p. 930-933.
11. Douhéret, O., et al., *Nanoscale electrical characterization of organic photovoltaic blends by conductive atomic force microscopy.* Applied Physics Letters, 2006. **89**(3): p. -.
12. Reid, O.G., K. Munechika, and D.S. Ginger, *Space Charge Limited Current Measurements on Conjugated Polymer Films using Conductive Atomic Force Microscopy.* Nano Letters, 2008. **8**(6): p. 1602-1609.
13. Kamkar, D.A., et al., *Single Nanowire OPV Properties of a Fullerene-Capped P3HT Dyad Investigated Using Conductive and Photoconductive AFM.* ACS Nano, 2012. **6**(2): p. 1149-1157.
14. Dante, M., J. Peet, and T.-Q. Nguyen, *Nanoscale Charge Transport and Internal Structure of Bulk Heterojunction Conjugated Polymer/Fullerene Solar Cells by Scanning Probe Microscopy.* The Journal of Physical Chemistry C, 2008. **112**(18): p. 7241-7249.
15. Ionescu-Zanetti, C., et al., *Semiconductive Polymer Blends: Correlating Structure with Transport Properties at the Nanoscale.* Advanced Materials, 2004. **16**(5): p. 385-389.
16. Chung, J.W., et al., *Single-crystalline organic nanowires with large mobility and strong fluorescence emission: a conductive-AFM and space-charge-*

limited-current study. Journal of Materials Chemistry, 2009. **19**(33): p. 5920-5925.
17. Stapleton, A.J., et al., *Pathway to high throughput, low cost indium-free transparent electrodes.* Journal of Materials Chemistry A, 2015. **3**(26): p. 13892-13899.
18. Ashley, D.S., et al., *Carbon nanotube modified probes for stable and high sensitivity conductive atomic force microscopy.* Nanotechnology, 2016. **27**(47): p. 475708.
19. Takshi, A. and J.D. Madden, *Large apparent inductance in organic Schottky diodes at low frequency.* Journal of Applied Physics, 2006. **99**(8): p. 084503.
20. Chen, Q., et al., *Opto-electronic characterization of electron traps upon forming polymer oxide memory diodes.* Applied Physics Letters, 2011. **99**(8): p. 083305.
21. Rath, D.R., *Pressure control apparatus for use in an integrated circuit testing station*, 1988, Google Patents.
22. Yassine, A.M., *Wafer shielding chamber for probe station*, 1998, Google Patents.
23. Tarter, T.S. and N.T. Do, *Method and apparatus for electrical characterization of an integrated circuit package using a vertical probe station*, 2002, Google Patents.
24. Snyder, D.E., C.T. Veenendaal, and T.G. Creedon, *Integrated circuit probe station*, 1990, Google Patents.

Chapter 3

3. Understanding Planar Organic Field Effect Transistors

Introduction

Solution processing is a scalable and cost effective technique by which to deposit active layer materials. In order to investigate the feasibility of solution processing and fabrication variables planar devices in bottom contact and top contact architectures are investigated using the small molecule Tri-isopropyl-silane - di-benzo chrysene (TIPS-DBC) organic semiconductor. Top contact devices will be made using the organic resin benzocyclobutene (BCB) dielectric. Bottom contact devices will be fabricated on silicon featuring thermally grown SiO_2. The morphology of the active layer in devices will be compared and understood with respect to device properties in order to develop an understanding of planar organic field effect transistors, their operation and limitations.

3.1 Planar OFET structures

Planar device architectures are defined by the position of their electrical contacts (gate, source and drain). The two structures fabricated are seen in Figure 3.1. Figure 3.1 A. shows a schematic of a top contact organic field effect transistor. Figure 3.2 B. shows the bottom contact organic field effect transistor architecture.

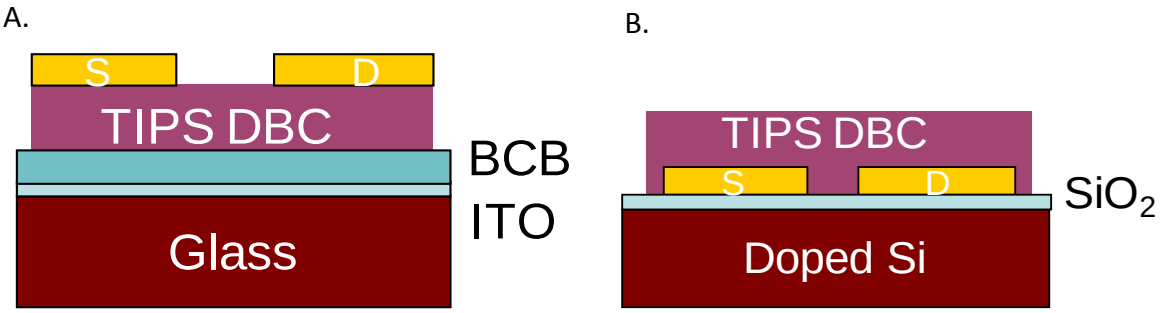

Figure 3.1. FET schematics for fabricated devices. A. top contact FET configuration and B. bottom contact FET configuration.

The channel length, *L*, of the devices was 20 μm and the channel width, *W*, was fixed at 10 mm. The substrate temperature during the evaporation of TIPS-DBC was controlled at room temperature, 50 °C and 75°C to compare nanomorphologies resulting from deposition conditions.[1] This study will compare the material performance between solution processed and evaporated devices whilst understanding the limitations of planar devices

3.1.1 Device Operation

Fabricated devices were electrically characterised with their output and transfer characteristics measured. Figure 3.2 shows a representative transfer characteristic and output characteristic for a spin coated top contact OFET.

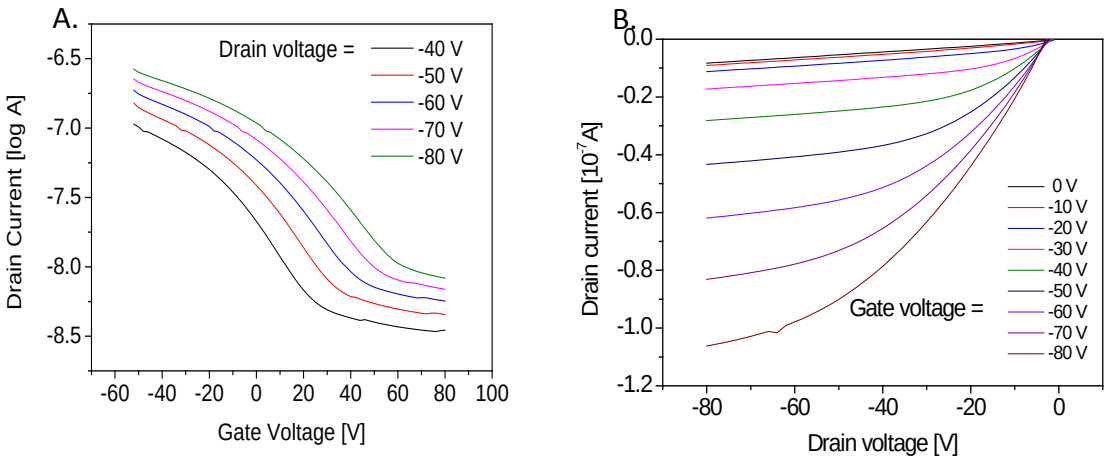

Figure 3.2. I-V characteristics of spin cast TIPS-DBC devices. A. Transfer curve with gate voltage sweeping from -50 V to 50 V and B. output curve with gate voltage ramped to -80 V. Measurements were taken under room temperature in a nitrogen environment.

Figure 3.2 A. shows the transfer characteristic of the device with the drain voltage kept constant over the range -40V to -80V as the gate voltage was swept -60V to 80V. Figure 3.2 B. shows the characteristic output curve of the device. With the gate voltage kept constant at a set voltage over the range 0V to -80V and the drain voltage swept over the range 0V to -80V. Operation under negative applied V_{GS} and V_{DS} indicates a device operating as a p-type channel accumulation device. The output curve shows two operating regimes a linear regime ($V_{DS} < V_{GS} - V_T$) and a saturation regime at voltages $V_{DS} = V_{GS} - V_T$. An equivalent circuit for the planar OFET is proposed in Figure 3.3.

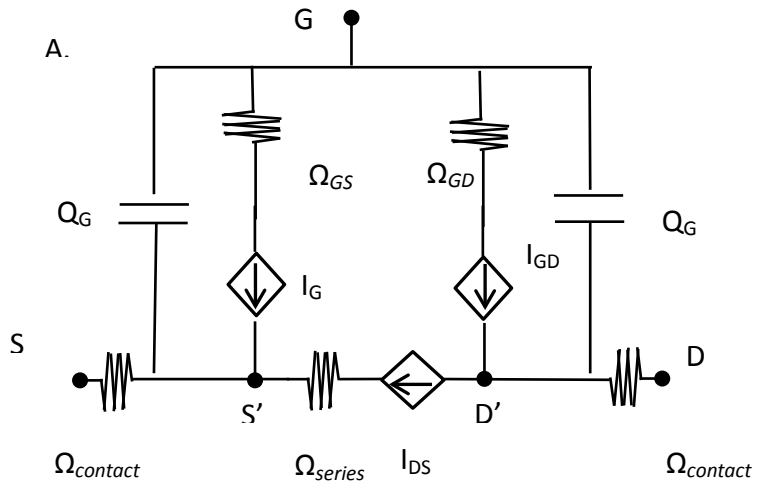

Figure 3.3. OFET equivalent circuit. A. Equivalent circuit describing the electrical performance of an OFET.

The equivalent circuit describes the operation of a planar OFET as a network of capacitive and resistive elements. Key to the operation of the organic field effect transistor is the semiconductor-dielectric interface, as V_{GS} is applied the lateral field incident is increased polarising the material and changing the current flux of the semiconductor. The gradual channel approximation applies when the lateral field is significantly greater than the electric field between source and drain. The potential drop along the length of the channel *x* is assumed to be linear forming a consistent enhancement across the device. Detrimental to the device performance is the contact resistance in the device which is dependent on the structure employed.[2]

3.2 Device Characteristics and Semiconductor Morphology

3.2.1 Top Contact Devices

Solution processed devices were prepared using a range of spin speeds, with the carrier mobility and threshold voltage device parameters calculated. An important parameter in describing the performance of an OFET is the field effect mobility, μ_{FE}, which is a measure of the field induced carrier transport through a film. The field effect mobility is influenced by the organisation of the molecules with respect to each other in the bulk, and at the channel-capacitor interface, which potentially introduces charge traps thereby reducing charge transport through the channel.[3,

4] The carrier mobility values presented in this work were averaged from measurements over a minimum of four devices on the same substrate, with an variation of ±15%. From the respective slopes $\delta\sqrt{I_D}/\delta V_G$ is determined and along with the device parameters *L*, *W*, capacitance per unit area, C_i of 10 nF/cm^2, the saturated field effect mobility; $\mu_{e,h}$, was calculated using:

$$\mu_{e,h} = \frac{2L}{WC_i}\left(\frac{\partial\sqrt{I_{DS}}}{\partial V_{GS}}\right)^2 \qquad \text{Equation 3.1}$$

The maximum current and switching of a device can be extracted from I-V characteristics using the equation:

$$I_D = \frac{W}{L}C_{OX}\mu_{SAT}[(V_{GS}\text{-}V_T)^2 \qquad \text{Equation 3.2}$$

Where V_t is the threshold voltage (the V_{GS} point at which the free carrier density equals the trap density). The threshold voltage is extracted from the x-intercept of the $\sqrt{I_d}$ vs. V_{gs} plot for devices fabricated from different spin speeds and can be seen in Figure 3.4.

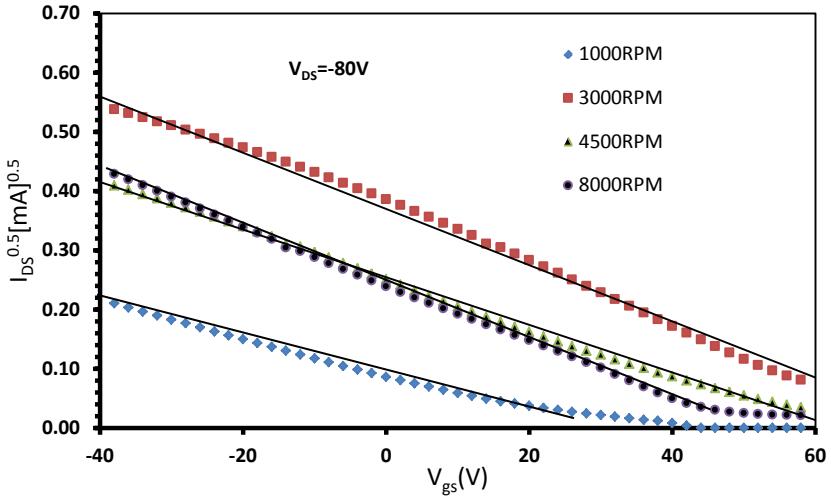

Figure 3.4- $\sqrt{I_d}$ vs. V_{gs} curve of solution processed TIPS-DBC OFETs prepared using different spin rates. Data is theoretically fit using equation (1).

The extracted device parameters for solution processed devices fabricated with spin speeds 1000RPM- 8000RPM is displayed in Table 3.1. The root mean square roughness (RMS) was extracted from atomic force microscope images of the operating area with the obtained atomic force microscope images shown in Figure 3.5.

Table 3.1.Root Mean Square Roughness and mobility of solution processed films.

Spin speed (RPM)	RMS (nm)	μ_{FE} ($cm^2V^{-1}s^{-1}$)	μ_{lin} ($cm^2V^{-1}s^{-1}$)	V_t (V)	On/ Off
1000	14.0	0.7×10^{-3}	1.4×10^{-4}	25	10^5
3000	6.5	1.0×10^{-3}	2.9×10^{-4}	70	10^3
4500	4.0	1.0×10^{-3}	2.5×10^{-4}	60	10^4
8000	4.5	1.5×10^{-3}	3.2×10^{-4}	45	10^4

Devices fabricated by solution processing show field effect mobility in the range 0.7 x 10^{-3} $cm^2V^{-1}s^{-1}$ – 1.5 x 10^{-3} $cm^2V^{-1}s^{-1}$. The best obtained ON/OFF ratio is seen to be 10^5 and occur in devices fabricated at 1000RPM. ON/OFF ratio for solution processed devices span the range 10^3- 10^5. The threshold voltages of the top contact devices can be seen to span the range 25V-70V with the lowest measured threshold voltage occurring for devices spun cast at 3000RPM.

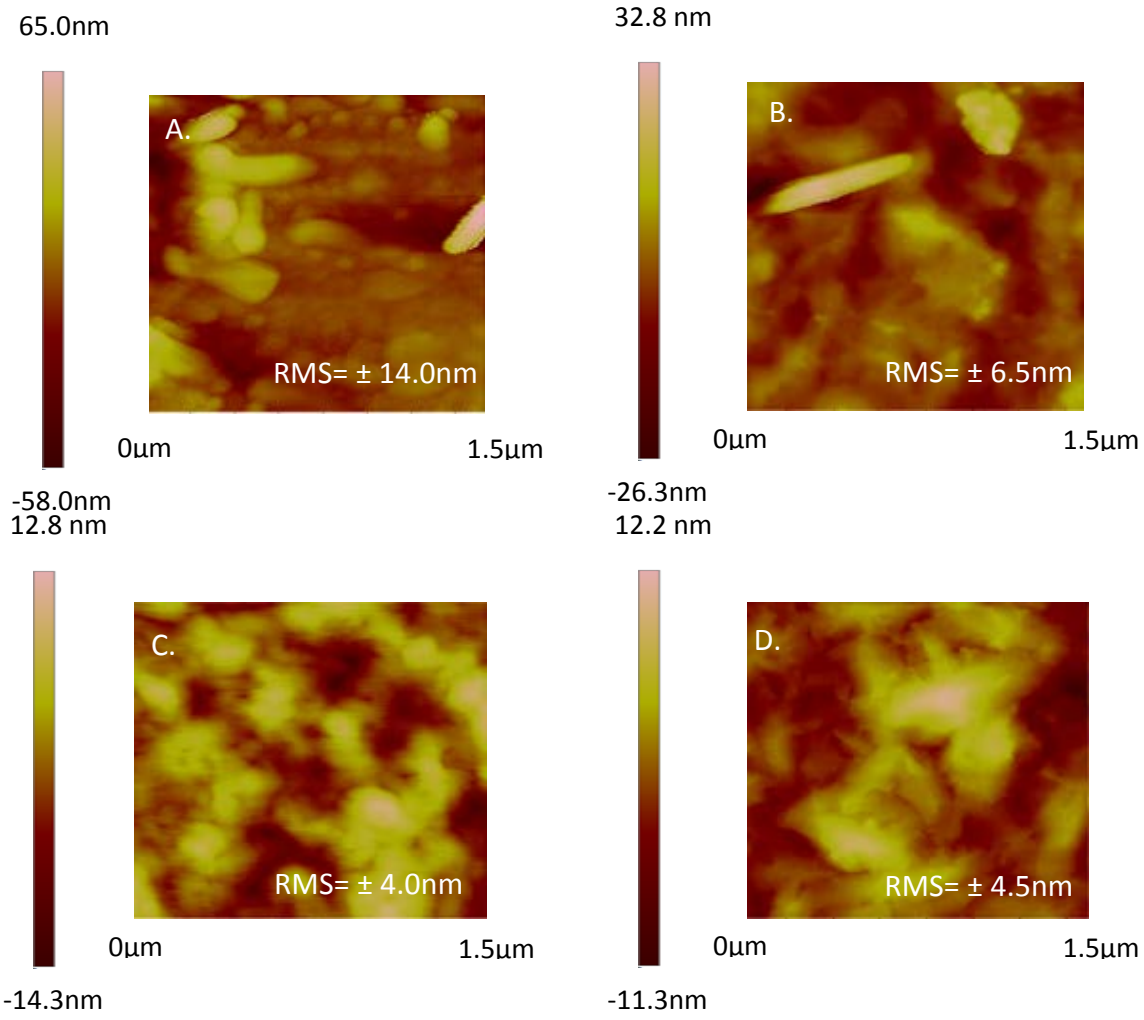

Figure 3.5. AFM images of solution processed films on top of BCB substrates .A. 1000RPM, B. 3000RPM, C. 4500RPM and D. 8000RPM.

Small molecules provide a much greater opportunity for crystallisation and packing than is possible in polymeric systems, due to enhanced reorientation and diffusion.[3, 4] Hence, the field effect mobility can be highly dependent on the nanomorphology which is a result of the processing conditions employed. TIPS-DBC films prepared by solution processing with spin speeds at 4500 and 8000RPM produce films with a nondescript surface as can be seen in the AFM in Figure 3.5C and Figure 3.5D with a root mean square (RMS) surface roughness of 4nm and 4.5nm respectively. At lower spin speeds, the RMS roughness increases to 6.5nm for 3000RPM and 14nm at 1000 RPM, as seen in Figure 3.5 B. and Table 1. Importantly, the film prepared by spin coating at 1000 RPM has a polycrystalline appearance as can be seen in Figure 3.5A.

Lower spin speeds lead to thicker films, and it can be speculated that due to slower solvent evaporation, there is a greater opportunity for the crystallisation of small molecules. It should be noted that the top surface is not the primary current path in bottom gate transistors, which implies that the top surface morphology is not of high importance. However, since the films are very thin compared to the dimensions of the surface features, the highly granular structure observed on the top surface, is expected to give an indication of the morphology at the gate dielectric interface region. The film morphology at this interface is well known to play an important role as charge transport takes place at this interface at applied high gate voltage.[5, 6]

The thin-film topography is seen to change under various processing conditions and correlated with the electrical properties of the corresponding FET. To better understand the role of crystalline order on mobility and device performance, ultrathin films of TIPS-DBC have been produced by drop casting dilute chloroform solutions on top of a pre-patterned Au electrode on a SiO_2 dielectric. This results in highly ordered films with approximately 2nm high terraces of what appears to be crystalline shown in Figure 3.6.

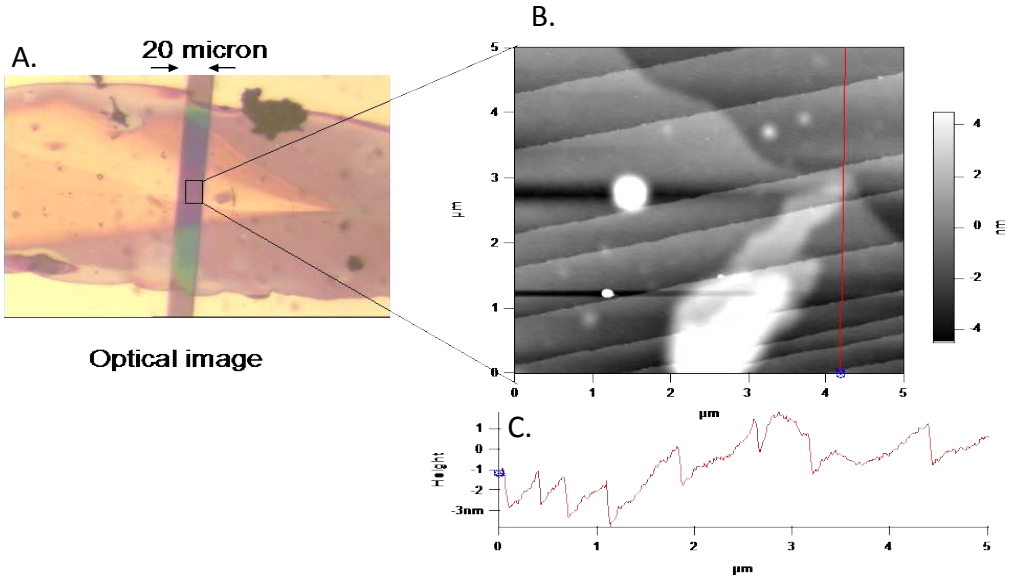

Figure 3.6. A. Optical image of thin film processed by drop casting producing large crystals on top of the source-drain Au electrodes. B. 5µm x 5µm AFM topography image. C. height profile across surface environment.

A key drawback to in the performance of top contact devices is the semiconductor-dielectric interface. Due to the architecture the roughness of the dielectric interface

can effectively increase the effective gate length of top contact devices, increasing the power consumption and reducing the switching frequency of fabricated devices. Furthermore, the formation of polycrystalline films can, result in multiple interfaces and can be a source of further charge traps. Charge traps produce an additional parasitic capacitance in the device equivalent circuit increasing the threshold voltage of fabricated devices. The promotion of favourable morphologies with low roughness at the channel-capacitor interface is critical to device success.[7] The use of benzocyclobutene (BCB) as a gate dielectric in bottom gate devices provides an interface with very low roughness and therefore effective gate length is reduced (BCB surface RMS= 2.5nm).[8]

Top contact devices also possess a parasitic resistance between the injecting electrode and the accumulation channel formed at the dielectric interface. Despite the structure producing lower contact resistances in general compared to bottom contact devices.[9] The parasitic resistance has been reported in the few monolayers at the dielectric-semiconductor interface and has been shown to influence the field effect mobility and overall device performance depending on the thickness of the organic semiconductor.[10-13]The parasitic resistance is described by the $\Omega_{contact}$ and is symmetric for the source and drain electrodes. This parasitic resistance arises from the increased distance from the charge injecting electrode to the accumulation channel found in the top contact geometry. The effect of this resistance increases as the gate length is scaled and the channel resistance decreases acting as an additional contact resistance in the equivalent circuit. Ultimately increasing the operating voltages required to operate the device.

3.2.2 Bottom Contact Evaporated TIPS-DBC devices

In contrast to solution processed top contact OFETs, bottom contact devices were fabricated on silicon featuring a thermally grown silicon dioxide dielectric. TIPS-DBC films were evaporated at different temperatures and electrically characterised. Figure 3.7A shows a representative transfer characteristic plot. Figure 3.7B shows a representative output characteristic plot.

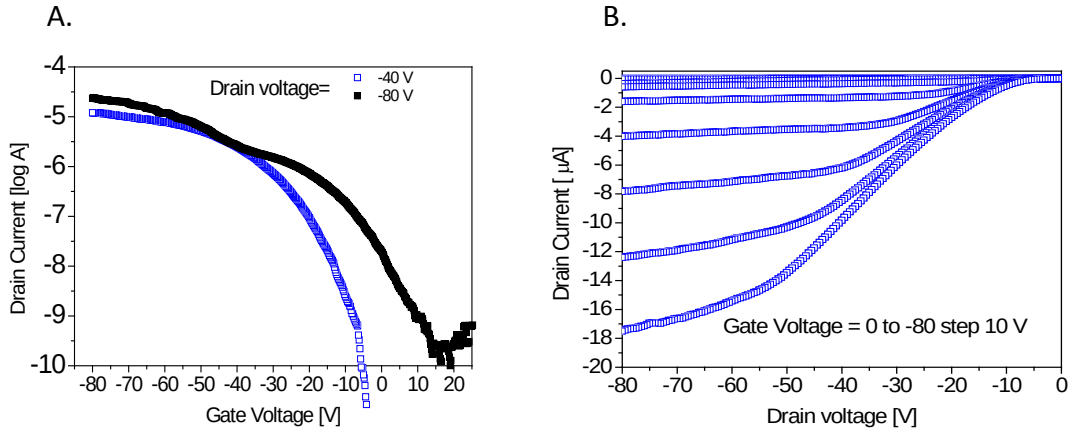

Figure 3.7. I-V characteristics of an TIPS-DBC device evaporated at 50°C. A. Transfer curve with gate voltage sweeping from -80 V to 25V. B. Output curve with gate voltage ramped to -80 V. Measurements were taken under room temperature in a nitrogen environment.

Table 3.2- Root Mean Square Roughness and mobility of evaporated TIPS-DBC films

Process	RMS (nm)	μ_{FE} ($cm^2V^{-1}s^{-1}$)	μ_{lin} ($cm^2V^{-1}s^{-1}$)	V_t (V)	On/ Off
SiO_2 @ 25 °C	3.7	$1.5x10^{-6}$	$0.6x10^{-6}$	5	10^3
SiO_2 :PFBT/HMDS @ 25 °C	2.85	$8x10^{-6}$	$1.2x10^{-6}$	2.5	10^4
SiO_2 :PFBT/HMDS @ 50 °C	4.6	$2.4x10^{-4}$	$7.5x10^{-5}$	19	10^5
SiO_2 :PFBT/HMDS @ 75 °C	7.3	$8x10^{-5}$	$2.2x10^{-5}$	6	10^6

Devices fabricated by evaporation of TIPS-DBC in bottom contact configurations show field effect mobility in the range 1.5 x 10^{-6} $cm^2V^{-1}s^{-1}$ – 2.4 x 10^{-4} $cm^2V^{-1}s^{-1}$. The

best obtained ON/OFF ratio is seen to be 10^6 and occur in devices evaporated at 75°C. ON/OFF ratio for evaporated devices span the range 10^3- 10^6. The threshold voltages of the top contact devices can be seen to span the range 2.5V-19V with the lowest measured threshold voltage occurring for devices evaporated at 25°C.

For the evaporated films, the highest mobility is found for the 50°C deposition protocol as summarised in Table 2, corresponding to the lowest roughness. Importantly the highest mobility for solution processing also correlated to the lowest roughness, but solution processing resulted in a higher mobility in all cases. While a higher threshold voltage in transistors using BCB as the gate dielectric can be expected due to the lower dielectric constant of BCB compared with SiO_2, the increase in threshold voltage observed as the spin speed was increased is interesting. One explanation could be related to the increasing grain boundaries in the conduction channel due to the polycrystalline structure of the TIPS DBC. This would require a larger threshold voltage to accumulate charge or compensate for the increased defects in the crystal structure. This effect would increase as the crystallite size decreases and the density of grain boundaries increases.

AFM images of evaporated TIPS-DBC thin-films on SiO_2 shown in Figure 3.8 display a granulated, structured and ordered topography with a roughness of approx. 5 nm. The topography is quite different to the 4500/8000RPM spin coated films despite a similar roughness.

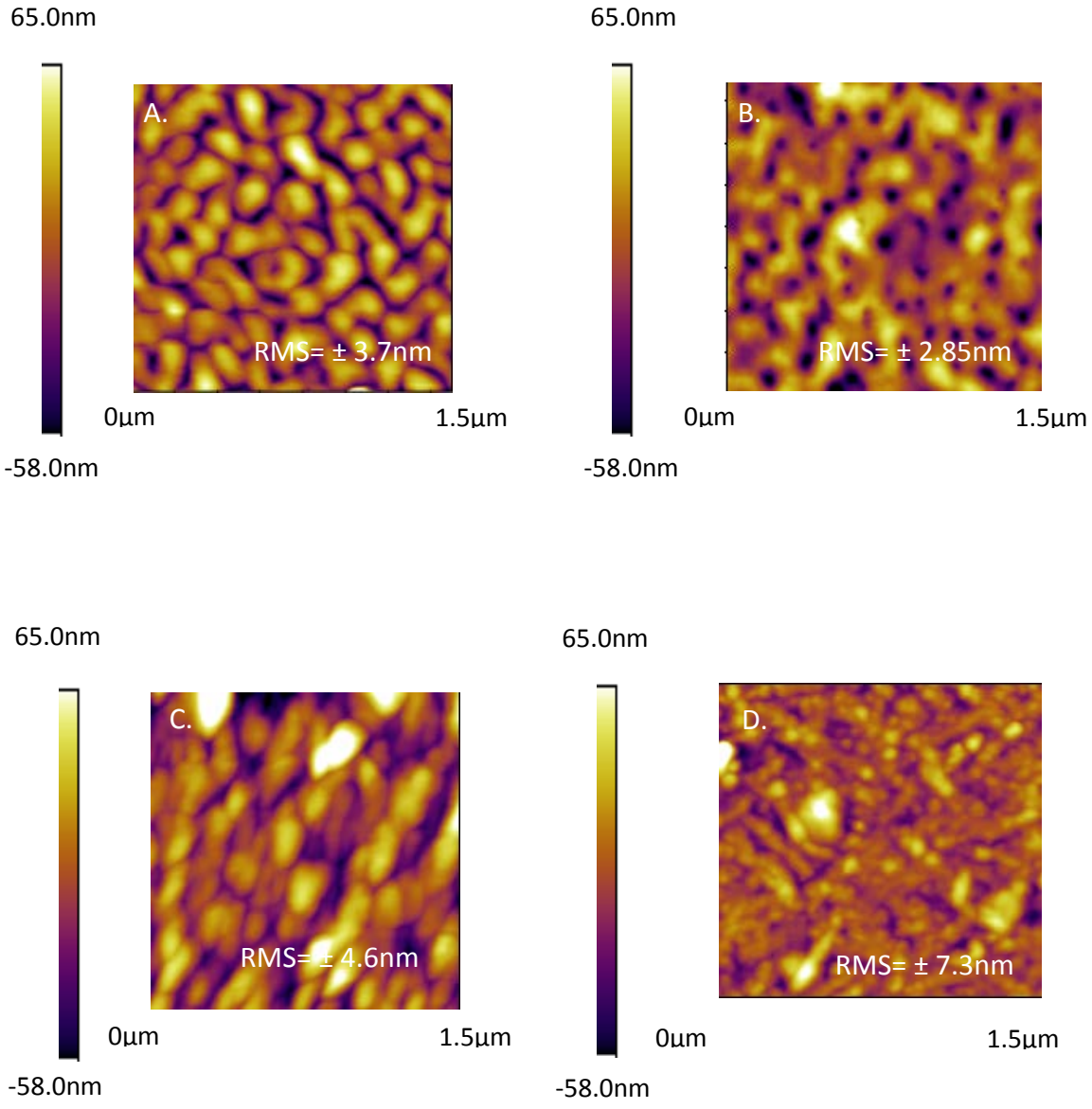

Figure 3.7. AFM images of evaporated thin films of TIPS-DBC under various processing conditions. A. 25 °C anneal temperature. B. 25°C anneal temperature with a PFBT/HDMS primer treatment. C. 50°C anneal temperature with a PFBT/HDMS primer treatment. D.75°C anneal temperature with PFBT/HDMS primer treatment.

Evaporated TIPS-DBC films exhibit a highly ordered topography at low temperatures with increased randomness as deposition temperature is increased (Figure 3.7 B. to D.). The surface roughness for these films is shown in Table 2. The topography at 50 °C shows a decreased order and grainy surface features when compared with films

fabricated at 25 °C (Figure 3.7C versus Figure3.7A). The topography at 75 °C shows fractures and localised regions of roughness and possible polycrystallinity (Figure 3.7D). Device characteristics for evaporated films are summarised in Table 2. Importantly, although films prepared by evaporation all had lower roughness than their solution processed counterparts, the hole mobility was substantially lower in all cases. The highest mobility in solution processed films was 1.5 $x10^{-3}$ $cm^2V^{-1}s^{-1}$compared to the range of mobility from $1.5x10^{-6}$ to $2.4x10^{-4}$ $cm^2V^{-1}s^{-1}$ in evaporated films. These results show that solution processing can offer performance advantages over evaporation, as well as added ease of deposition and lower cost. The strong dependence of the mobility on the morphology developed through different processing condition provides an opportunity to optimise device performance.

Despite the improved performance of the TIPS-DBC small molecule in the top contact configuration under solution processing, the majority of high mobility devices in literature are fabricated utilising bottom contact architectures.[14-18]A key drawback to the bottom contact architecture is due to the morphology of the semiconducting material formed during the deposition onto the patterned electrode surface. Near the electrode-semiconductor interface bottom contact architectures feature increased disorder at the electrode edge producing devices increasing the contact resistance and reducing performance.[12, 13]

Furthermore, key to improving the commercial feasibility of these structures is reducing the operating voltage of these devices. Reducing the power consumption of the technology can be improved in reducing the scaling of these devices, reducing gate length and in turn, reducing the effective gate length is a key aspect in realising complimentary circuits using organic field effect transistors. Devices fabricated using the above processes are limited in the resolution of the gate length. The lateral resolution limitations of the applied patterning technology are a key factor in scaling of the gate length to sub-micron resolutions and reducing operating voltages. The two architectures featured are examples of photolithographic processes with reduced scope for scale up. Commercialisation of

short channel organic devices requires a technology capable of effective and cost efficient scale up.

3.3 Conclusion

Planar organic field effect transistors were fabricated featuring top contact and bottom contact planar architectures. Devices were fabricated featuring the organic small molecule TIPS-DBC. Fabricated devices showed p-type accumulation mode operation with device properties dependent on the architecture and processing of the active layer. The TIPS-DBC top contact devices where seen to have field effect mobility in the range 0.7 x 10^{-3} $cm^2V^{-1}s^{-1}$ – 1.5 x 10^{-3} $cm^2V^{-1}s^{-1}$ with an ON/OFF ratio of 10^5 achievable. The threshold voltage in top contact devices was seen to span the range 25V-70V with operating voltages of up to 80V. Spun cast films of the TIPS-DBC small molecule showed varied morphology which was seen to affect the device performance with a polycrystalline appearance observed in the 1000RPM spin coat films. The polycrystalline nature of the film could result in charge traps at the dielectric interface effectively increasing the effective gate length and leading to larger than expected threshold voltages. Top contact devices showed field effect mobility in the range 1.5 x 10^{-6} $cm^2V^{-1}s^{-1}$ – 2.4 x 10^{-4} $cm^2V^{-1}s^{-1}$ with an ON/OFF ratio of 10^6 achieved. The improved mobility of TIPS-DBC devices under solution processing shows that solution processed devices are a viable technology to promote high performance transistor devices utilising the cheap associated cost with solution processing.

Both architectures feature limitations in effective scaling of the gate length resulting in high operating voltages of both architectures which could be reduced through effective scaling of the gate resulting in a lower power consuming device with improved switching performance. Top contact devices feature a parasitic access resistance from the source into the conducting channel, acting as additional contact resistance remains constant during the scaling of device dimensions. Bottom contact devices feature greater contact resistances due to increased disorder in the

active channel arising from deposition onto the patterned electrode surface specifically at the edge of the electrodes. The lateral resolution and cost of the photolithographic patterning suggests planar architectures will struggle to reach commercially viable short channel architecture. Providing motivation for the investigation of vertical architectures capable of short channel lengths to produce lower power consumption and faster switching devices to meet a market demand.

References

1. Gould, R.D., *Structure and electrical conduction properties of phthalocyanine thin films.* Coordination Chemistry Reviews, 1996. **156**(0): p. 237-274.
2. Meijer, E.J., et al., *Scaling behavior and parasitic series resistance in disordered organic field-effect transistors.* Applied Physics Letters, 2003. **82**(25): p. 4576-4578.
3. Tsao, H.N., et al., *The Influence of Morphology on High-Performance Polymer Field-Effect Transistors.* Advanced Materials, 2009. **21**(2): p. 209-212.
4. Chang, P.C., et al., *Film Morphology and Thin Film Transistor Performance of Solution-Processed Oligothiophenes.* Chemistry of Materials, 2004. **16**(23): p. 4783-4789.
5. Dinelli, F., et al., *Spatially Correlated Charge Transport in Organic Thin Film Transistors.* Physical Review Letters, 2004. **92**(11): p. 116802.
6. Singh, T.B., et al., *Monitoring the Channel Formation in Organic Field-Effect Transistors via Photoinduced Charge Transfer.* Advanced Functional Materials, 2009. **19**(5): p. 789-795.
7. Don Park, Y., et al., *Interface engineering in organic transistors.* Materials Today, 2007. **10**(3): p. 46-54.
8. Chua, L.-L., et al., *High-stability ultrathin spin-on benzocyclobutene gate dielectric for polymer field-effect transistors.* Applied Physics Letters, 2004. **84**(17): p. 3400-3402.
9. Pesavento, P.V., et al., *Gated four-probe measurements on pentacene thin-film transistors: Contact resistance as a function of gate voltage and temperature.* Journal of Applied Physics, 2004. **96**(12): p. 7312-7324.
10. Braga, D. and G. Horowitz, *High-Performance Organic Field-Effect Transistors.* Advanced Materials, 2009. **21**(14-15): p. 1473-1486.
11. Braga, D., et al., *Ultralow contact resistance in electrolyte-gated organic thin film transistors.* Applied Physics Letters, 2010. **97**(19): p. 193311.
12. Wang, S.D., Y. Yan, and K. Tsukagoshi, *Understanding contact behavior in organic thin film transistors.* Applied Physics Letters, 2010. **97**(6): p. 063307.
13. Natali, D., L. Fumagalli, and M. Sampietro, *Modeling of organic thin film transistors: Effect of contact resistances.* Journal of Applied Physics, 2007. **101**(1): p. 014501.
14. de Boer, R.W.I., T.M. Klapwijk, and A.F. Morpurgo, *Field-effect transistors on tetracene single crystals.* Applied Physics Letters, 2003. **83**(21): p. 4345-4347.
15. Sundar, V.C., et al., *Elastomeric Transistor Stamps: Reversible Probing of Charge Transport in Organic Crystals.* Science, 2004. **303**(5664): p. 1644-1646.
16. de Boer, R.W.I., et al., *Organic single-crystal field-effect transistors.* physica status solidi (a), 2004. **201**(6): p. 1302-1331.
17. Mas-Torrent, M., et al., *Single-crystal organic field-effect transistors based on dibenzo-tetrathiafulvalene.* Applied Physics Letters, 2005. **86**(1): p. 012110.
18. Mas-Torrent, M., et al., *Correlation between Crystal Structure and Mobility in Organic Field-Effect Transistors Based on Single Crystals of Tetrathiafulvalene Derivatives.* Journal of the American Chemical Society, 2004. **126**(27): p. 8546-8553.

Chapter 4

4. Optimised Two Terminal Devices on Polycarbonate for Vertical Transistor Applications

Introduction

Fabrication of two terminal devices on polycarbonate substrates allows for devices to be realised on low cost substrates. Plastic substrates also offer advantages in terms of opacity and mechanical properties allowing for non-traditional device architectures and processing technologies to be investigated. Optimising processing conditions for layered functional films on polycarbonate and the resulting devices is critical to reproducible device fabrication on polycarbonate. To this end, simulation of current-voltage behaviour provides an important tool in the analysis of experimental results and extraction of circuit parameters. Allowing equivalent circuits to be simulated and the performance fitted to current voltage traces providing a tool to describe changes in device performance. Understanding the changes and variation in the performance of a device and its equivalent circuit are critical to accurate future transistor characterisation and an optimised two terminal device.

4.1 Deposition of Polymeric Solutions on Polycarbonate

Early trials of depositing polymeric solutions onto polycarbonate substrates with gold electrodes were attempted and can be seen in Figure 4.1. Resulting thin films were observed to be non-uniform in thickness with visible defects and can be seen in in Figure 4.1B. The underside of the working substrate in Figure 4.1C shows the underside of the substrate with observable defects throughout the electrode. The topography of the active polymer layer and top electrode of a completed device is seen in Figure 4.1D. The defect morphology is presented in Figure 4.1D and E. Substrates presented with a crazed surface consistent with environmental stress cracking of polycarbonate material due to solvent induced stress cracking of the polycarbonate.[1] Devices tested had open circuit resistances measured and were not suitable for transistor fabrication.

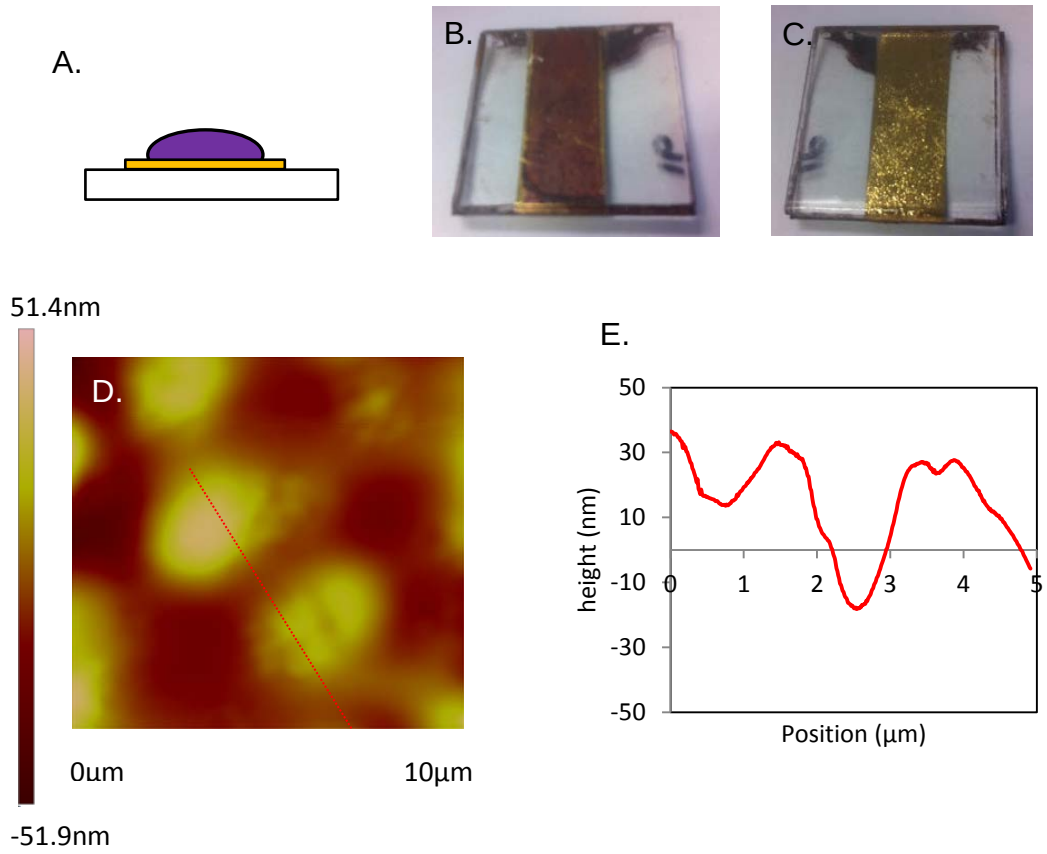

Figure 4.1. Atomic force microscope images on devices with observed stress cracking behaviour. A. Deposition schematic. B. Device substrate after the solution deposition of thin film. C. Underside of device substrate after thin film deposition D. 10µm x 10µm topographic image of top electrode in completed device. The area analysed through cross-section measurement indicated by the red line E. Cross section height analysis of polymer surface.

To prevent stress cracking UV-NVS resin was investigated as a protective layer to allow additional films to be cast over the UV-NVS film. Thin films of UV-NVS resin were spin coated onto polycarbonate substrates and UV cured. The UV curing of UV-NVS requires photo initiation at 250nm and 320nm wavelength light.[2] key to the preparation of thin polymeric films are the wetting properties of the UV-NVS material and the gold electrode substrate. Figure 4.2 shows the contact angle properties for UV-NVS and gold with water and 1,2-dichlorobenzene chlorinated solvent.

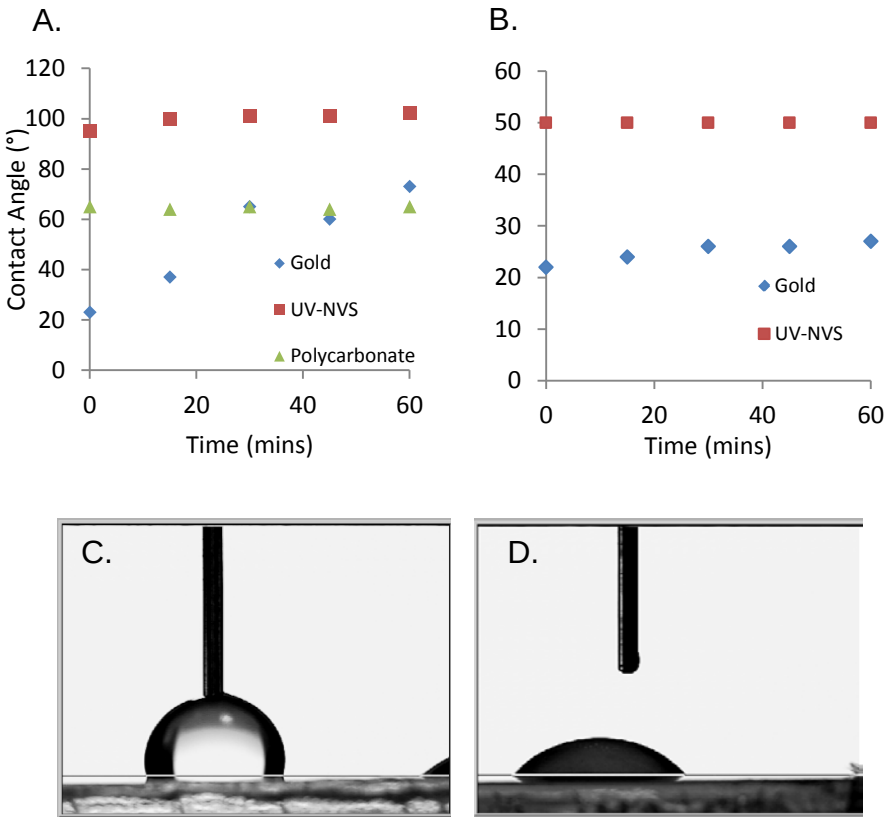

Figure 4.2. Contact angle measurements with respect to time. A. Water contact angle for UV-NVS (red square), polycarbonate (green triangle) and gold (blue diamond). B. 1,2-dichlorobenzene contact angle for UV-NVS (red square) and gold (blue diamond). C. Optical image of water droplet on UV-NVS film. D. Optical image of 1,2-dichlorobenzene droplet on UV-NVS.

Figure 4.2A shows the water contact angles for the electrical platform over a one hour test period. The UV-NVS protective layer shows a hydrophobic quality with a contact angle of 95° initially increasing to 101° after 60 mins. By comparison the pristine polycarbonate has a steady contact angle of 64°. Gold contact angle is seen to initially be very hydrophilic with a contact angle of 23° increasing to 73° after 60

mins. This increase in gold contact angle is documented and the result of exposure to ambient conditions resulting in a tarnished film at the top surface of the electrode.[3] The wetting properties of the materials using 1,2-dichlorobenzene are seen in Figure 4.2B. 1,2-dichlorobenzene shows a steady contact angle with UV-NVS of 50° and 22° increasing to 27° for gold over 60mins. Figure 4.2C and Figure 4.2D show the optical images for the water and 1,2-dichlorobenzene contact angle with UV-NVS respectively. UV-NVS forms a hydrophobic surface with high water contact angle and shows a low contact angle with 1,2-dichlorobenzene. The low contact angle with 1,2-dichlorobenzene for UV-NVS and gold makes it a viable platform for the future over coating of polymeric films out of chlorinated solvents. Completed UV-NVS films allowed the deposition of subsequent polymeric thin films from chlorinated solvents and prevented the polycarbonate substrate from solvent induced stress cracking.

4.2 Optimised P3HT Thin Film Morphology

Processing conditions have been shown to have a dramatic impact on thin film morphology. The choice of solvent,[4] temperature,[5] through to polymer solution age[6] all have varying impacts on the morphology of a spin coated thin film. The charge mobility, describing the ability for a material to conduct, is influenced by morphology. As such, morphology is seen to play a role in the performance of organic field effect transistors.[7-9]

4.2.1 P3HT AFM Studies

AFM was used to study the role of annealing temperature on the surface morphology of P3HT thin films. Films were prepared in a nitrogen environment and annealed for one hour in a nitrogen atmosphere on a temperature controlled hotplate. Samples were annealed under four test temperatures for 1hr- 50°C, 100°C, 150°C and room temperature measured at 26°C. Surface height profiles were obtained in tapping mode and can be seen in Figure 4.3.

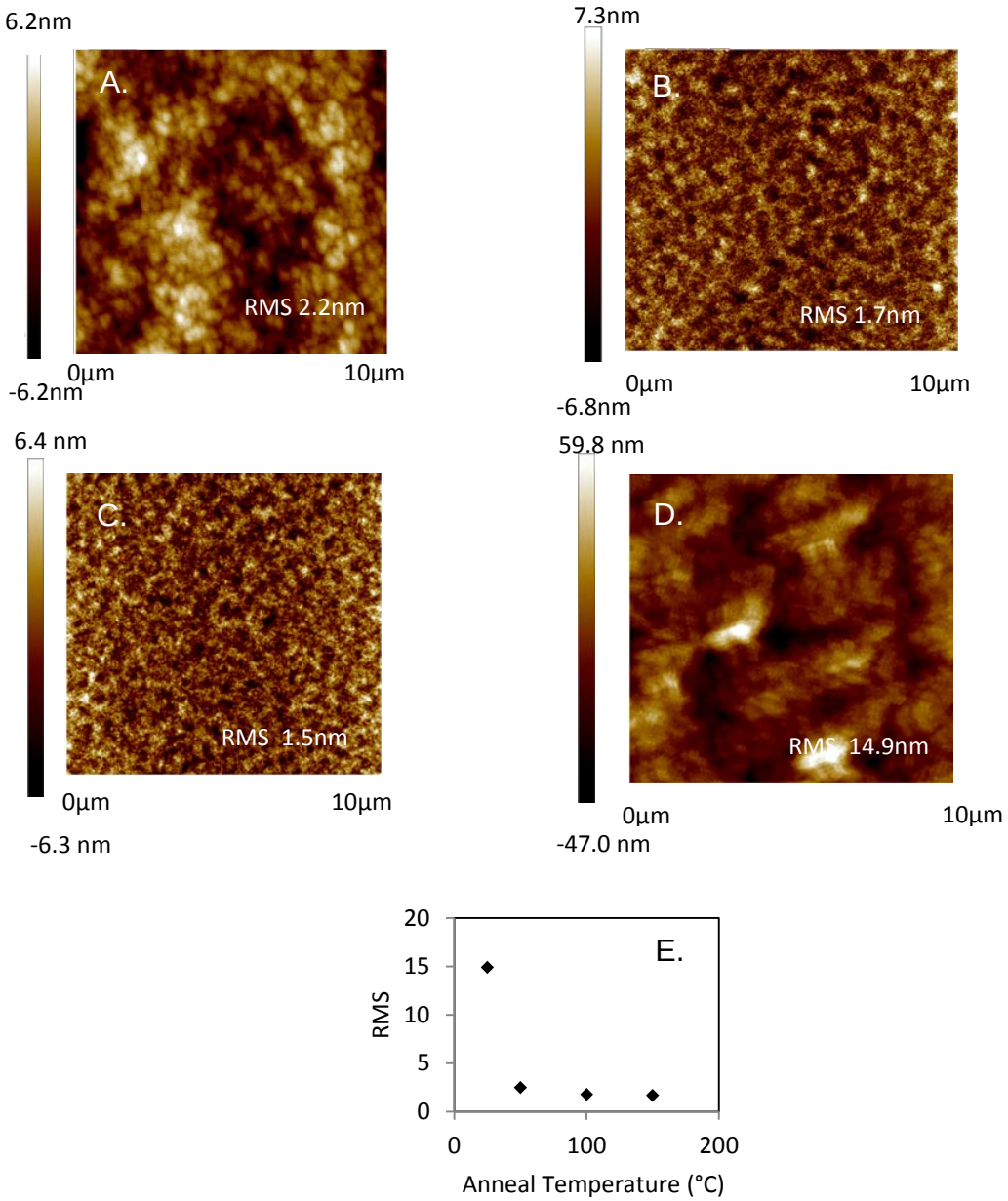

Figure 4.3. Comparison of 10um x 10um AFM height images of P3HT thin films with varying annealing temperatures A. 50°C , B. 100°C, C. 150°C and D. Room temperature. E. RMS roughness plotted with respect to anneal temperature.

The AFM height images were used to calculate a root mean square (RMS) for P3HT films. RMS values indicate varying roughness under anneal temperature with the roughest sample undergoing a room temperature anneal with an RMS of 14.9 nm. RMS roughness was seen to decrease with the increasing anneal temperature with 50°C samples having an RMS=2.2nm, 100°C=1.7nm and 150°C=1.5nm. Comparing favourably with the results of Nguyen *et al*.[10] who in in 2008 studied the internal

structure of P3HT and P3HT blends with conductive AFM (C-AFM) and obtained an RMS value for 150°C annealed thin films of 1% w/v P3HT of 1.7nm.

The roughness of the top surface of the polymeric film is an important aspect in the development of a two terminal device. The formation of an electrical contact at the interface of the polymer and working metal electrode is an important aspect in this research. A large interface roughness can result in the formation of energetic trap states, increasing the contact resistance within the circuit.[11] The sample at 150°C offers the lowest surface roughness and the high temperatures are known to increase the crystalline order throughout the material, increasing material mobility. [12] Do gain greater insight on the crystalline formation the conductivity of planar thin films of P3HT was examined with conductive AFM mapping to gain insight into the polythiophene crystal domains under varied anneal temperatures. Figure 4.4A shows the resulting topographic height sample with Figure 4.4B showing a cross section analysis across the specified location on the sample surface annealed at 150°C. Figure 4.4C and D show the corresponding current maps taken at 4V and cross section analysis.

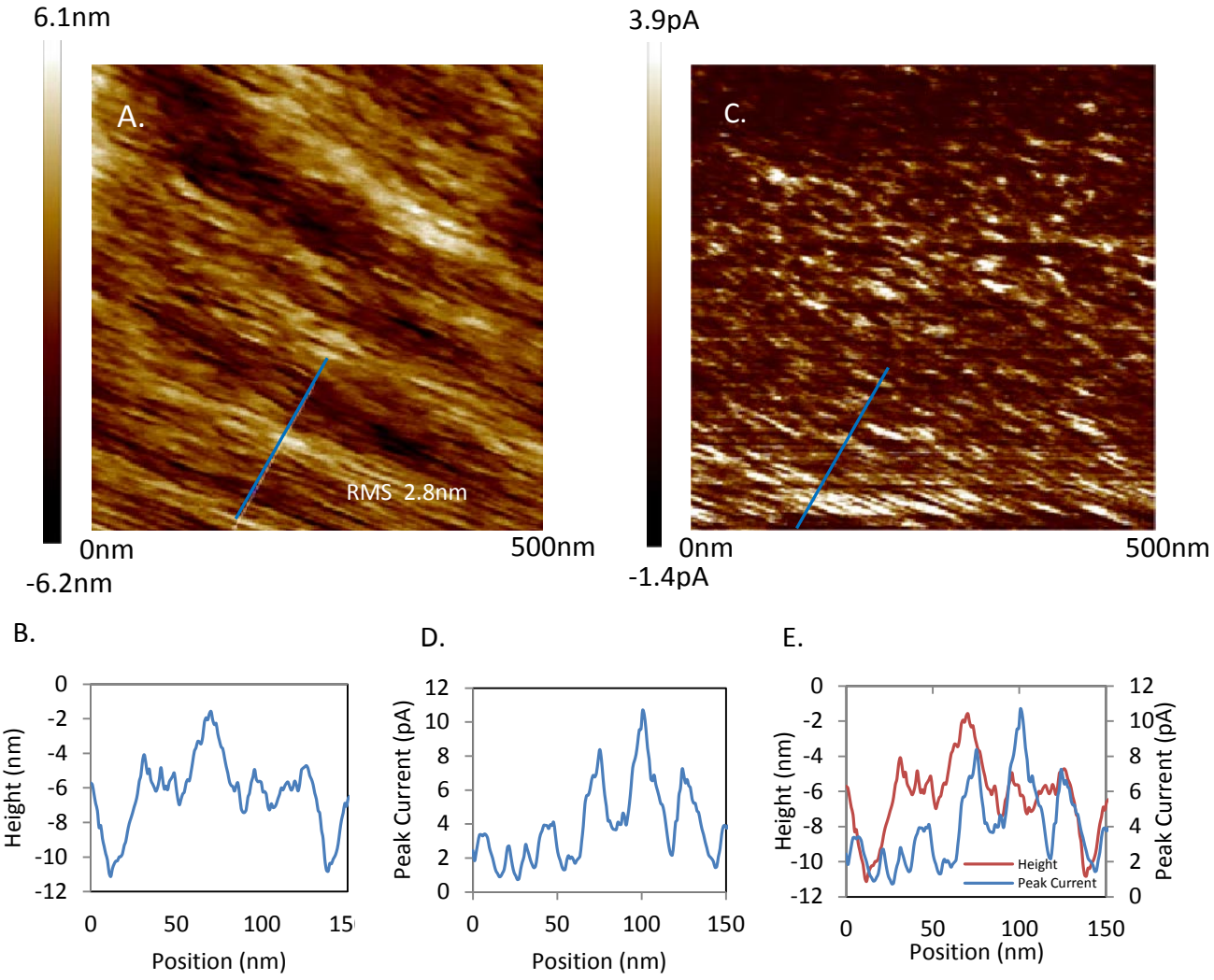

Figure 4.4. Conductive mapping of P3HT thin films A. 500nm x 500nm tapping mode height image of 150C annealed sample with area analysed by cross section (blue line). B. Cross section analysis showing height at the location labelled in A. C. Peak current conductive map over the imaged area with area analysed by cross section (blue line). D. Cross section analysis of the peak current magnitudes with respect to location. E. Superimposed topographic height and peak current cross section traces.

The cross section over the indicated region shows an average peak to peak spacing calculated to be 16.4nm corresponding to the known crystal packing of polythiophenes.[6] P3HT is known to orientate through alkyl chain backbones at a normal to the surface with the sp^2 carbon chains down the length of the backbone responsible for conduction.[13] Conductive mapping shows regions of conductivity across the sample surface, the pattern of these regions appears to show a correlation with the height morphology- locations of conductivity which show a degree of nanoscale order and spacing with a current on the order of picoamps was

measured as seen in Figure 4.4E. The obtained topography of the room temperature sample can be seen in Figure 4.5.

Figure 4.5A shows the resulting topographic height sample with Figure 4.5B showing a cross section analysis across the specified location on the sample surface annealed at room temperature. Figure 4.5C and D show the corresponding current map taken at 4V and cross section analysis. The obtained height images show topography with an RMS value of 10.4 which compares to the previously measured value for $10\mu m^2$ samples of ±14.9 nm. The topographic images for room temperature annealed samples show a surface with reduced order at the surface compared to that at 150°C with an increased roughness over the 150°C sample also. The spacing between peaks remains on the order of 15-20nm however, correlating with the 150°C annealed sample.

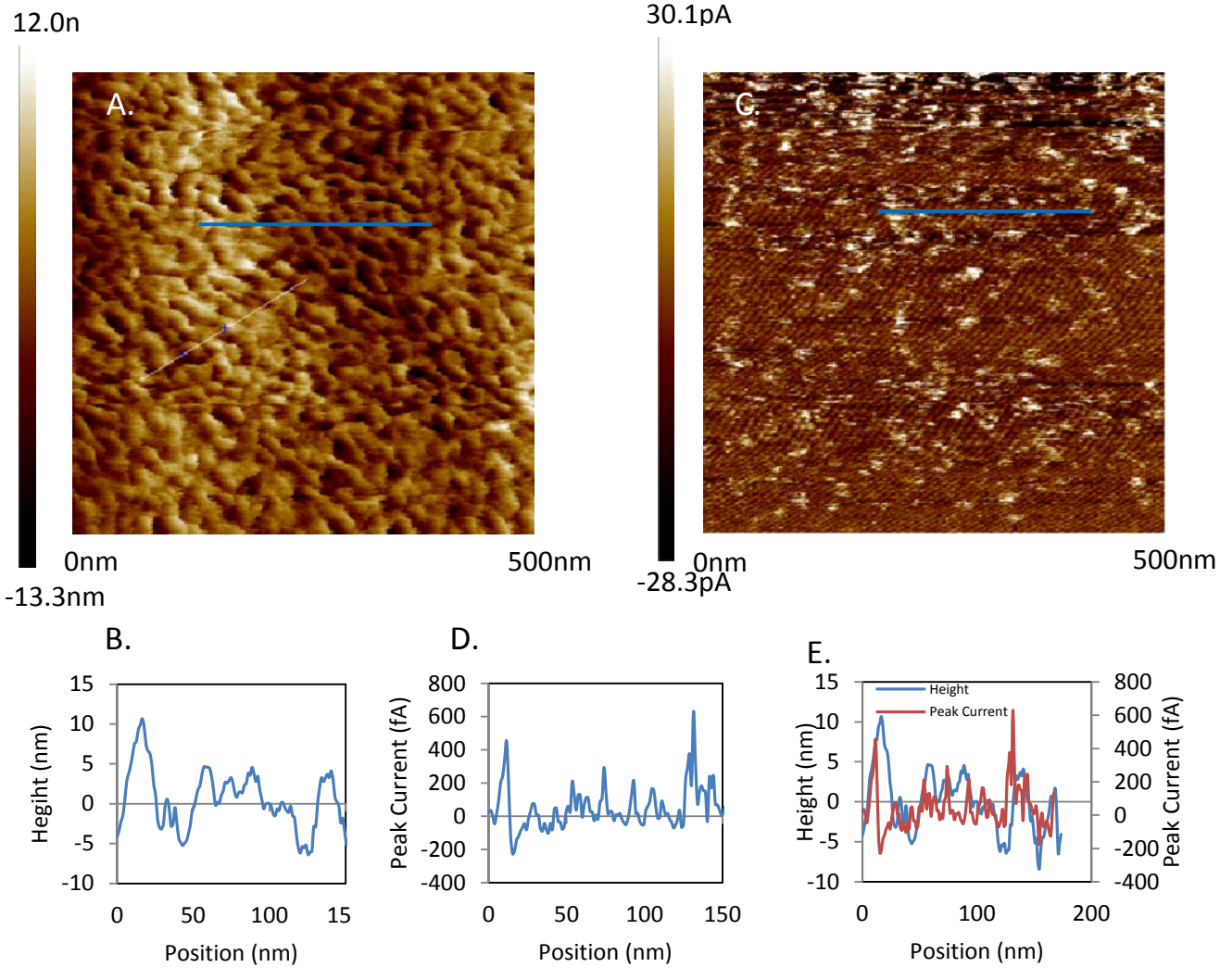

Figure 4.5. Conductive mapping of P3HT thin films A. 500nm x 500nm tapping mode height image of room temperature annealed sample with area analysed by cross section (blue line). B. Cross section analysis showing height at the location (blue line) A. C. Peak current conductive map over the imaged area. D. Cross section analysis of the peak current magnitudes with respect to location. E. Superimposed topographic height and peak current cross section traces.

The obtained conductivity map shows regions of conductivity with a reduced magnitude on the order 0.3pA for room temperature annealed surfaces. In comparison, the surface annealed at 150°C shows current on the order of femtoamps. The reason for this variation in current is unclear as both samples were imaged at 4V. The increased roughness of the surface may reduce the cantilever area in contact with the sample being imaged reducing measured current.[14] Furthermore, the conductivity map shows minimal long range order across the surface with the cross section correlation between current and topography seen in Figure 4.5E. The room temperature annealed conductivity map shows agreement with the height image suggesting observation of the edge on lamellar packing of the P3HT polymer under both anneal conditions. The use of the carbon nanotube tipped conductive probe has allowed for the highest resolution topographic images of thin films of P3HT to be acquired.[15]

Through *in situ* conductive mapping the height features of the P3HT thin film show locations of high current with the ordering of the topographic and height features seen to be impacted by anneal temperature. An anneal temperature of 150°C was shown to produce the lowest roughness thin films with an RMS of 1.5nm producible and was employed to reduce interface roughness and improve device performance.

4.3 Layered Structures on Polycarbonate

4.3.1 Considerations

During the fabrication and development of electrical devices consideration to the deposition of working electrodes and the device failure rate is essential to developing a robust electrical platform. Electrical devices require reproducible electrode contacts capable of consistent electrical contact during measurement. Two methods to deposit patterned electrodes were investigated for use with polycarbonate substrates, direct current sputtering of metals through manually aligned shadow masks and evaporation of samples utilising a mounted sample stage

and physically aligned shadow masks. Direct current sputter coating with a combination of manual alignment of masks provides a faster throughput technology with a lower associated cost of production.[16] The two deposition methods are compared using a model spin coated polymer film of P3HT with a thickness of 225nm as the active layer with a gold bottom electrode. The failure rate is determined by the yield of short circuited devices which will be used to evaluate the fabrication method.

4.3.2 Sputter Coating of Electrodes via Manually Aligned Shadow Masking

Shadow masks were designed so that polycarbonate substrates with thin polymer films could have electrodes deposited using a Quorumtech K757X sputter coater under a pressure of 10^{-3} Torr. Figure 4.6 shows the patterning sequence utilised when using a manually aligned shadow mask. The mask design featured a 25.4mm stainless steel backing strip and several 20mm fingers spot-welded down the backing strip at a spacing of ~ 0.2mm, allowing the deposition of several narrow fingers by masking (Figure 4.6A). The mask patterns a symmetric gold electrode with two shared equipotential electrodes in the shape of a ribcage (Figure 4.6B) on to the polycarbonate substrate. Over which the polymeric solution was spin coated. The mask was further modified through a masking tape to create a pattern for top contacts to be manually aligned and to register with the bottom electrode (Figure 4.6C). The mask was aligned by matching the straight edge of the mask with the straight edge of the substrate *in situ* prior to metal sputtering. The resulting electrode pattern can be seen in Figure 4.6D. The resulting pattern created two rows of devices when polymer was spin coated onto Figure 4.6B with all devices in a row sharing a bottom electrode contact with a total of 12 devices per substrate. The obtained device failures from short circuits are shown in Figure 4.6E for three sputtered electrode metals.

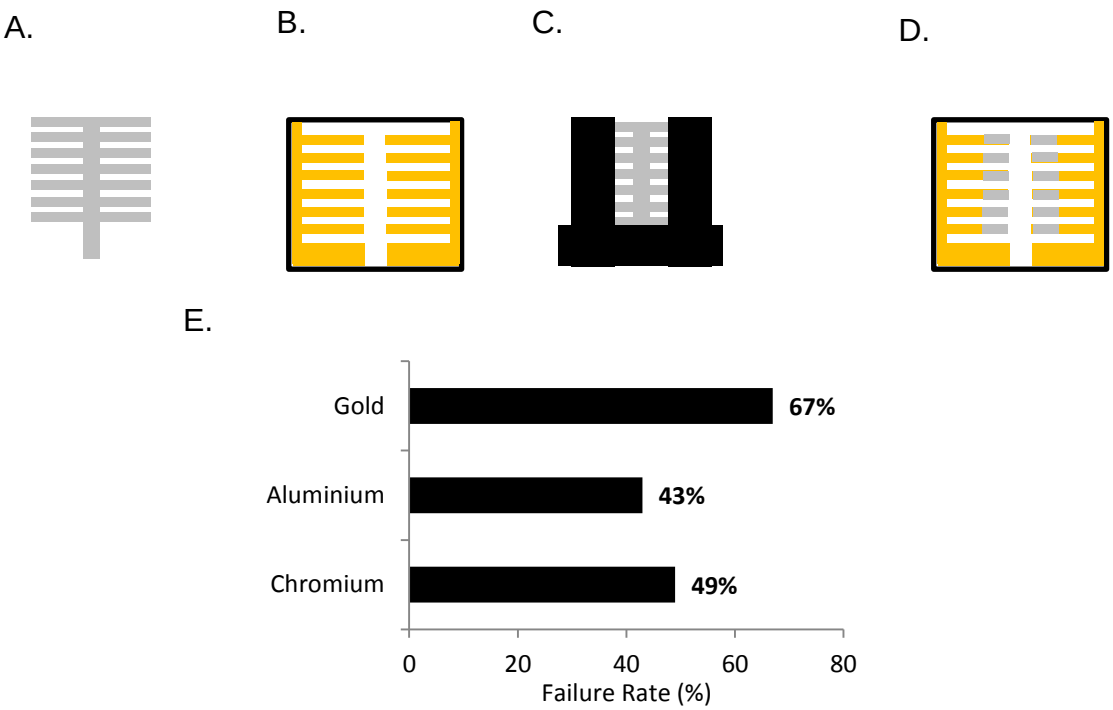

Figure 4.6. Electrode patterning work flow for a manually aligned shadow mask featuring a rib cage design allowing thin ~ 0.2mm wide devices. A. Manually aligned rib cage shadow mask. B. Resulting patterned electrode post metal deposition. C. Manually aligned rib cage mask with functional taping. Resulting patterned top electrode. E. Failure rate for devices with various sputtered metal electrodes gold, aluminium and chromium.

The devices fabricated with an aluminium electrode resulted in the lowest short circuit failure rate at 43%, chromium devices performed with a failure rate of 49% and devices with a top sputtered gold electrode showed the highest failure rate at 67%.

To identify the failure mode, a shadow mask featuring a uniform gold communal electrode was designed with the work flow is with the steps taken to pattern substrates using the mask shown in Figure 4.7. A mask featuring a rectangular 25mm x 25mm pattern was created out of brass material (Figure 4.7A). Alignment involved marking the middle of the working substrate with a stationary reference point and ensuring that the rectangular electrode was deposited in the middle of the substrate resulting in the pattern seen in Figure 4.7B. An additional top electrode was designed which was based on the previous design. This time it incorporated machined circles through the fingers creating a larger contact patch on the deposited electrodes to allow for reproducible contact seen in Figure 4.7C.

Furthermore, the top electrode contact fingers were designed with a controlled spacing- between 0.1mm-0.8mm creating various device areas and allowing for assessment of device failure with respect to electrode width as seen in Figure 4.7.

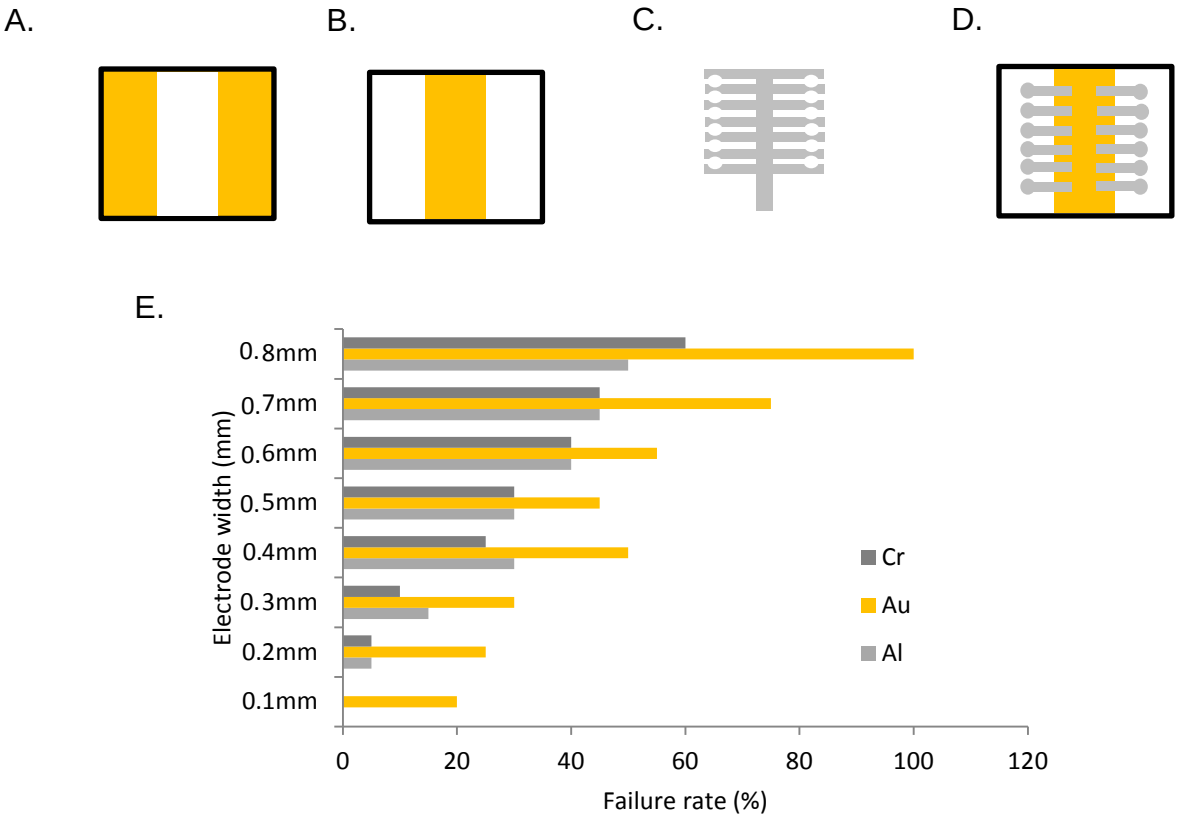

Figure 4.7. Electrode patterning for a manually aligned shadow mask featuring a rib cage design allowing for variable cross-sectional area. A. Uniform communal electrode shadow mask. B. Resulting patterned electrode. C. Top ribcage shadow mask with contact patch and variable electrode width. D. Resulting patterned top electrode. E. Failure rate for devices with various sputtered metal electrodes gold, aluminium and chromium with varied electrode width.

The deposition of top electrodes shows an increase in failure rate as the width of the top electrode and subsequent device area is increased. The high rate of failure caused by sputter coating has also been attributed to the higher energy of sputtered ions compared to physical vapour deposition which can damage the sputtered surface through ion bombardment promoting the shorting of devices. [17] The ion damage can further hamper the formation of a pure metal-semiconductor contact.[18] Furthermore, the poor performance for gold sputtering may be a result of diffusion of gold atoms through polymer and silicon material due to its inert nature.[19, 20]

4.3.3 Evaporation of Electrodes with a High Accuracy Sample Mount and Shadow Mask

Evaporation was investigated as a lower energy process to deposit top electrodes. Using the Angstrom Covap II the shirt circuit failure rate for batch processing of two terminal devices with patterned electrodes on polycarbonate substrates was investigated. Three substrates with 24 two terminal cells were examined for two different electrode pattern depositions. Shown in Figure 4.9 a communal electrode pattern was compared to a discrete electrode pattern which allowed for each individual device to have a discrete contact for electrical measurement.

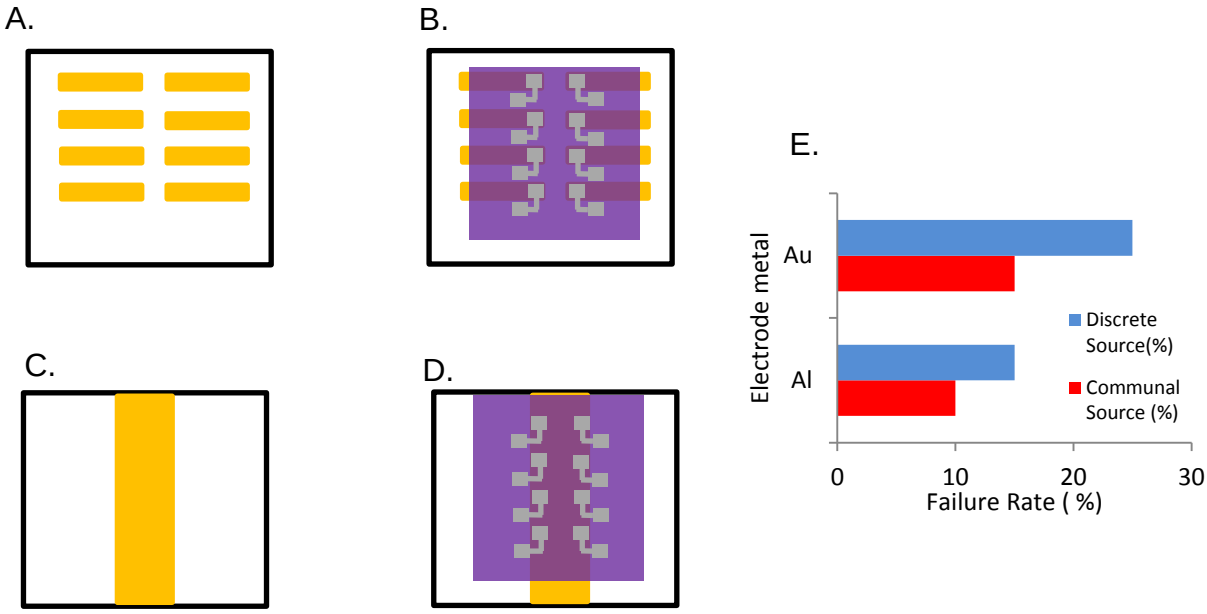

Figure 4.8. Electrode pattern schematics. A. Discrete electrode pattern. B. Resulting device fabricated with top electrode. C. Communal electrode pattern. D. Resulting devices fabricated with top electrode. Cross sectional area 1.5mm^2 ±0.01mm^2. E. Failure Rates for gold and aluminium top electrode devices with communal (blue bar) and discrete source (red bar) pattern.

Devices fabricated with an aluminium top electrode showed a failure rate of 10% in the communal electrode device configuration. With a discrete electrode configuration failure rate was shown to be 15%. For gold top electrode devices with a communal source showed a failure rate of 15%. Gold top electrode devices with a discrete source showed a failure rate of 25%. Failure rate increased for a device with discrete source electrode configurations that used aluminium and gold metals as the top electrode, increasing 5% for Aluminium and 10% for gold. When

compared to sputter deposited top electrode devices failure rate is reduced in evaporated devices.

Capable of reduced failure rates with larger cross sectional area an evaporative approach is ideal in the fabrication of two terminal devices. Gold top electrode devices show a higher overall failure rate under both deposition methods attributed to diffusion into the polymer increasing the likelihood of shortages. In 2002 Thran *et al.*[21] showed that noble metals can show trace concentrations up to 400nm into trimethylcyclohexane polycarbonate polymer. It should also be noted a discrete source configuration is highly advantageous when observing the performance of two terminal, and three terminal devices. When applying a voltage across a two terminal device that incorporates a communal source, the bottom electrode acts as a node, effectively biasing all cathodes with respect to the anode. Constantly biasing a device could alter the electrical characteristics and prematurely degrade a device and promote the diffusion of metal through the polymer material.[22, 23] Discrete electrode devices, employing either gold or aluminium top electrodes were able to be fabricated with a success rate of at least 75%.

4.4 Schottky Barrier Devices

Producing vertical devices with low reverse current magnitude is a key challenge in developing a well performing transistor structure. Schottky diodes are a unique and novel solution to reduce reverse currents in a vertical transistor structure whilst retaining a large operational area.[24-26] Schottky diodes were fabricated using a P3HT active layer with aluminium cathode and gold anode. Due to a mismatch in work functions between Al (W_f = 4.2eV) and P3HT (HOMO= 4.9eV) when the two materials are brought into contact, charges diffuse across the interface forming a rectifying junction.[27] Schottky diodes were electrically characterised through the application of a potential voltage across the aluminium electrode and gold electrode measuring the output current at the aluminium cathode under an applied potential voltage. With the measured current - voltage trace providing information

on the behaviour of charge carriers within the two terminal Schottky devices and the device itself. The schematic shown in Figure 4.9A shows the substrate schematic for Schottky device substrates and Figure 4.9B shows the testing biases under which electrical characterisation took place. A portion of the polymer coated gold contact is exposed post spin coating by dipping a cotton cue tip in toluene and removing polymer allowing electrical contact to be made with the gold electrode. Devices are tested sequentially with two sides of 4 devices being fabricated totalling 8 devices on the substrate.

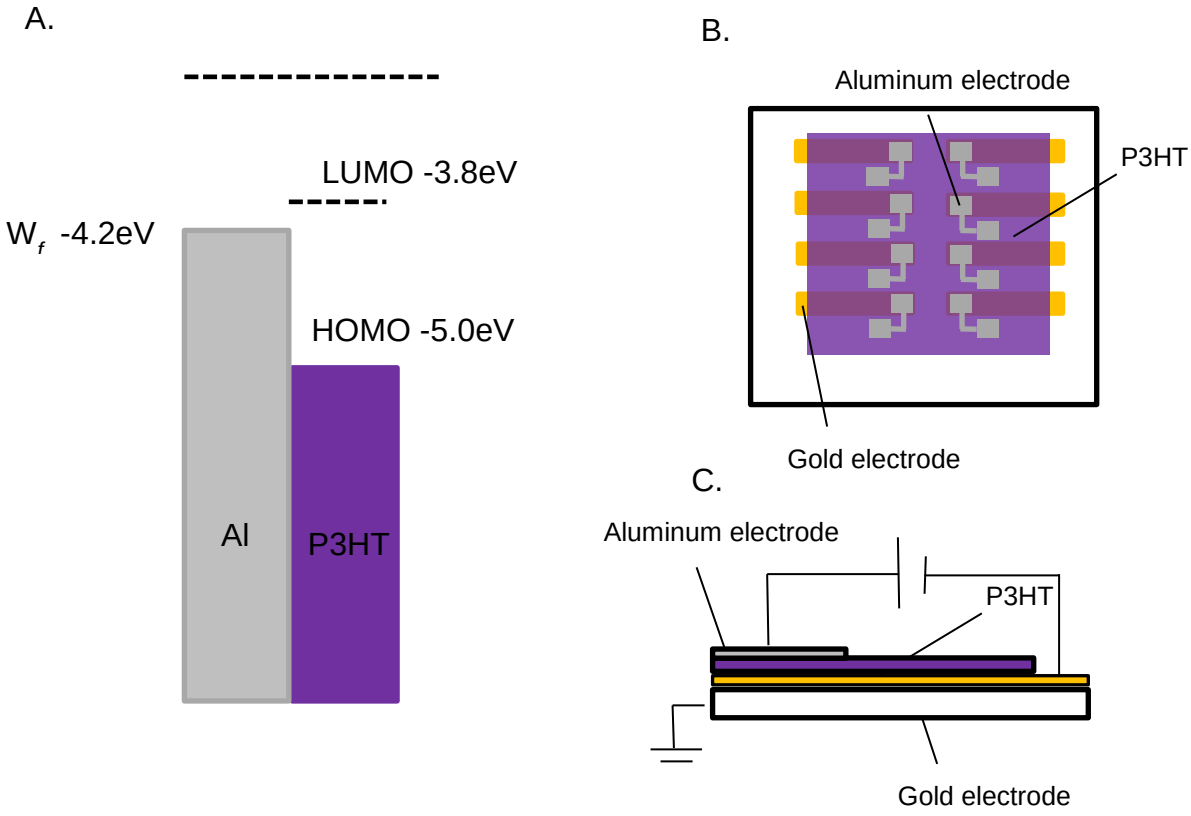

Figure 4.9. Fabricated P3HT-aluminium Schottky diodes. A. Energy level diagram at the P3HT-Al interface. B. Top view substrate schematic for two terminal Schottky barrier substrates C. Side view electrical characterisation cross section schematic indicating applied biases under testing for two terminal devices on polycarbonate. [27]

During the testing of two terminal devices the potential applied across the gold and aluminium electrodes creates an electric field producing a current which due to the p-type nature of P3HT is conducted through hole charges as the majority charge carrier.[28] Using the device substrate schematic seen in Figure 4.9B the polymeric electrical channel is created between the cross-sectional area of the metal

electrodes. With P3HT a forward current will be measured under negative applied voltages in the -/- quadrant of the I-V trace operating under forward bias conditions.

4.4.1 Schottky Diode Equivalent Circuit

Figure 4.10 shows the proposed two terminal device equivalent circuit for use in the DC analysis of fabricated Schottky diodes. In Figure 4.10A the cross section of a fabricated two terminal showing passive circuit elements within the device. Figure 4.10B shows the full equivalent circuit of the device. The role of the parameters $cap_{junction}$, $\boldsymbol{\Omega_{shunt}}$, Ω_{series} and ideality factor have been simulated for the Schottky diode equivalent circuit using the Shockley equation and is presented in Appendix B. A capacitance term, $cap_{junction}$ describes the parasitic capacitance at the Schottky junction. The other key characteristics of the equivalent circuit are a series resistance Ω_{series}, determining the intrinsic resistance describing the voltage drop across the bulk channel and the shunt resistance term, Ω_{shunt} describing the reverse and leakage currents through the device.

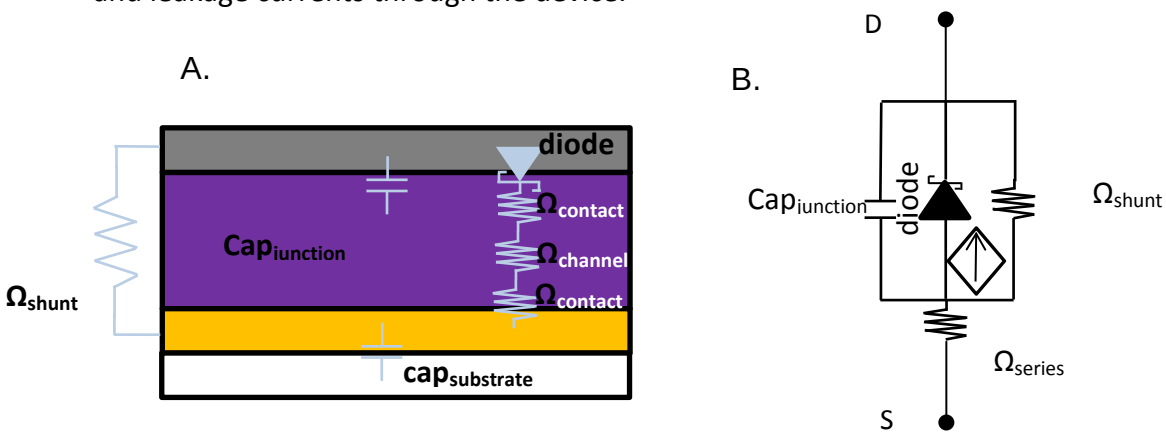

Figure 4.10. Schottky diode equivalent circuit A. Side view schematic of a two terminal device indicating elements of equivalent circuit. The contributions to the series resistance, $\boldsymbol{\Omega_{contact}}$ and $\boldsymbol{\Omega_{channel}}$, the junction capacitance $\boldsymbol{cap_{junction}}$, the shunt resistance $\boldsymbol{\Omega_{shunt}}$ and the Schottky barrier. B. Proposed equivalent circuit based on the Shockley equation.

Theoretically, the introduction of the Schottky barrier between the source and drain reduces reverse currents and leads to lower reverse currents in three terminal devices. This is due to the shunt resistance term, Ω_{shunt} being present in the circuit and a rectifying junction at the drain electrode. The forward current of the device is determined by the series resistance Ω_{series} and the contribution of the contact resistance, $\Omega_{contact}$. Understanding the changes in Ω_{series} and Ω_{shunt} in the two

terminal Schottky devices is an important step in realising a three terminal device featuring a Schottky barrier. The two terminal device Schottky barrier devices form the source-drain equivalent circuit and determine leakage currents in a completed device. Towards the development of a three terminal device, Ω_{series} and Ω_{shunt} need to be reproducible and not vary with repeat testing or time ultimately improving device performance and improving the resolution to observe transistor behaviour during electrical characterisation.

4.5 Forward Current and Rectification Ratio dynamics.

Electrical characterisation of two terminal Schottky devices on polycarbonate was undertaken in order to develop a reliable two terminal electrical platform capable of future processing towards a three terminal device. A nitrogen test chamber described in §2.4.2 was used allowing for testing and analysis of devices without exposure to atmosphere.

4.5.1 Time Dependence of Device Performance

Devices were transferred into the inert testing chamber after fabrication and were tested sequentially. Current-voltage traces were obtained for each point over the range ±4V with a sweep rate of $0.65V.s^{-1}$. The current-voltage characteristic was observed over 30 mins with a periodic scan every 60s the difference can be seen in Figure 4.11.

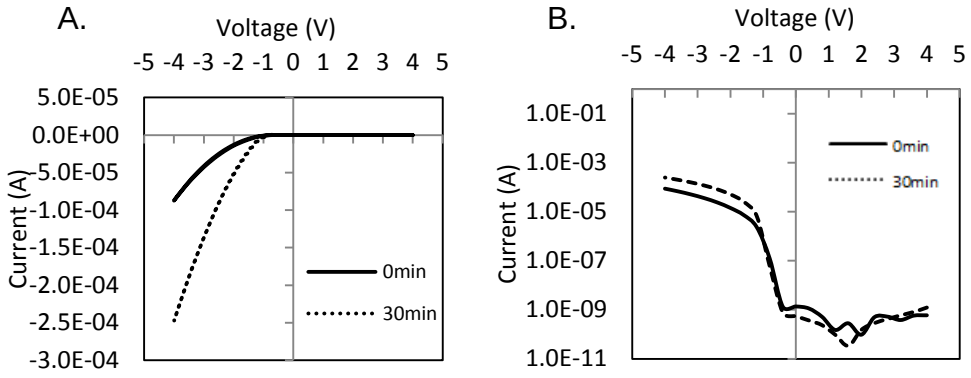

Figure 4.11 .Two terminal Schottky barrier device current-voltage characterisation immediately after fabrication. A. -/- quadrant output plot over a 30 min testing period. Initial trace (solid line) and after 30mins testing (dashed line) B. Log vs. V characteristic plot for two terminal Schottky barrier devices. Devices were tested in a nitrogen environment after the deposition of evaporated aluminium.

Current-voltage traces for newly fabricated devices show an increasing forward current. In Figure 4.12A the forward current is plotted with respect to time for an immediately tested discrete electrode device. Figure 4.12B shows the ON/OFF rectification performance of the device over that time. The performance over the sequential 30min study period was analysed with respect to the proposed equivalent circuit. The obtained experimental current-voltage traces for devices on the substrate were fitted to the proposed equivalent circuit through the procedure outlined in Appendix B. with complete performance for the substrate and extracted circuit parameters presented in Appendix C.

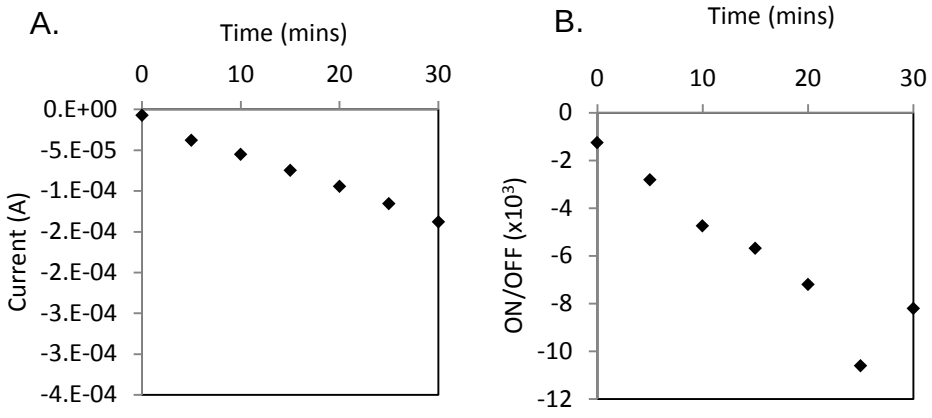

Figure 4.12. Forward current increases in fabricated devices as a function of time over 30mins of testing. A. Forward current performance. B. Rectification ratio over 30mins testing.

Figure 4.13 shows the equivalent circuit performance for newly fabricated two terminal Schottky devices on polycarbonate. Series resistance is seen to start at high values and decrease over the study period to lower values, reciprocating the behaviour of forward current during the study. The series resistance is seen to be highest at the beginning of the experiment with Device 1 showing resistance Ω_{series}=125kΩ reducing to 28kΩ changing 97kΩ over the 30mins. The lowest series resistance is measured in Device 5, the final device tested with initial Ω_{series}= 10kΩ reducing to 8.7kΩ changing 1.3kΩ over the testing period.

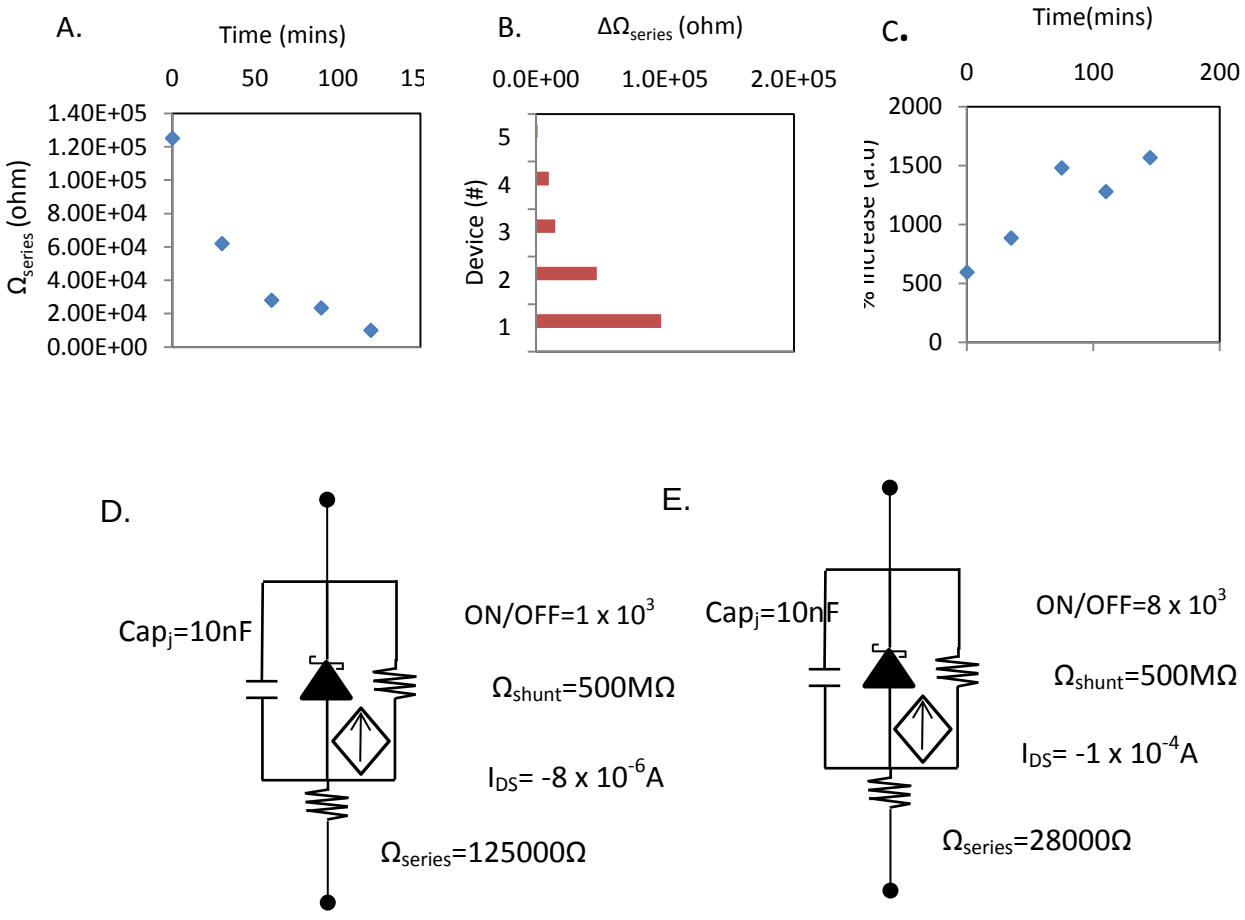

Figure 4.13. Equivalent Circuit behaviour for an immediately tested device substrate. A. Simulated series resistance of devices with respect to time after electrode deposition. B. Changes in series resistance over 30mins of consecutive testing. C. Percentile increase in forward current with respect to time after electrode deposition. D. Simulated equivalent circuit for a device immediately removed from vacuum E. Simulated equivalent circuit after 30mins of consecutive testing.

This results in a time varying series resistance element in the equivalent circuit. With devices tested two hours after electrode deposition showing a reduced change in the series resistance over the period of study of 1.25kΩ. Suggesting two hours

after deposition the variation in the runs is significantly reduced. Lous *et al.[29]* has shown the time based formation of the Schottky barrier due to interface kinetics between the deposited electrode and polymer in a comparable system that featured a Schottky barrier between a polythiophene oligomer and eutectic alloy. This suggests that the time based formation of the P3HT/Al Schottky barrier is resulting in run to run variation for the platform.

4.5.2 Vacuum Stored Devices.

In order to ensure complete formation of the Schottky barrier devices were fabricated and stored for 20 hours under vacuum and electrically characterised. Fabricated devices were stored at 10^{-6} Torr vacuum for 20hr after electrode deposition and transferred into the testing chamber and electrically characterised. A representative current- voltage trace is seen in Figure 4.14.

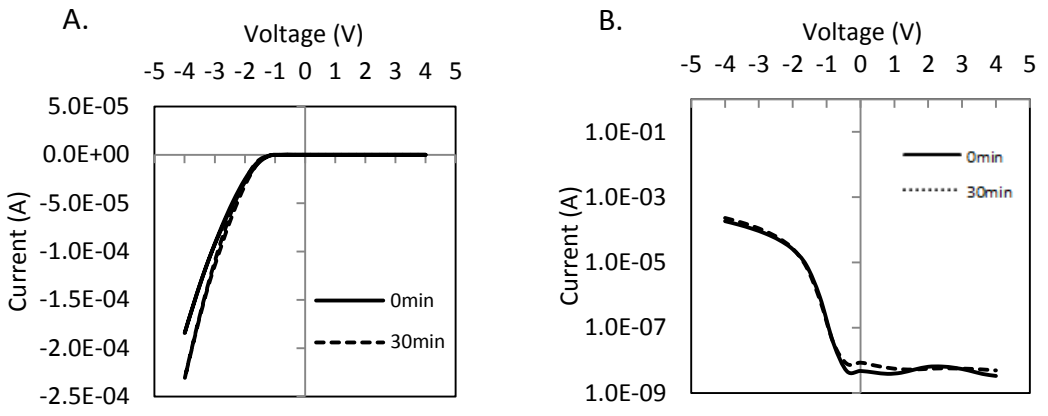

Figure 4.14 . Two terminal Schottky barrier device current-voltage characterisation immediately after fabrication. A. -/- quadrant output plot over a 30 min testing period. Initial trace (solid line) and after 30mins testing (dashed line). B. Log vs. log scale characteristic plot for two terminal Schottky barrier devices. Initial trace (solid line) and after 30mins testing (dashed line). Devices were tested in a nitrogen environment 20hrs after the deposition of evaporated

Vacuum stored devices show improved forward current magnitude over immediately tested devices. With the forward current -1.8 to -2.3X10^{-4}A comparable to devices one hour after aluminium electrode deposition and an increase over newly fabricated devices of over an order of magnitude. In Figure 4.15A the initial forward current is plotted with respect to time and the ON/OFF

performance plotted in Figure 4.15B. Additional plots for all devices tested are provided in Appendix C.

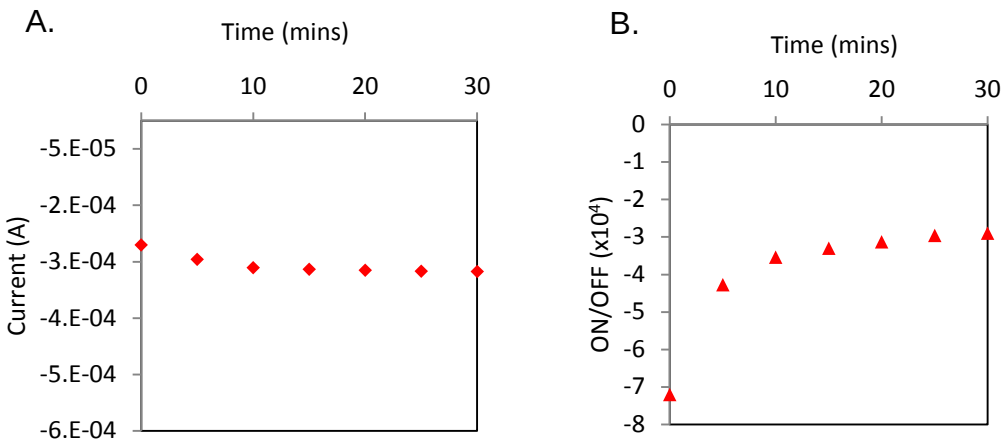

Figure 4.15. Forward current increases in vacuum stored devices as a function of time over 30mins of testing. A. Forward current performance. B. Rectification ratio over 30mins testing.

The series resistance is seen to be in the range of 23kΩ-15kΩ at the beginning of the 30mins study period shown. A change in series resistance over the 30min testing period is measured to be 2.5kΩ. The equivalent circuit performance for vacuum stored devices is shown in Figure 4.16.

Figure 4.16A graphs the series resistance across all devices with respect to the time measured. Series resistance shows no correlation with time for vacuum stored devices. Figure 4.16B shows the difference between series resistance at the initial testing point and after the 30min study period. The time variation in the vacuum fabricated devices is greatly reduced including the resulting increases in forward current seen in Figure 4.16C. Producing an equivalent circuit with reduced run to run variation and time based variation. Over the 30min devices are seen to reach 88% of their final current within 5min and 94% over 10 min.

Devices stored in vacuum storage for 20 hours show reduced increases in the forward current under the same experimental conditions. Due to minimal changes in forward current, the rectification ratio in vacuum stored devices has greater consistency over successive runs and is independent of time.

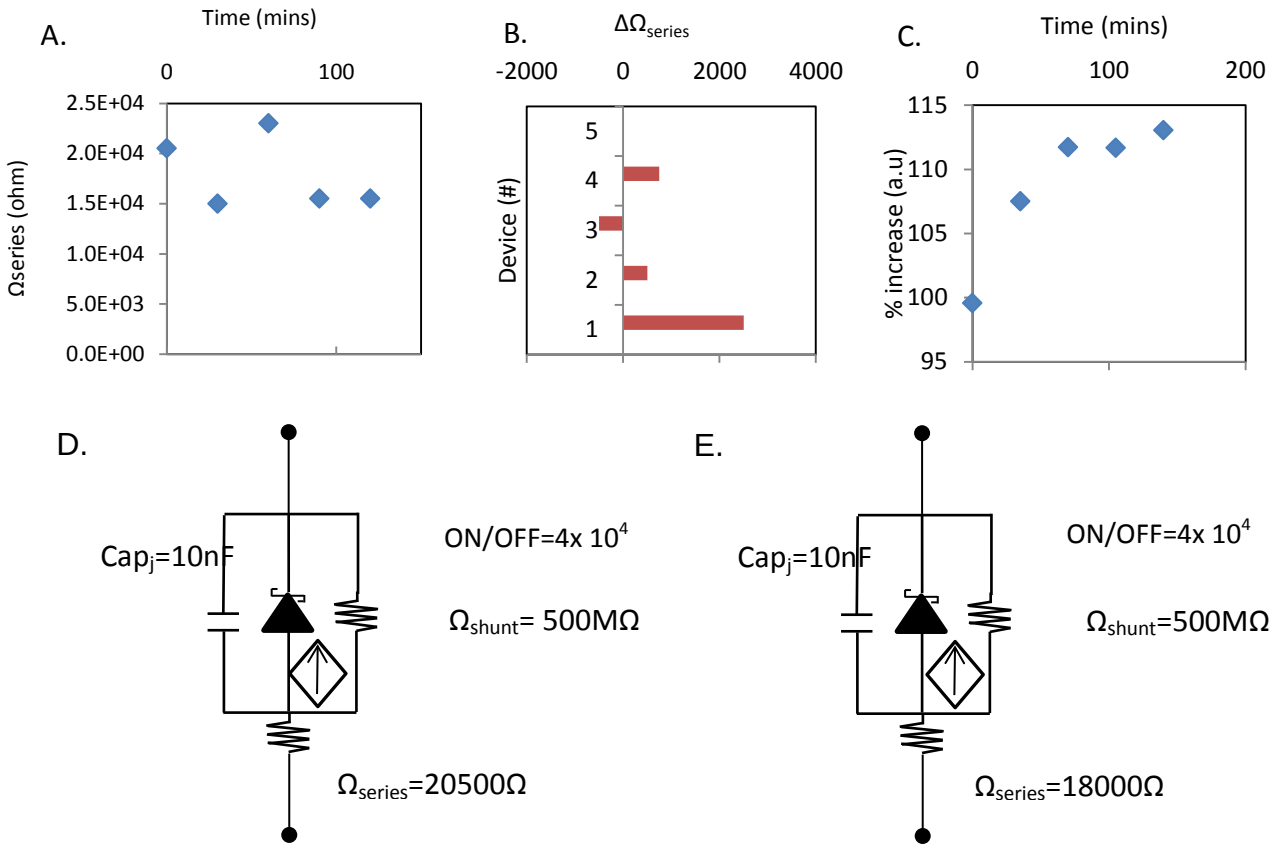

Figure 4.16. Device substrates stored in vacuum for 20 hours A. Simulated series resistance of devices with respect to time after electrode deposition. B. Changes in series resistance over 30mins of consecutive testing. C. Percentile increase in forward current with respect to time after electrode deposition. D. Simulated equivalent circuit for a device immediately removed from vacuum E. Simulated equivalent circuit after 30mins of consecutive testing.

20 hours of vacuum resting is seen to produce a more reliable device with improved performance. Allowing any future processing of the device to yield more stable electrical performance and improve the resolution of any field effect.

4.6 Statistical Analysis of Two Terminal Schottky Diodes

To understand variability in fabrication procedures from one substrate and device to others, a statistical analysis of 60 devices was made with the aim of being able to produce results with significance from fewer individual samples. Device electrical characteristics were taken over 10 device substrates that had been stored for 20 hours under vacuum before testing. Collected current-voltage data was analysed with respect to the position of the device relative to the substrate. The 4 x 2 distribution of devices as produced by the electrode pattern (as seen in Figure 4.9) produced four sets of positional data with the two columns of devices considered symmetrical with data categorised by their vertical positions Position 1-4. With position 1 the top most devices near the substrate edge and position 4 the lowest in the array. Figure 4.17 shows the distribution of forward and reverse current by position and the standard deviation measured for each data set. Table 4.1 shows the statistics for analysed forward and reverse currents over the 60 devices with respect to the position on the substrate.

The measured standard deviation for forward current in devices is shown in Figure 4.17A,B,C and D and is seen to be largest for position 1 (Figure 4.17A) and 4(Figure 4.7D) at 4.85×10^{-4} A and 2.60×10^{-4}A respectively when compared to position 2 (Figure 4.17B) and 3(Figure 4.17C) at 2.50×10^{-4} A and 1.98×10^{-4}A respectively. A similar trend is seen with the reverse current standard deviation with position 1 and 4 (2.63×10^{-6} A and 3.80×10^{-4}A respectively) when compared to position 2 and 3 (1.56×10^{-6} A and 2.06×10^{-6}A respectively). The mean measured forward current is also increased in devices in Position 1 and 4 (I_{FWD}= -6.12×10^{-4} A and -5.65×10^{-4}A respectively) compared to position 2 and 3 (I_{FWD}= -4.58×10^{-4} A and -4.87×10^{-4}A, respectively). The results show a greater variability in the devices fabricated in positions 1 and 4 attributed to the positioning of the devices further to the substrate edge in comparison to position 2 and 3. The higher mean forward current suggests thinner device active layers for devices in position 1 and 4. Device position 2 and 3 are surrounded by the gold electrodes of position 1 and 4 and are located

closer radially to the centre during the solution processing potentially improving the homogeneity and consistency of thin films over the region.

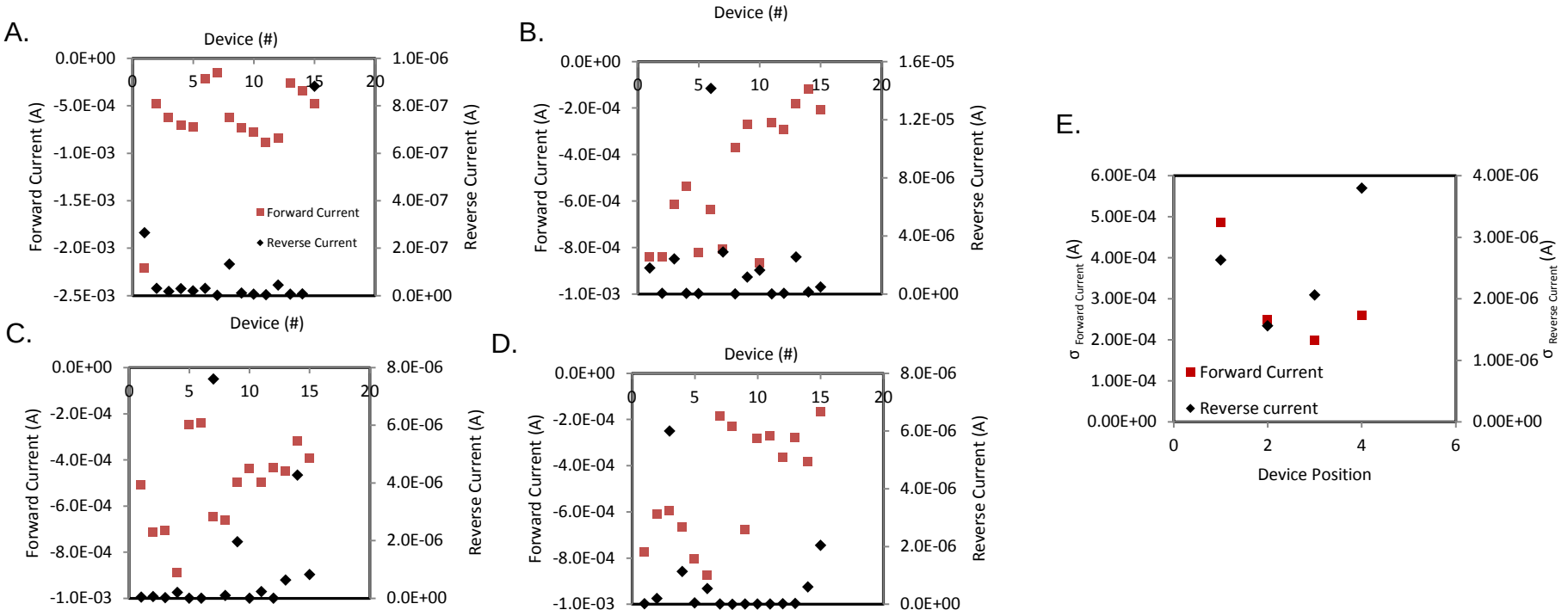

Figure 4.17. Distribution of forward current (red) and reverse currents (black) with respect to device position and the resulting standard deviation. A. Distribution of currents in position 1. B. Distribution of currents in position 2. C. Distribution of currents in position 3. D. Distribution of currents in position E. Calculated standard deviation by device position.

Table 4.1. Satistically averaged forward and reverse diode currents.

	Combined		*Position 1*		*Position 2*		*Position 3*		*Position 4*	
	I_{FWD} (A)	**I_{REV} (A)**	**I_{FWD} (A)**	**I_{REV} (A)**	**I_{FWD} (A)**	**I_{REV} (A)**	**I_{FWD} (A)**	**I_{REV} (A)**	**I_{FWD} (A)**	**I_{REV} (A)**
Mean	-5.53E-04	9.58E-07	-6.12E-04	2.88E-07	-4.58E-04	7.99E-07	-4.87E-04	9.79E-07	-5.65E-04	2.05E-06
Standard Error	3.49E-05	1.25E-07	1.18E-04	1.85E-07	6.24E-05	3.90E-07	4.95E-05	5.16E-07	7.22E-05	1.05E-06
Median	-5.41E-04	3.49E-08	-6.26E-04	2.79E-08	-3.74E-04	3.42E-08	-4.73E-04	1.54E-07	-6.16E-04	1.16E-06
Std. Deviation	3.21E-04	2.61E-06	4.85E-04	2.63E-06	2.50E-04	1.56E-06	1.98E-04	2.06E-06	2.60E-04	3.80E-06
Largest	-2.21E-03	1.41E-05	-2.21E-03	2.24E-09	-8.75E-04	2.43E-09	-8.89E-04	2.90E-09	-8.68E-04	2.45E-09
Smallest	-8.89E-04	2.24E-09	-1.20E-04	3.17E-06	-1.66E-04	6.00E-06	-1.57E-04	7.75E-06	-1.83E-04	1.41E-05

Over the 60 device sample the mean forward current was -5.53 x10^{-4} A over the range -2.21 x 10^{-3} A to -8.89x 10^{-4} A. The mean reverse current was 9.58x 10^{-7} A over the range 1.4 x 10^{-5} A to 2.24 x 10^{-9} A. The range of the reverse current shows a range over four orders of magnitude whilst forward currents span one order of magnitude. An averaged capacitance and shunt resistance was simulated from the current-voltage behaviour and a statistically determined equivalent circuit proposed in Figure 4.18A.

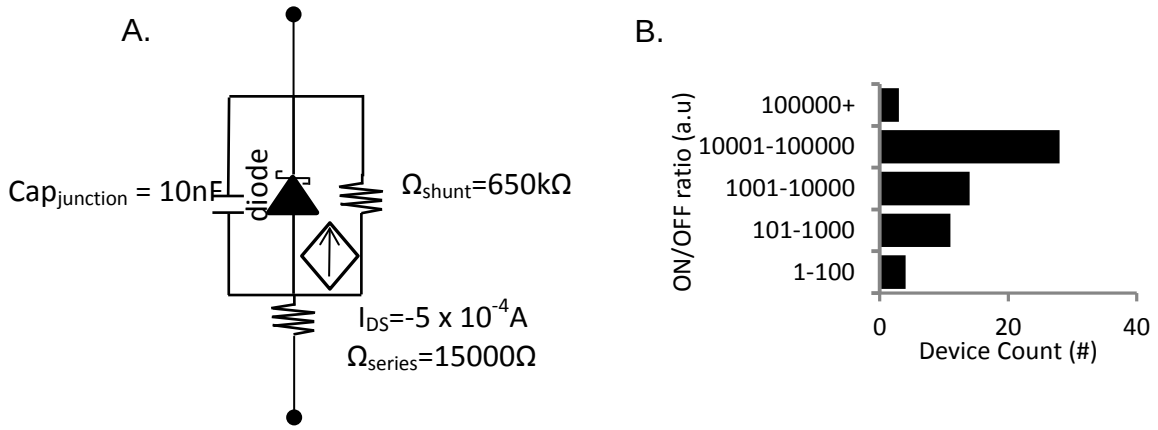

Figure 4.18. Statistical analysis of two terminal Schottky barrier batch processing. A. Statistically averaged device equivalent circuit. B. Bar graph showing the distribution of ON/OFF ratios over 50 devices.

The histogram plot of obtained rectification ratios over the 60 device sample is seen in Figure 4.18B. This distribution of reverse currents reduces the measured rectification ratio in devices and produces a distribution of rectification ratios. 31 out of 60 devices show a rectification in the order of 10^4- 10^5 with the highest recorded rectification measured to be 1.3 x 10^6 with 3 devices. 29 out of 60 devices showed a rectification of 10^4 or lower with 13 devices showing rectification less than 10^3. Lower rectification ratios are caused due to increases in reverse currents and are explained in the device equivalent circuit through the shunt resistance. Devices with high reverse currents possess low shunt resistance as discussed in Appendix B. The fabrication methodology leads to a device yield of 85%. 19% of total devices suffered from non-ideal operation; with 14% of total device exhibited short circuits, 4% inadequate contact and 1% poor operation.

4.7 Conclusions

Deposition of polymeric thin films on polycarbonate is seen to lead to environmental stress cracking of the substrate resulting in the loss of electrical continuity along the bottom electrode producing electrically isolated devices. A UV-NVS protective layer was introduced and allowed deposition of polymeric films out of chlorinated solvents on polycarbonate substrates. The UV-NVS protective layer produces a hydrophobic surface with favourable wetting with chlorinated solvent 1,2-dichlorobenzene providing an ideal layer for overcasting polymer thin films on polycarbonate.

The p-type semiconductor, P3HT was investigated for use with the substrate and the morphology characterised. Annealing temperature was seen to influence film roughness with reduced roughness under high anneal temperatures observed. Utilising a high resolution carbon nanotube conductive probe conductive mapping of the polymer surface show long range order in samples annealed at 150°C with regions of conductivity corresponding to locations of increased height with suspected conduction across the edge on lamellar structure of P3HT observed. Samples annealed at room temperature show a disordered morphology with the corresponding conductive map correlating with the disordered topography. The result is the highest resolution conductive mapping of P3HT to date showing conduction correlated with topographic features.

Top electrode metal choice and deposition method is seen to play a role in device short circuit yield with DC sputtering resulting in failure rates as high as 67% for gold sputtered electrodes, 49% for chromium compared to 43% for aluminium in manually aligned substrates. The yield of short circuited devices is seen to increase as electrode area increases for all metals with gold deposition showing the highest failure rate. Moving to an evaporation based electrode deposition reduced the failure rate for comparable discrete electrode and shared electrode substrates to 15% and 10% respectively for gold and aluminium. Evaporated aluminium is the best performing top electrode process due to the lower energy of evaporation deposition reducing metal diffusion and shorting throughout the device.

Evaporated aluminium top electrodes were used to fabricate Schottky barrier diode devices through the mismatch of work function at the aluminium/P3HT interface, creating a Schottky junction. Fabricated Schottky diode devices show time dependent performance, simulation of the equivalent circuit shows a shift in the internal series resistance, Ω_{series} from 125kΩ to 28kΩ over a 30 min period. These variations are described as a time varying resistive element in the equivalent circuit and hinder device characterisation. Devices fabricated with the same method and stored under vacuum for 20 hours show reduced forward current variation with a maximum shift in the internal series resistance, Ω_{series} from 20kΩ to 18kΩ. A statistical analysis of 60 devices resulted in a device yield of 85% with a forward mean current of 5.4×10^{-4} A over the range -1.28×10^{-4} A to 8.89×10^{-4} A with a mean reverse current of 4.78×10^{-7} A over the range 3.60×10^{-6} A to 1.29×10^{-9} A. A three magnitude range in reverse currents causes a wide distribution of rectification ratios negatively affecting device performance. Of the 60 devices, 19% of devices showed non-ideal operation with the majority being caused through a short circuit failure (14%). The result is the first reported polymeric devices fabricated on polycarbonate allowing the unique properties of plastic substrates to be employed in further processing.

References

1. Ye, Y., et al., *Transitions of morphological patterns of crystallizing polycarbonate in thin films.* Journal of Applied Polymer Science, 2012. **124**(1): p. 560-567.
2. Treadway, G., alchmst@vbbn.com, 2013. coating. [E-mail] Message to DG Gruszecki (alchmst@vbbn.com). Sent 14 April 13. Available at: 14 April 13 [Accessed 15 April 13].
3. Yuan, Y. and T.R. Lee, *Contact Angle and Wetting Properties*, in *Surface Science Techniques*, G. Bracco and B. Holst, Editors. 2013, Springer Berlin Heidelberg. p. 3-34.
4. Majewski, L.A., et al., *Influence of processing conditions on the stability of poly(3-hexylthiophene)-based field-effect transistors.* Applied Physics Letters, 2006. **88**(22): p. 222108.
5. Kline, R.J., et al., *Dependence of Regioregular Poly(3-hexylthiophene) Film Morphology and Field-Effect Mobility on Molecular Weight.* Macromolecules, 2005. **38**(8): p. 3312-3319.
6. Bielecka, U., et al., *Effect of solution aging on morphology and electrical characteristics of regioregular P3HT FETs fabricated by spin coating and spray coating.* Organic Electronics. **In Press, Uncorrected Proof**.
7. Tsao, H.N., et al., *The Influence of Morphology on High-Performance Polymer Field-Effect Transistors.* Advanced Materials, 2009. **21**(2): p. 209-212.
8. Chang, P.C., et al., *Film Morphology and Thin Film Transistor Performance of Solution-Processed Oligothiophenes.* Chemistry of Materials, 2004. **16**(23): p. 4783-4789.
9. Arif, M., et al., *Poly(3-hexylthiophene) crystalline nanoribbon network for organic field effect transistors.* Applied Physics Letters, 2010. **96**(24): p. 243304.
10. Dante, M., J. Peet, and T.-Q. Nguyen, *Nanoscale Charge Transport and Internal Structure of Bulk Heterojunction Conjugated Polymer/Fullerene Solar Cells by Scanning Probe Microscopy.* The Journal of Physical Chemistry C, 2008. **112**(18): p. 7241-7249.
11. Natali, D. and M. Caironi, *Charge Injection in Solution-Processed Organic Field-Effect Transistors: Physics, Models and Characterization Methods.* Advanced Materials, 2012: p. n/a-n/a.
12. Chu, C.-W., et al., *Control of the nanoscale crystallinity and phase separation in polymer solar cells.* Applied Physics Letters, 2008. **92**(10): p. -.
13. Yang, H., et al., *Effect of Mesoscale Crystalline Structure on the Field-Effect Mobility of Regioregular Poly(3-hexyl thiophene) in Thin-Film Transistors.* Advanced Functional Materials, 2005. **15**(4): p. 671-676.
14. Kamkar, D.A., et al., *Single Nanowire OPV Properties of a Fullerene-Capped P3HT Dyad Investigated Using Conductive and Photoconductive AFM.* ACS Nano, 2012. **6**(2): p. 1149-1157.
15. Ashley, D.S., et al., *Carbon nanotube modified probes for stable and high sensitivity conductive atomic force microscopy.* Nanotechnology, 2016. **27**(47): p. 475708.
16. Sittinger, V., et al., *Production of MF and DC-pulse sputtered anti-reflective/anti-static optical interference coatings using a large area in-line coater.* Thin Solid Films, 2006. **502**(1-2): p. 175-180.

17. Donnelly, V.M. and A. Kornblit, *Plasma etching: Yesterday, today, and tomorrow.* Journal of Vacuum Science & Technology A, 2013. **31**(5): p. -.
18. Fonash, S.J., S. Ashok, and R. Singh, *Effect of ion-beam sputter damage on Schottky barrier formation in silicon.* Applied Physics Letters, 1981. **39**(5): p. 423-425.
19. Wilcox, W.R. and T.J. LaChapelle, *Mechanism of Gold Diffusion into Silicon.* Journal of Applied Physics, 1964. **35**(1): p. 240-246.
20. Cole, D.H., et al., *Dynamic Properties of a Model Polymer/Metal Nanocomposite: Gold Particles in Poly(tert-butyl acrylate).* Macromolecules, 1999. **32**(3): p. 771-779.
21. Thran, A., et al., *Evidence of noble metal diffusion in polymers at room temperature and its retardation by a chromium barrier.* Applied Physics Letters, 2002. **81**(2): p. 244-246.
22. Sekitani, T., et al., *Suppression of DC bias stress-induced degradation of organic field-effect transistors using postannealing effects.* Applied Physics Letters, 2005. **87**(7): p. -.
23. J. D. McBrayer, R.M.S.a.T.W.S., *Diffusion of metals in silicon dioxide.* Journal of the Electrochemical Society, 1986. **133**(6).
24. Xu, Z., et al., *Vertical organic light emitting transistor.* Applied Physics Letters, 2007. **91**(9): p. 092911.
25. Ma, L. and Y. Yang, *Unique architecture and concept for high-performance organic transistors.* Applied Physics Letters, 2004. **85**(21): p. 5084-5086.
26. Yang, H., et al., *Graphene Barristor, a Triode Device with a Gate-Controlled Schottky Barrier.* Science, 2012. **336**(6085): p. 1140-1143.
27. Giulianini, M., et al., *Current-voltage characteristics of poly(3-hexylthiophene) diodes at room temperature.* Applied Physics Letters, 2009. **94**(8): p. 083302.
28. Jain, S.C., M. Willander, and V. Kumar, *Conducting Organic Materials and Devices*, in *Semiconductors and Semimetals*, M.W. S.C. Jain and V. Kumar, Editors. 2007, Elsevier. p. i-x, 1-188.
29. Lous, E.J., et al., *Formation of a Schottky barrier between eutectic Ga,In and thiophene oligomers.* Journal of Applied Physics, 1997. **81**(8): p. 3537-3542.

Chapter 5

5. Vertical Walled Architectures in Two Terminal Plastic Devices

Introduction

A methodology to introduce vertical wall architectures into device substrates is necessary in the fabrication of vertical walled devices. Previous work has shown the possibilities of laser processing,[1, 2] silicon etching,[3, 4] shadow masking,[5] photolithography and high throughput solid state embossing[6] to create vertical wall structure in device substrates. However, existing techniques are limited by material and substrate selection reducing the applications for fabricated devices. One approach that leverages the mechanical properties of polymers is mechanical cutting. Several mechanical cutting approaches including scalpel scoring, scissor cutting and CNC milling are investigated as high throughput methods for introducing vertical wall architecture. Furthermore, focussed ion beam (FIB) milling is examined as a methodology to introduce vertical wall device architecture.

In 2007 Krishnamurthy *et al.*[7] examined mechanical drilling of glass fibre reinforced polymeric films on glass substrates. Delamination was seen to occur in combination with lateral damage due to the thrust force excreted into the sample from the feed rate of the drilling action. Krishnamurthy *et al.*[7] further suggests thermal strain from these edge interactions can damage and further encourage edge delamination. The work of Krishnamurthy *et al.*[7] demonstrates the failure mechanisms of polymeric material under the forces exerted during mechanical cutting. Evaluating the lateral damage, delamination occurrences and resulting electrical properties across a device substrate will determine the feasibility of a selected methodology for incorporation in transistor fabrication.

5.1 Vertical Architecture Methodologies

The introduction of a vertical wall in vertical channel device substrates creates an exposed surface this allows for a functional interface across the polymeric channel when coupled with a functional film. Reducing lateral damage to the polymer channel and ensuring a cut edge capable of electrical continuity are essential to creating an optimised device. The adhesion between materials at this interface is governed by the strength of the bonding between the materials, physical interactions such as van der Waal's forces or columbic forces and the physical geometry of the interface.[8] Delamination of active materials is a major cause of device failure in electronics and electronics packaging.[9] Delamination is considered to be an adhesive failure if localised to the interface or cohesive failure if delamination occurs throughout the material a distance from the interface.[9, 10] The resulting roughness is a contributing factor in adhesion between successive layers and their interfaces.[11]Through the use of using scanning electron, optical and atomic force microscopy the morphology of the resulting vertical walls and morphological occurrences will be evaluated.

5.1.1 High Temperature Scalpel Cut Vertical Walls

Hot scalpel cutting of device substrates was investigated as a possible high throughput technology for the introduction of vertical wall architecture in device substrates. The cuts were carried out at temperatures near the glass transition temperature of polycarbonate (T_g ~150°C)[12] to reduce the mechanical hardness of the surface. Polycarbonate substrates with fabricated devices were heated on a hotplate at 150°C for one hour. The top surface of the substrate was measured to be 123.7°C by IR Thermometer. Prior to cutting scalpels were heated by immersion in silicon oil bath heated on a hotplate at 200°C. Heated polycarbonate substrates with fabricated devices were scored with the hot scalpel blade and the resulting cut topography investigated through optical and electron microscopy and can be seen in Figure 5.1.

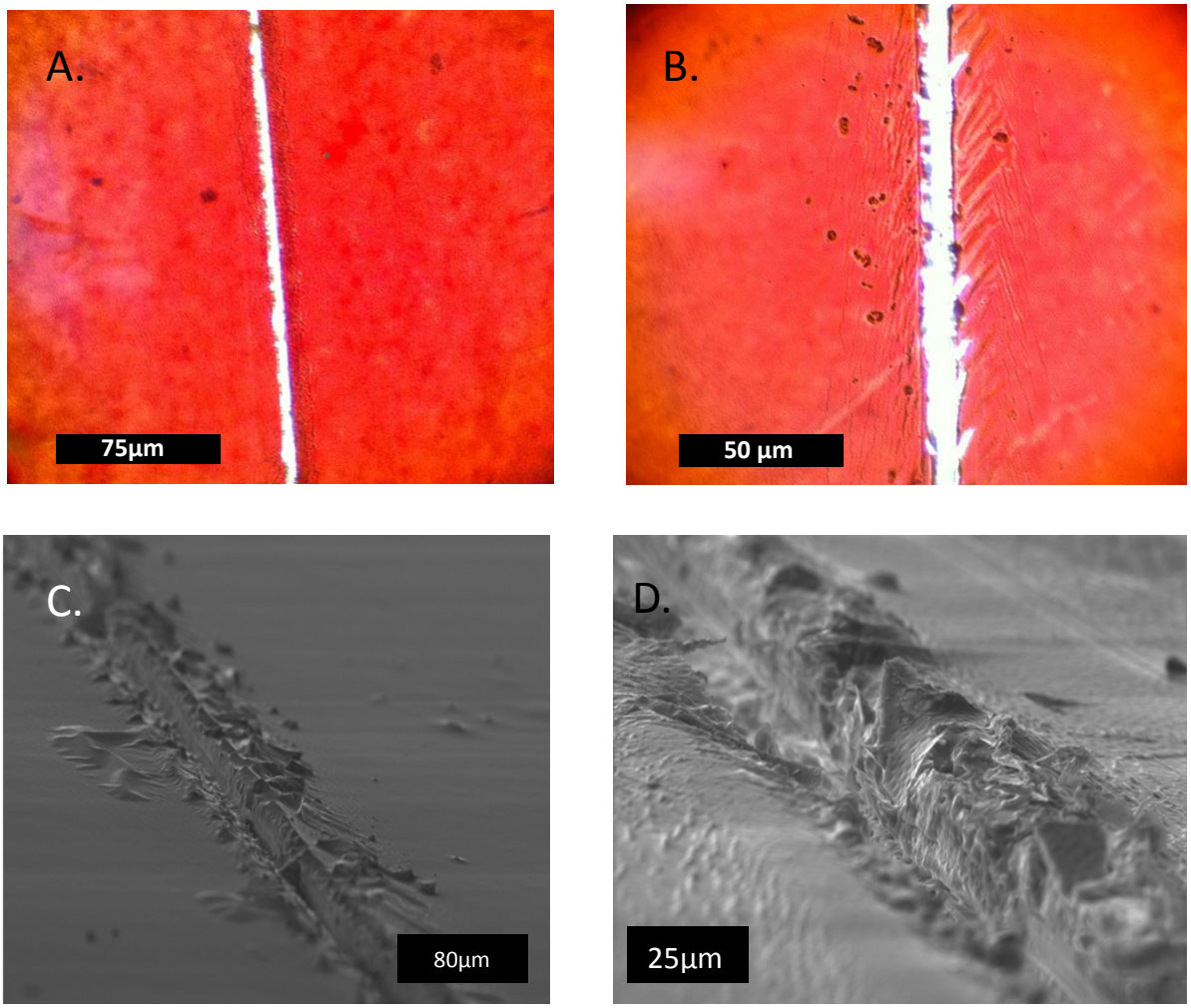

Figure 5.1.Optical and scanning electron microscope images of vertical wall architecture introduced by hot scalpel cutting. A. Optical microscope image of scalpel cut. B. Zoomed in optical microscope image of scalpel cut substrates. C. Scanning electron microscope image of hot scalpel cut. D. Zoomed in scanning electron microscope image showing the top interface of the cut surface and topographic features of the scalpel cut.

Scalpel scored substrates show a cut width of 5µm-10µm as shown in Figure 5.1A. The scalpel cut edge shows lateral damage on the order of 25µm from the cut which can be seen In Figure 5.1B. At the cut edge polymer can be seen to be removed, under scanning electron microscope (Figure 5.1C and D) polymer material at the surface of the cut can be seen to be lifted from the cut edge with areas of fragmented polymer being seen along the length of the cut. Along with this a deformation of the polymer can be seen in the zoomed in optical image and scanning electron image running the length of the cut on both edges. The

topography of the polymer and deformation of the surface can be seen in Figure 5.2.

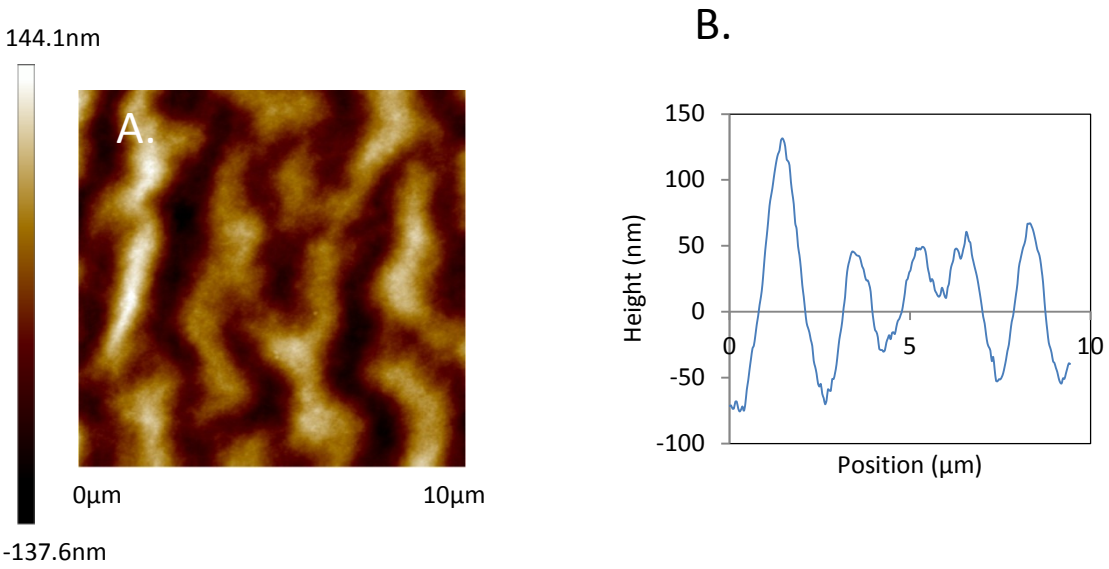

Figure 5.2.Film deformation from hot scalpel scoring of device substrates A. 10µm x10µm topographic height image of the polymeric deformation across the cut surface. B. Cross-section analysis of the topographic image.

The deformation across the surface shows a topographic surface with a height fluctuation with a cross section displacement range of 190nm. During the scalpel cutting action the movement of the blade creates a lateral force pulling and tearing the polymer material as it cuts through the material producing a cut edge with fragments of polymer delaminated at the cut edge and at a distance from the cut edge suggesting a cohesive delamination failure. Furthermore, the mechanical cutting action produces a cut without a clearly defined edge with the cutting action displacing material along the length of the cut.

5.1.2 Mechanically Cut Two Terminal Devices on PET Substrates

Two terminal devices were fabricated on flexible poly(ethylene terephthalate) (PET) substrates using an epoxy transfer method from a silicon template developed at Flinders University by Stapleton *et al.*[13] The transfer method allowed two terminal devices with gold communal source electrodes to be fabricated on the

flexible substrate as seen in Figure 5.3A. The device electrical properties and substrate yields along with a failure analysis are provided in Appendix D.1. PET substrates had vertical architectures introduced through the mechanical cutting of the device substrate by scissor cutting the susbtrates with desktop scissors. The resulting cut edge can be seen in Figure 5.3B.

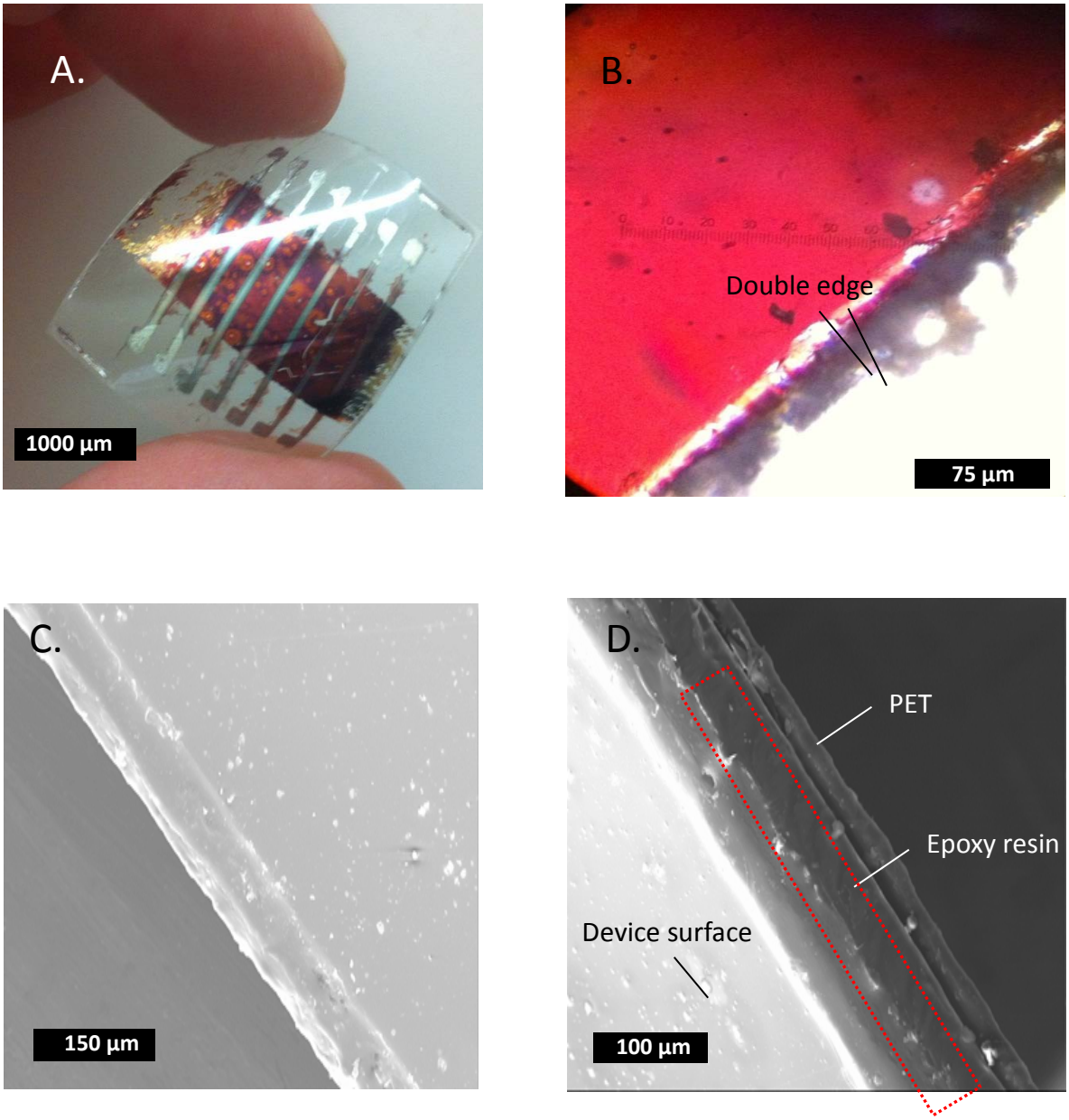

Figure 5.3. Mechanically cut two terminal devices on flexible PET substrates. A. Optical image of a two terminal device substrate on PET. B. Optical microscope image of the cut edge. C. Planar SEM of the cut surface. D. Cross section SEM of mechanical through PET.

Under optical microscope imaging the cut edge shows removed polymer up to 20µm from the cut edge. Down the length of the cut a double edge can be seen which is also seen in Figure 5.3C. The double edge may be due to bending of the

substrate during the cutting motion displacing the cutting blades relative to the substrate resulting in a cut edge which has had a non-uniform shear force applied over a larger area. The cross section of the surface can be seen in Figure 5.3D. The cross-section of the device substrate shows the PET substrate where it meets the epoxy resin and the cut cross section. The cross section shows an overlap in the epoxy resin (red square in Figure 5.3D) caused by the shear forces during cutting.

5.1.3 Focussed Ion Beam Milling

A Helios D433 Focussed Ion Beam (FIB) was used to mill a vertical wall in two terminal devices on polycarbonate substrate. The FIB technique uses a focussed beam of gallium ions to mill features with a spatial resolution of 5nm. The beam was used to cut an angled vertical wall into two terminal device substrates and monitored *in situ*. Figure 5.4 shows the application of focussed ion beam technology in the milling of two terminal devices and the resulting electrical properties of the substrate.

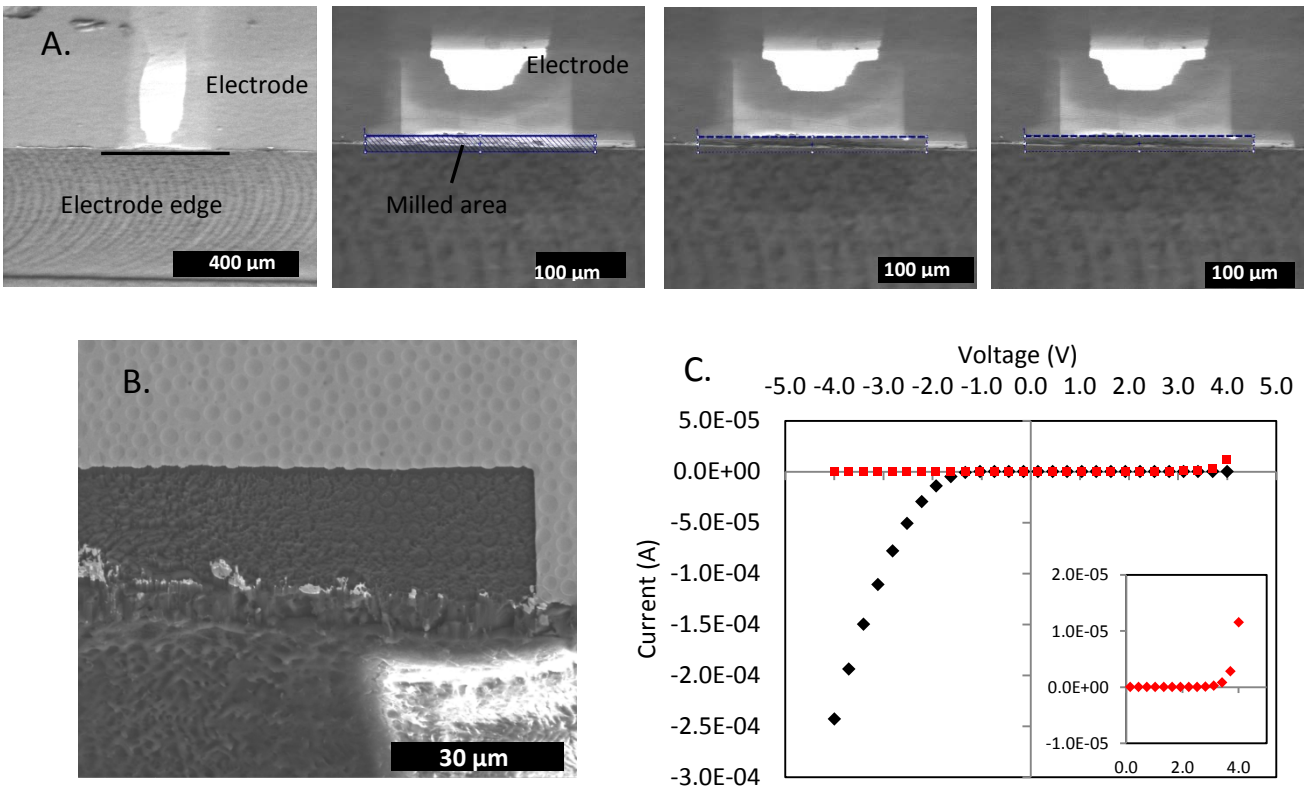

Figure 5.4. FIB milling of two terminal polycarbonate substrates. A. *In situ* monitoring of FIB milling procedure. B. SEM of resulting milled surface. C. Optical microscope image of completed device with epoxy gate electrode. D. Representative electrical characterisation of device substrates before (black line) and after (red line) FIB milling.

Figure 5.4A shows a two terminal device substrate with the electrode and electrode edge labelled. At the electrode edge the FIB was programmed to mill an area across the device (blue box Figure 5.4A) introducing a vertical wall with low lateral resolution and a high resolution programmable vertical wall seen in Figure 5.4B. During the milling procedure a significant change in electrical properties was observed across all devices on the substrate and can be seen in Figure 5.4C. Post FIB processing the two terminal Schottky devices show reduced forward currents on the order of 10^{-7}A and an increase of reverse currents with a current of 5 X 10^{-5}A measured at 4V. The result was observed in all devices processed and suggests significant degradation of the polymeric active layer attributed to the high energy process degrading chemical structure throughout the polymer. The significant loss of electrical performance suggests FIB milling of polymeric devices results in degraded devices with the majority of current produced via ionic conduction or electrons resulting from the degradation of the polymer matrix.

5.1.4 CNC Mechanically Cut Vertical Trench Walls.

A computer numerical controlled (CNC) A4 circuit board mill was used to introduce a trench through the middle of a device substrate. The sidewall in contact with the polymer channel is created through the angled face of 0.2mm tungsten carbide cutting tool which introduces an angled cut of 45° to the normal via a peripheral cut. The cutter operates through a mechanical spindle system with ball bearing stabilisation and can provide rotation speeds of up 40,000 revolutions per minute (RPM). Figure 5.5 shows two terminal device substrates with machine cut vertical walls.

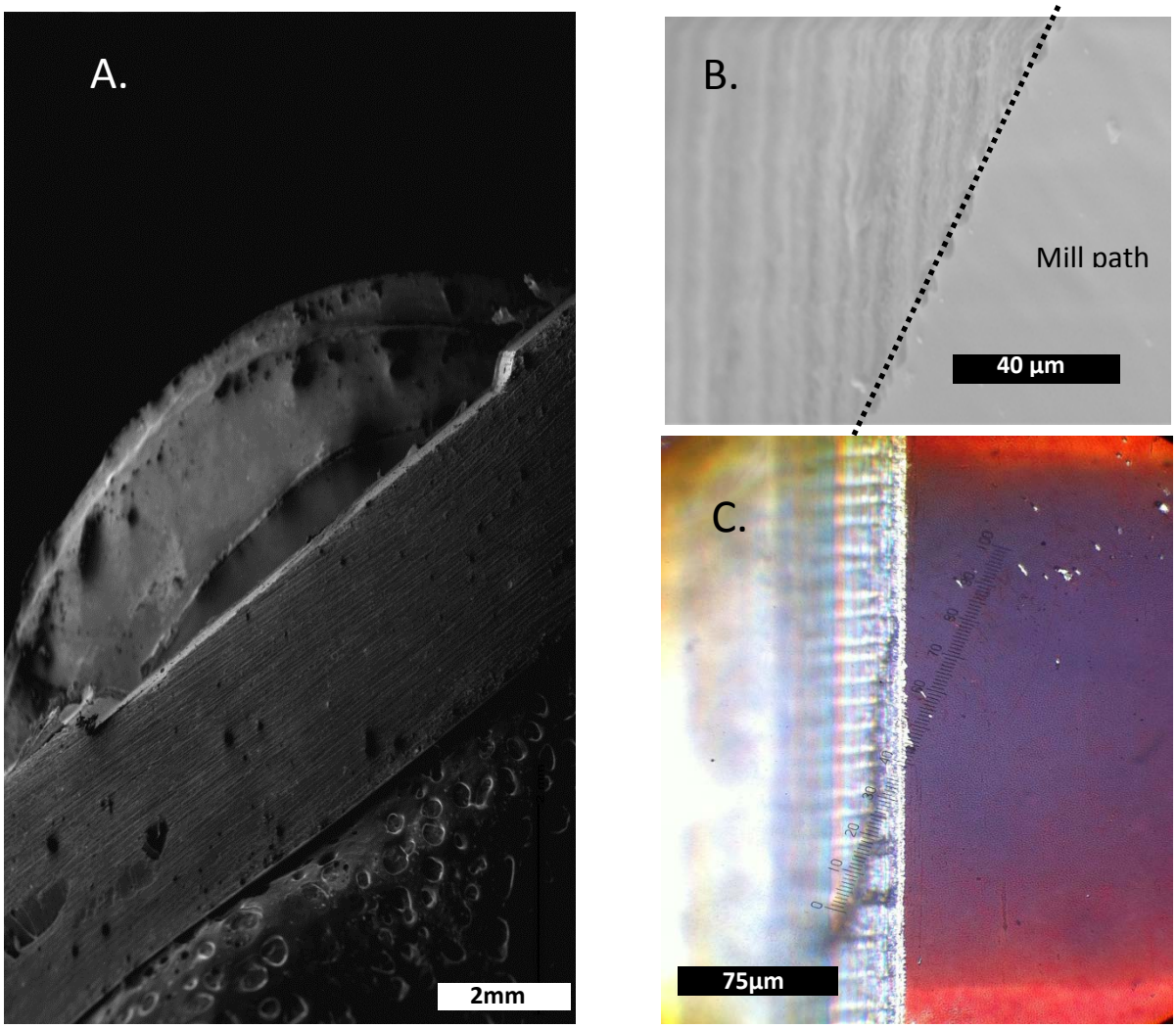

Figure 5.5. The introduction of a CNC machine cut vertical wall A. Two terminal devices prior to machine cut. B. Two terminal device after the machine cut process resulting in the introduction of a trench through the middle of the substrate and an angled vertical wall into the device.

Figure 5.5A shows a two terminal device substrate with a mechanically cut trench. Machine cutting of device susbstrates produces a trench depth of approx 500µm in the substrate. The cut edge can be seen in Figure 5.5B and an optical microscope image in Figure 5.5C. The cut edge shows reduced lateral damage at the cut edge in comparison to scalpel cut substrates and the scissor cut substrates. With lateral damage extending several microns for the cut edge but a clearlly formed cut is made through the substrate. In Figure 5.5B the periodic cutting action of the tool bit can be seeen along the lengeth of the cut resulting in a non uniform edge. The introduction of the cut edge was shown to have no influence on device yields. Due to the clearly defined edge, and angled surface allowing for favourable wetting and

solution procesing dynamics CNC machine cutting of two terminal device substrates was further investigated for the introduction of vertical walls into thin film stacks of polymer and metal.

5.2 Optimised CNC Mechanically Cut Two Terminal Devices for Vertical Transistors

A variable in this system is the cutting the speed at which the spindle head moves the cutter across the sample. Knowing the influence of the tracking speed on adhesion failures at the cut interface allows us to find an optimal spindle head speed to achieve an optimal interface. Adhesion failures between the polymeric film and the metal electrodes introduce changes to the device architecture from the ideal device cross section and are described in Figure 5.6. The deviations from idealised structure for P3HT- gold delamination is seen in Figure 5.6B and for gold-polycarbonate interface shown in Figure 5.6C. The result is an interface with varying morphology.

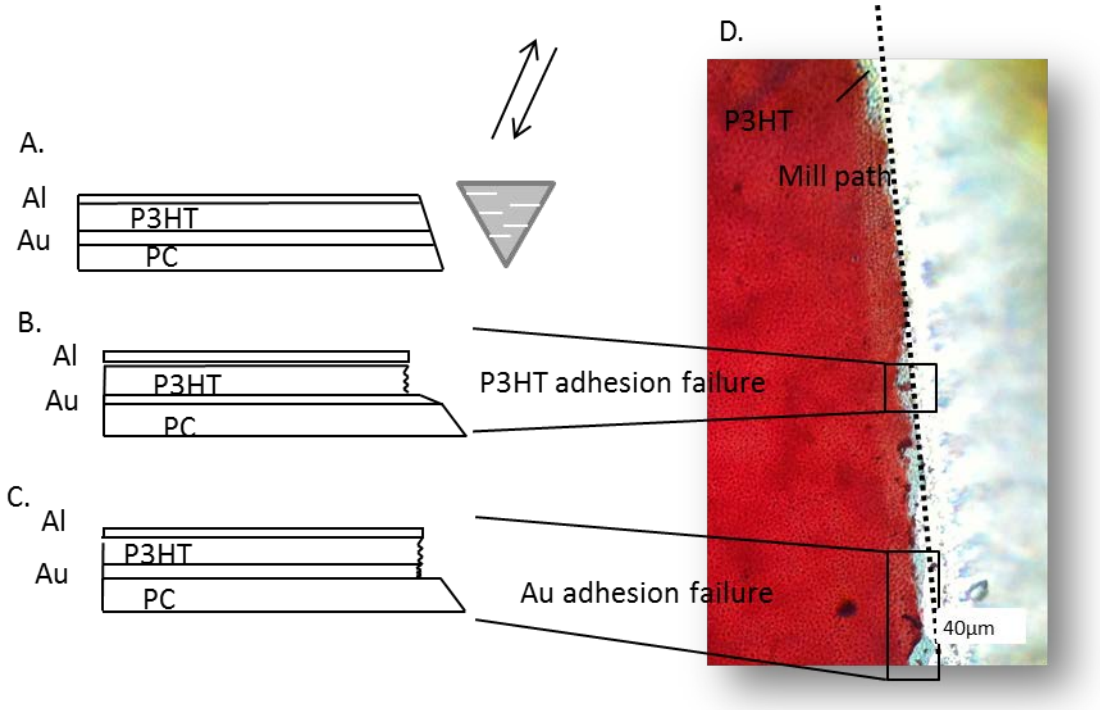

Figure 5.6. Delamination occurring during the CNC machine cutting of substrates. A. Idealised device structure B. Gold adhesion failure removing/stripping P3HT in the process C.P3HT adhesion failure and D. Optical microscope image showing a representative vertical cut with damage.

The speed of the cutter traversing across the surface is controlled through the programming interface and can be set between 5mm.s^{-1}- 20mm.s^{-1}. Finalised devices had vertical walls cut through the CNC circuit board mill. The linear cut velocity was measured to be 5m.s^{-1} and was used to produce a climbing cut (cutter speed direction in line with traversal speed direction). The cut interface at the edge of two terminal devices was investigated and adhesion failures measured to determine the quality of the cut edge at different spindle head tracking speeds.

5.2.1 Adhesion Failures with Respect to CNC Machine Cutting Parameters

Characterisation of adhesion failures was undertaken under optical microscope over four substrates with two terminal devices fabricated. A methodology for accurately surveying the cut was established by which a mill path was visualised through the substrate and locations with defects deviating from the mill path measured as either P3HT adhesion failure or gold adhesion failure. The methodology was able to characterise defects on the micron scale across the cut interface. The P3HT adhesion failures occurring per two terminal device is seen below in Figure 5.7 for four tracking speeds and the resulting averages and standard deviation.

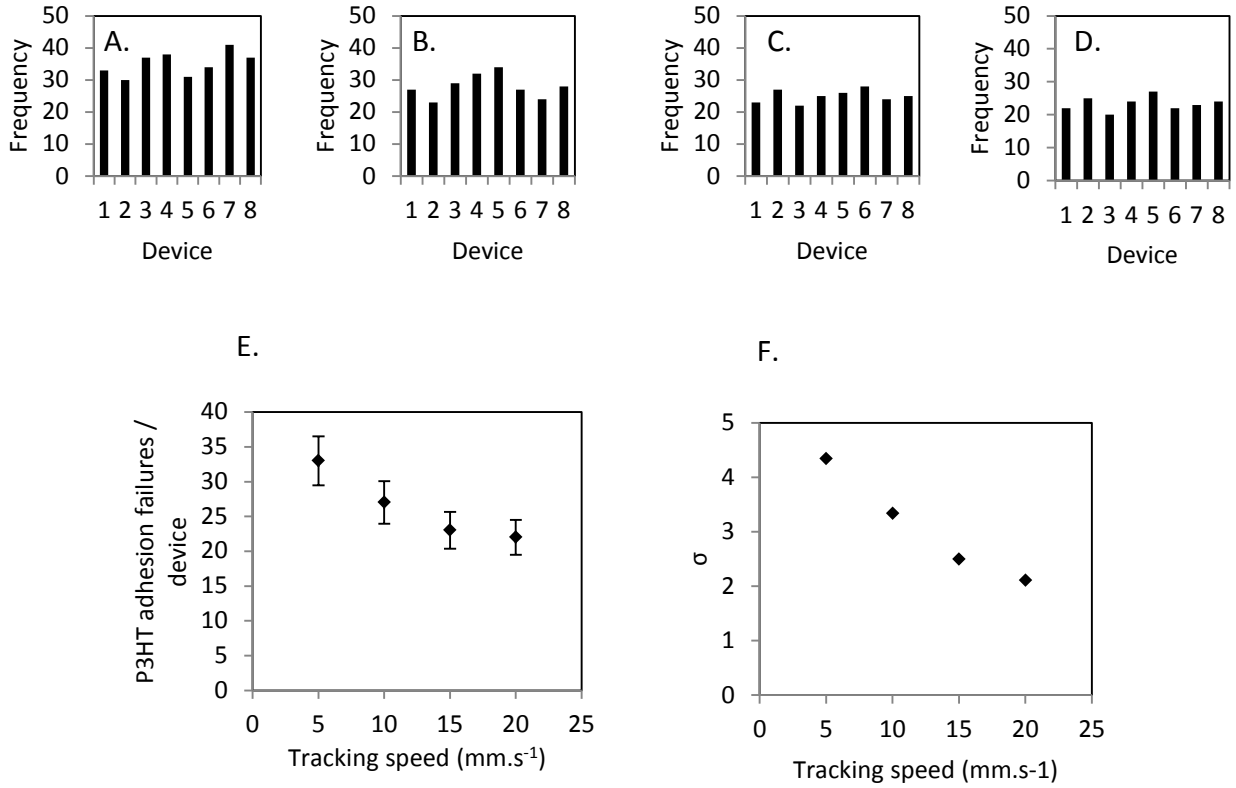

Figure 5.7.P3HT adhesion failures at the electrode-cut interface with respect to CNC circuit board spindle head tracking speed. A. P3HT delamination at 5mm.s^{-1} tracking speed. B. P3HT delamination at 10mm.s^{-1} tracking speed. C. P3HT delamination at 15mm.s^{-1} tracking speed. D. P3HT delamination at 20mm.s^{-1} tracking speed. E. Averaged delamination occurrences. Error bars represent the standard error corresponding to a 68% confidence interval. F. Measured standard deviation with respect to tracking speed.

P3HT adhesion failures were observed with 33 ± 3.6 occurrences at 5mm.s^{-1} compared to 22 ± 2.5 at 20mm.s^{-1} indicating faster translation speeds were desirable. The occurrences of P3HT adhesion failures at the cut edge are seen to increase as the spindle head tracking speed is reduced. Furthermore, the standard error appears to increase at slower tracking speeds suggesting not only greater P3HT adhesion occurrences but greater variability in the quality of the edge. Figure 5.8 shows gold adhesion occurring along the electrode edge with respect to spindle head tracking speed.

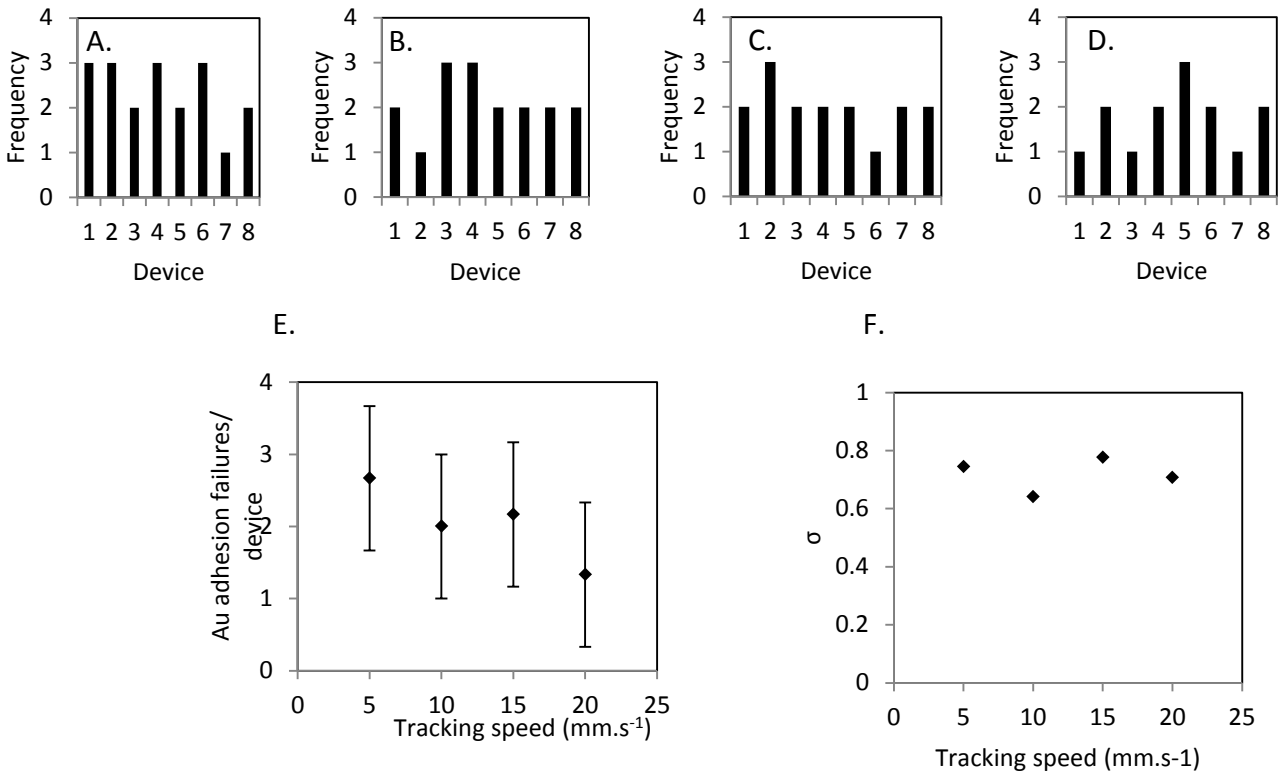

Figure 5.8. Gold adhesion failures at the electrode-cut interface with respect to CNC circuit board spindle head tracking speed. A. Gold delamination at 5mm.s^{-1} tracking speed. B. Gold delamination at 10mm.s^{-1} tracking speed. C. Gold delamination at 15mm.s^{-1} tracking speed. D. Gold delamination at 20mm.s^{-1} tracking speed. E. Averaged delamination occurrences. Error bars represent the standard error corresponding to a 68% confidence interval. F. Measured standard deviation with respect to tracking speed.

Across spindle head tracking speeds 5mm.s^{-1}- 20mm.s^{-1} gold adhesion failures were measured for each device. Gold adhesion failures were observed with 2.7 ± 1.1 occurrences at 5mm.s^{-1} compared to 1.3 ± 1.2 occurrences at 20mm.s^{-1}. Gold adhesion occurrences were greater at lower spindle head speeds compared to higher spindle head tracking speeds showing the same behaviour as P3HT adhesion failures. The ratio of the Au: P3HT adhesion occurrences are shown below in Figure 5.9.

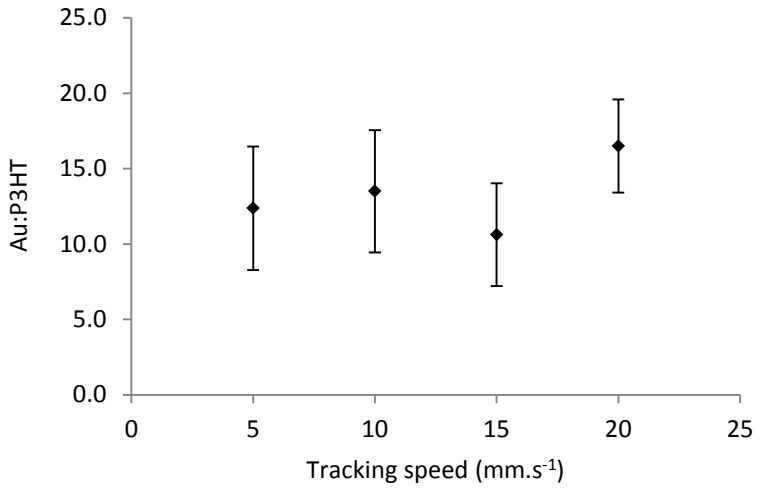

Figure 5.9. Gold adhesion failures at the electrode-cut interface with respect to CNC circuit board spindle head tracking speed. Error bars represent the standard error corresponding to a 68% confidence interval.

The ratio measures the amount of P3HT adhesion failures with respect to gold adhesion failures at a specific spindle head speed. A ratio of 12.4 ± 4.5 at 5mm.s^{-1}, 13.5 ± 4.4 at 10mm.s^{-1}, 10.6 ± 3.4 at 15mm.s^{-1} and 16.5 ± 3.5 at 20mm.s^{-1} were calculated from experimental data. This suggests no correlation between tracking speed and the adhesion failure mode with respect to one another. When introducing a lateral cut using a CNC mechanical mill faster spindle head tracking is seen to reduce adhesion failures. At slower tracking speeds higher occurrences of adhesion failure are observed which are attributed to greater edge interactions. At slower tracking speeds it is likely that deflection of drill point as it cuts across the sample may introduce additional perpendicular force across the cut further encouraging delamination in comparison to faster spindle head tracking speeds.[7]

5.2.2 Investigating adhesion failure through AFM

An understanding into the electrical properties at the cut interface through conductive mapping of the device surface allows critical insight on the resulting interface and device feasibility. With lateral forces causing the adhesion failures between the P3HT and gold located on the device substrate. The extent of the damage on the electrical properties can be characterised via conductive AFM. Conductive microscopy was performed in a moisture filtered ambient atmosphere

at 26°C. Optical microscope was used to identify a location *in situ* at the cut interface to be the imaging location. Figure 5.10A shows an experimental schematic with applied biases for conductive mode operation B. Shows the AFM tapping mode height image and C. A three-dimensional render of the topographic height image compiled through the Nanoscope V software suite taken at the cut interface.

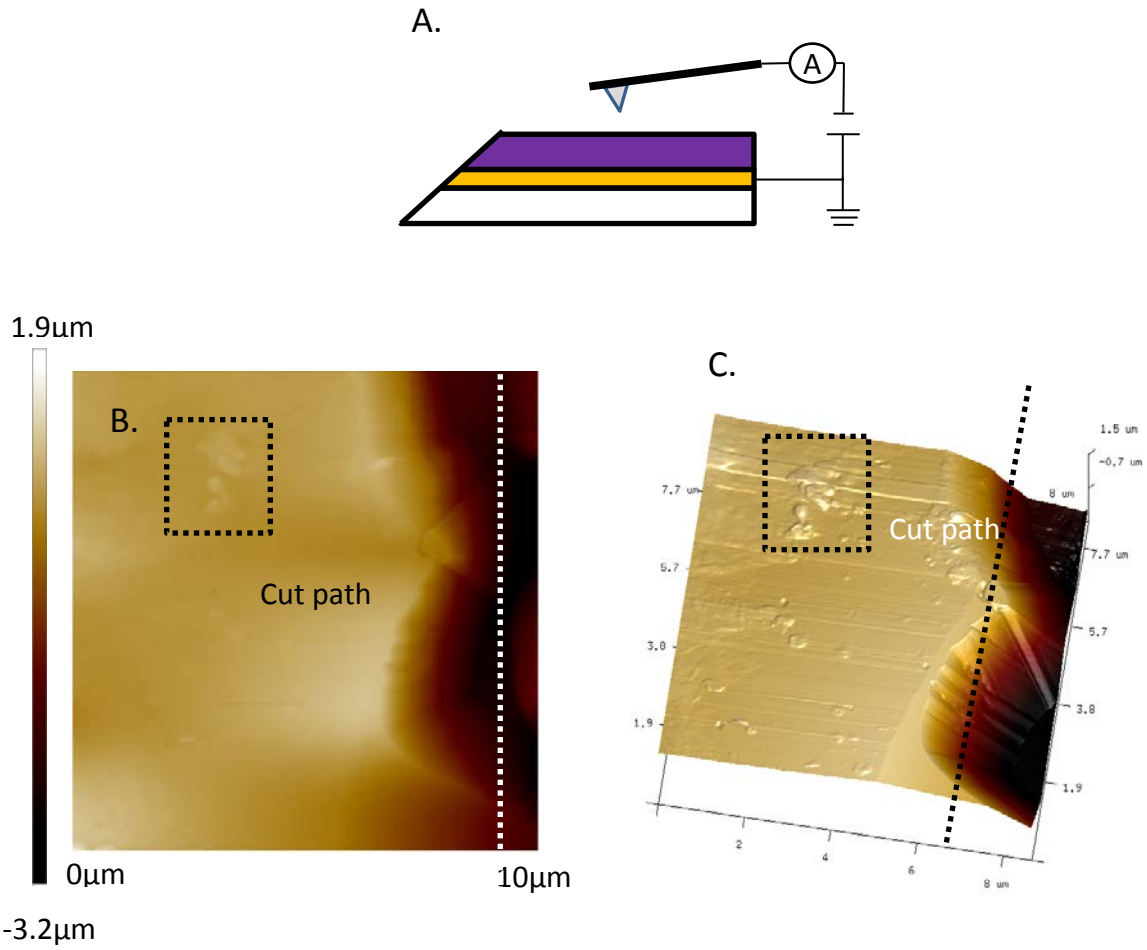

Figure 5.10 . Obtained topographic images of the cut edge A. Experimental schematic showing biases applied. B.10µm x 10µm AFM tapping mode height image of the cut-polymer interface. C. Three-dimensional topographic image of the tapping mode two dimensional image.

The cut path (labelled in Figure 5.10) has a periodicity involved in the tracking through the material due to the cutter action with undulations from the cut path of 2µm. In the topographic image the possible polymeric edge can be seen receded from the cut interface along with a region of possible polymeric or environmental debris (the square box in Figure 5.10) caused from the cutting process. The corresponding peak current image is presented below in Figure 5.11. Figure 5.11B

shows a rotated three dimensional render of the superimposed peak current map on the three dimensional topographic image. The height and conductive images are acquired concurrently and ensure 1:1 registration between the images over the examined area.

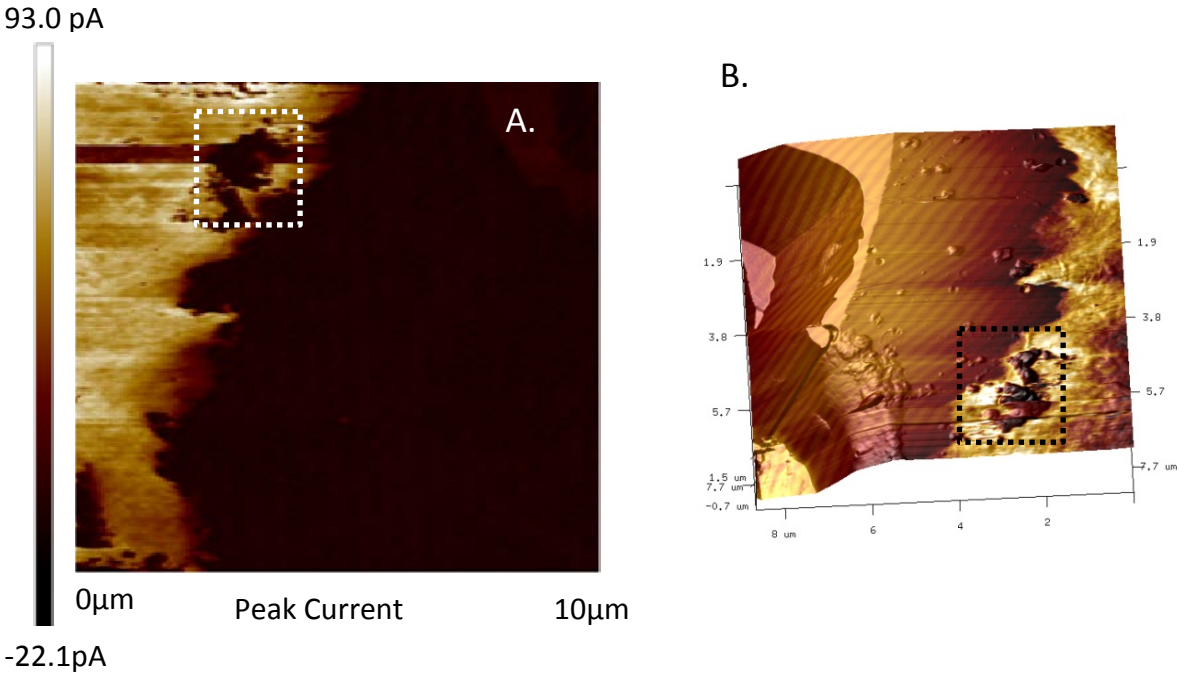

Figure 5.11. Conductive AFM conductive map and corresponding 3D render of the cut edge A. 10µm x 10µm AFM peak current image. B. Rotated three dimensional render of the topographic height image with superimposed peak current map.

The peak current map in Figure 5.11 shows regions of conductivity up to 93.0 pA at 4V tip bias over the area with the uniform conductive region believed to be P3HT polymeric material. The conductive region has clearly defined edges with a drop in peak current occurring at the edge of the conductive region to -20pA. No other electrical contrast is observed in the image suggesting the underlying gold electrode is not exposed at any point on the imaged surface. A labelled region of potentially polymeric or environmental debris (as seen in Figure 5.11B) shows no conduction through the area with the defect region aligning with the topographical image defect. Figure 5.12A shows the obtained topographic 2D image and Figure 5.12B the peak current map localised on the location of the debris and conductive region edge.

Figure 5.12A shows a local height maximum at the location of the debris and the corresponding peak current map in Figure 5.12B no peak current through the debris and the area immediately surrounding the debris. This could be the result of the cantilever failing to come into feedback with the surface due to the height differential between the local height maxima and the surrounding environment or an insulating piece of debris.

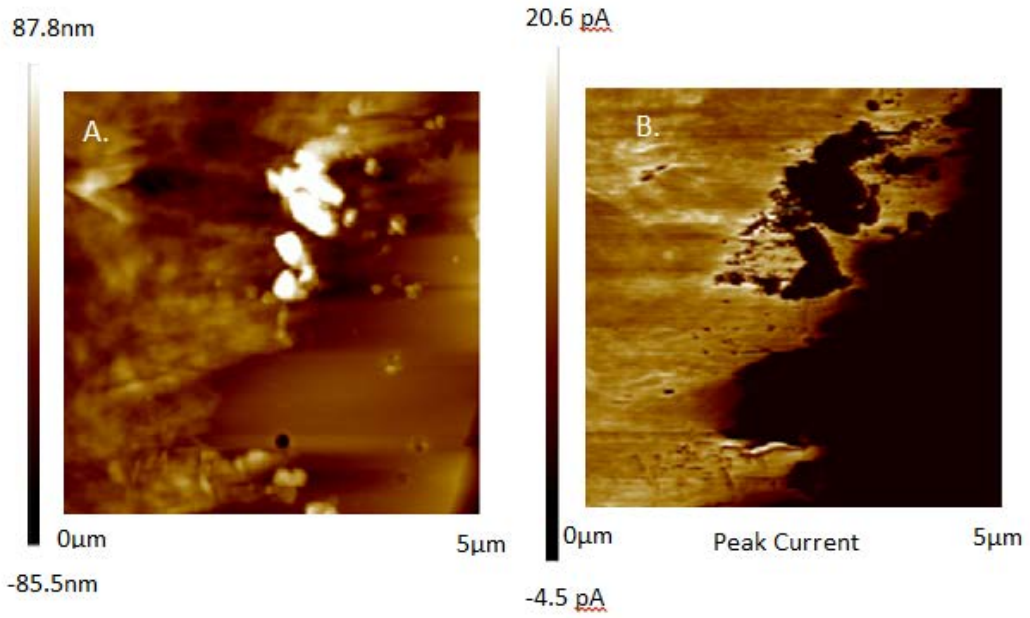

Figure 5.12. Conductive AFM conductive map A.10µm x 10µm peak current image B.5µm x 5µm AFM peak current image.

Peak current is observed consistently across the polymer matter on the sample with small observable locations of no observable peak current throughout the bulk of the material. Removal of polymer and underlying gold can be seen to occur from the cutting process on the order of micron from the cutting interface that was not observable due to the resolution of the optical microscope. Peak current can be observed through to the polymeric edge showing similar currents to locations within the bulk. The result suggests no damage to the electrical properties at the polymer edge occur due to the cutting process and the thermal energy involved. Small local areas on the order of nanometres show regions of no observable conductivity in comparison to the bulk conductivity. The cutting process appears to largely maintain the electronic integrity of the polymeric material. The

consequences of this interface on the resulting three terminal device performances will be probed further in subsequent chapters.

5.3 Conclusion

Two terminal device substrates had vertical wall structures introduced through several scalable technologies. With the resulting morphology of the vertical wall assessed for viability in producing an effective interface in a transistor device.

Hot scalpel cutting of the substrate near the glass transition temperature of the polycarbonate substrate resulted in a vertical wall with significant lateral damage on the order of 25µm. The cutting action of the scalpel introduces tearing of the polymeric film with displaced material producing a cut edge that is poorly defined. Scalpel cuts produce a poorly defined edge with significant delamination that would make the deposition of a functional film unlikely without significant optimisation.

Two terminal devices were fabricated and characterised on PET flexible substrate and had a vertical wall structure introduced through a scissor cut. The scissor shows a prominent double edge with lateral damage along the length of the cut on the order of 20µm. The cutting action is suggested to result in a double edge as the flexible substrate is cut with the blades being displaced relative to the substrate producing a double edge. The result is a cut surface with significant damage and an unknown structure at the cut edge.

Focussed Ion Beam milling was investigated and produced a clear edge with a well-defined surface with no observable lateral damage. However exposure to the procedure produced significant degradation in device performance.

CNC machining cutting of polycarbonate substrates showed machine cut lateral damage on the order of microns. An angled cut edge was produced allowing for favourable wetting dynamics for spin casting with a defined that had reduced topography defects in comparison to scissor and scalpel cut methods. The cut was optimised to reduce adhesion failure through optical microscope characterisation of adhesion failures with respect to the spindle head speed. Conductive AFM mapping

at the operational edge at the cut interface shows consistent electrical conductivity across the identified polymeric layer on the order of 90pA. Across the polymeric interface the continuity of electrical properties is seen to remain through to the edge of the polymeric material. During cutting, the polymeric thin film is torn with micron scale lateral ripping in devices suggesting a non-ideal device structure resulting from the mechanical cutting procedure. The results shows mechanical cutting could potentially be used in the introduction of vertical walls in transistor structures.

References

1. Parashkov, R., et al., *Organic vertical-channel transistors structured using excimer laser.* Applied Physics Letters, 2004. **85**(23): p. 5751-5753.
2. Kim, D., et al., *Holography and plasma oxidation for uniform nanoscale two dimensional channel formation of vertical organic field-effect transistors with suppressed gate leakage current.* Organic Electronics, 2011. **12**(11): p. 1841-1845.
3. Chen, Y. and I. Shih, *Fabrication of vertical channel top contact organic thin film transistors.* Organic Electronics, 2007. **8**(6): p. 655-661.
4. Khan, A.R., J. Siddique, and S.S.K. Iyer. *Advanced technique of vertical organic thin film transistor*. in *Multimedia, Signal Processing and Communication Technologies (IMPACT), 2013 International Conference on*. 2013.
5. Rossi, L., et al., *Low voltage vertical organic field-effect transistor with polyvinyl alcohol as gate insulator.* Journal of Applied Physics, 2011. **110**(9): p. 094508.
6. Stutzmann, N., R.H. Friend, and H. Sirringhaus, *Self-Aligned, Vertical-Channel, Polymer Field-Effect Transistors.* Science, 2003. **299**(5614): p. 1881-1884.
7. Velayudham, A. and R. Krishnamurthy, *Effect of point geometry and their influence on thrust and delamination in drilling of polymeric composites.* Journal of Materials Processing Technology, 2007. **185**(1–3): p. 204-209.
8. Altazin, S., et al., *Analytical modeling of the contact resistance in top gate/bottom contacts organic thin film transistors.* Organic Electronics. **In Press, Uncorrected Proof**.
9. Zhang, G.Q.D.W.D.F.X.J. *Mechanics of Microelectronics*. 2006.
10. Venables, J.D., *Adhesion and durability of metal-polymer bonds.* Journal of Materials Science, 1984. **19**(8): p. 2431-2453.
11. Yao, Q. and J. Qu, *Interfacial Versus Cohesive Failure on Polymer-Metal Interfaces in Electronic Packaging—Effects of Interface Roughness.* Journal of Electronic Packaging, 2002. **124**(2): p. 127-134.
12. Lide, D.R., *CRC handbook of chemistry and physics*. Vol. 85. 2004: CRC press.
13. Stapleton, A.J., et al., *Pathway to high throughput, low cost indium-free transparent electrodes.* Journal of Materials Chemistry A, 2015. **3**(26): p. 13892-13899.

Chapter 6

6. Fabrication of Vertical Transistors Featuring Solution Processed Dielectrics

Introduction

Traditional methodologies for incorporation of dielectric films in planar device structures include thermally grown SiO_2,[1], chemical vapour deposition techniques[2, 3] monolayer self-assembly[4], sputtering[5, 6] and anodization[7] of thin films. Vertical transistors represent a unique challenge in depositing a dielectric film due to the topography associated with vertical wall architectures. To date, transistors incorporating vertical walls have has dielectric films deposited using PECVD[8, 9] resulting in a conformal film across a multi-phase vertical wall topography. These depositions often take place under high temperatures limiting substrate selection and have a high associated cost.

One possible solution for film deposition in vertical wall transistors is solution processing of functional materials. Solution processed polymers have shown the ability to be cast[10], printed[11] and surface polymerised [12] in device structures. Solution processed films offer novel processing conditions allowing deposition at room temperature and compatibility with scalable printing technologies. Leveraging the benefits of solution processing to produce conformal dielectric films is an important step in the development of polymeric vertical transistors. Understanding the resulting morphology of the dielectric film across the vertical wall and associated electrical performance are key obstacles in producing a scalable vertical transistor platform.

6.1 Deposition of Dielectric Functional Material

6.1.1 Strategy

A machine cut vertical wall has been studied and has shown electrical continuity across the device operational area towards the cut edge (see §5.2). A device structure whereby a machine cut wall creates an interface allowing for a potential vertical transistor is presented in Figure 6.1. Key to the operation is a functional material applied across the substrate over the machine cut seen in Figure 6.1B. Over the deposited functional material a silver epoxy electrode is deposited manually creating a third terminal to apply a potential voltage between the gate and source and can be seen in Figure 6.1C.

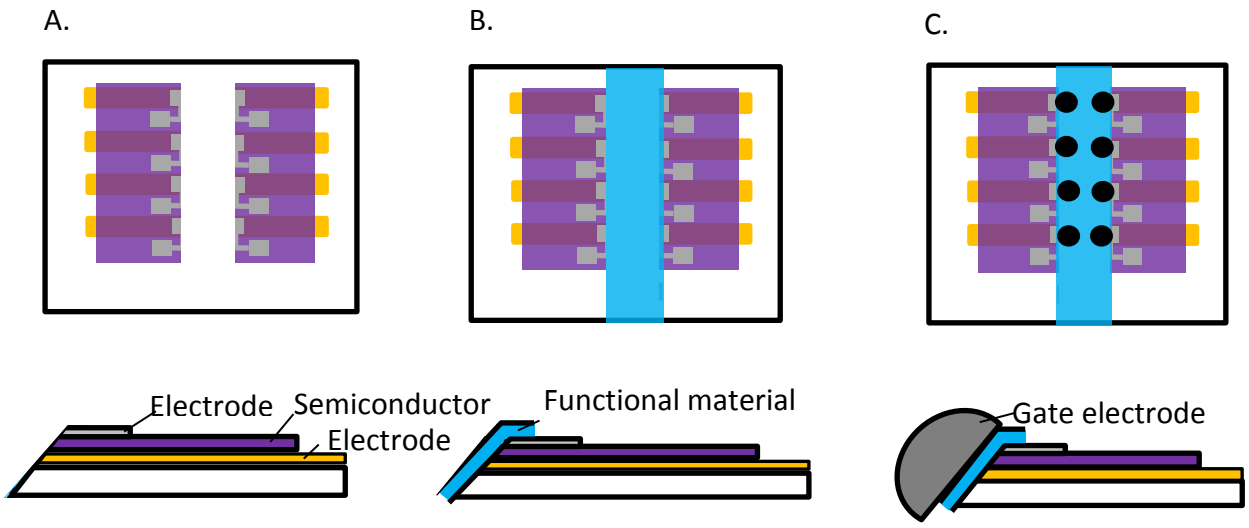

Figure 6.1. Top view and side view schematic describing deposition of dielectric material towards a three terminal device work flow. A. Cutting of two terminal device substrates. B. Dielectric film deposition. C. Gate epoxy electrode deposition.

Effective capacitive coupling between the semiconductor and dielectric material allows for the enhancement or depletion of the conductive channel between the source and drain. A well performing dielectric possesses a large dielectric constant, κ and provides low dielectric loss under AC signal. A high breakdown voltage is desirable and determines the operating voltages of the resulting device. [9, 13, 14]

Increasing the capacitance of the dielectric film has been shown to improve device performance of an OFET with high capacitance dielectrics increasing the lateral electric field at the semiconductor-dielectric interface at a given voltage. Another approach to increasing the capacitance of dielectric films is scaling to reduce dielectric film thickness.[9, 15]As a capacitive film is scaled to smaller lengths greater capacitance is needed to store the same charge area. With equivalent devices scaling of the thickness of the functional material will reduce power consumption and increase the magnitude of the lateral electric field at equivalent applied potential voltage and device dimension. The scaling properties of several solution processable dielectric films were probed for use in the device structure.

6.1.2 Solution Processable Dielectric Materials

The feasibility of solution processing dielectric functional materials for use on two terminal device substrates with a machine cut vertical wall cut was investigated. Two electrode configurations gold-aluminium source-drain and gold-gold source-drain electrode devices were fabricated and used to study several solution processed dielectrics. Symmetric gold electrode devices with a machine cut vertical wall as seen in Figure 6.2A and an asymmetric gold source and aluminium drain machine cut two terminal device as shown in Figure 6.2B.

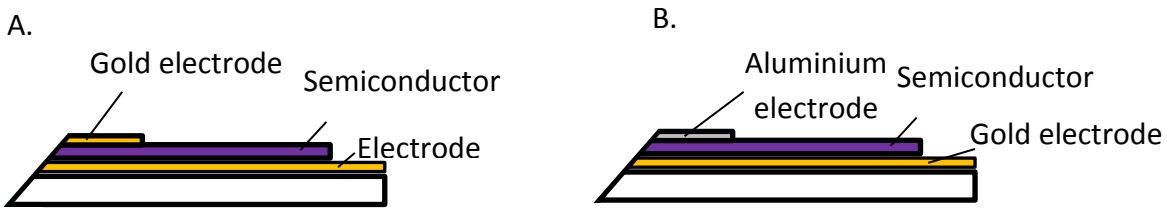

Figure 6.2.Cross section schematic of two terminal devices with different electrode configurations. A. Asymmetric electrode configuration with gold source electrode and aluminium drain electrode. B. Symmetric electrode configuration with gold source and drain electrode.

Two terminal device substrates with processed dielectric functional films had an epoxy gate electrode applied manually seen in Figure 6.3. The epoxy was applied using optical microscope to create a third contact over the spin coated vertical wall. The two terminal device substrates with gate epoxy applied gate electrodes were

then heat annealed at 100°C for 30mins. The completed devices were probed through the use of a Fluke multimeter. An experimental schematic showing the failure testing of dielectric functional material films between the gate-source and gate-drain electrodes through the use of a multimeter is seen in Figure 6.3.

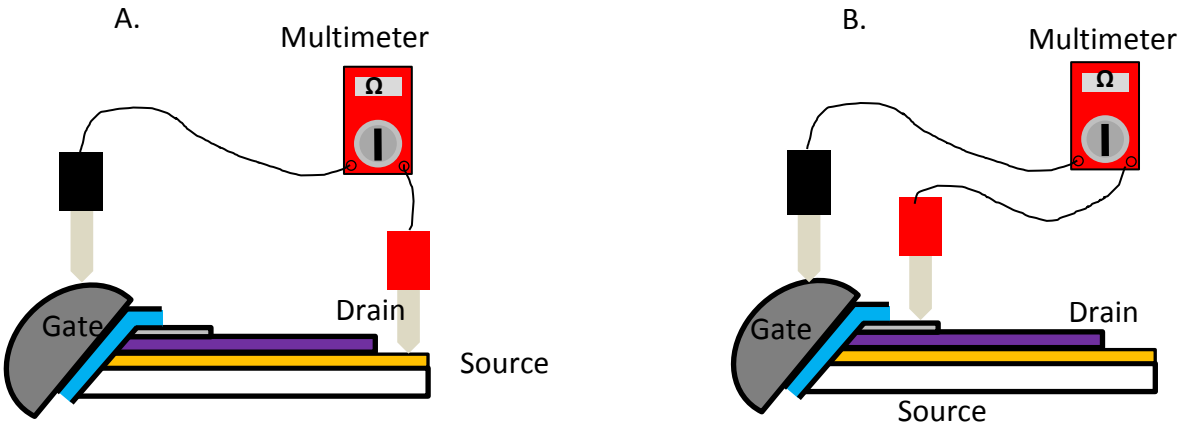

Figure 6.3. Failure analysis for three terminal devices A. Gate-source failure testing. B. Gate-drain failure testing.

Failure analysis was conducted by observing the resistance in the gate-source and gate-drain circuit. Measurements that showed a short circuit between gate-source or gate-drain were considered a failure. This procedure was carried out across all devices on all substrates tested. Functional materials were spin coated with spin speeds in the range 1000RPM-3000RPM. At each spin speed three device substrates were fabricated with a failure analysis conducted across all 16 devices on the substrate and catalogued as seen in Table 6.1.

Table 6.1. Failure rates for spun cast dielectric functional materials over symmetric and asymmetric electrode device configurations.

	Gold-gold failure rate (%)			*Gold-aluminium failure rate(%)*		
Material	1000RPM	2000RPM	3000RPM	1000RPM	2000RPM	3000RPM
UV-NVS	60	85	100	20	60	100
Cytop	45	80	100	20	50	100
PMMA	100	100	100	85	100	100
$LiClO_4$: PEO	100	100	100	100	100	100

At 3000RPM spin speed both device configurations had a failure rate of 100% for all dielectrics processed. The rate of failure for cytop solution processing was calculated to be 45% for symmetric electrode devices and 20% for asymmetric electrode devices at 1000RPM. Increasing the spin speed to 2000RPM the failure rate for cytop solution processing was calculated at 80% and 50% respectively. Devices with a top gold electrode show higher rates of failure than aluminium top electrode device. This is potentially due to the native oxide on the aluminium electrode improving the wetting of films across the top electrode. UV-NVS and cytop both show the ability to be spin coated and produce electrically insulating films across the machine cut surface. Due to its ability to be processed at room temperature and low failure rate in gold-aluminium electrode devices UV-NVS is considered a promising candidate for use in vertical transistor devices. The morphology and electrical properties of the resulting UV-NVS film were studied in order to further study the dielectric material for use in machine cut devices.

6.2 UV-NVS Dielectric Material

UV-NVS (Ultra Optics) UV cured resin was selected as a dielectric layer because it can be cured at room temperature, and was seen to produce insulating films across the cut surface at 1000rpm. UV-NVS is a multiphase optics coating incorporated into a PMMA polymer matrix.[16]PMMA is a dielectric material with a reported dielectric constant, $\kappa = 2.6$ that has been used in field effect transistor devices.[17, 18] A two terminal UV-NVS resistor cell was fabricated featuring a 10µm UV-NVS film and gold electrodes was electrically characterised and can be seen in Figure 6.4. UV-NVS resistor cells were shown to produce -5.8×10^{-8}A at ±4V and a resistance $\Omega =$ 100MΩ resulting in a conductivity $\sigma = 1 \times 10^{-8}$ S.m^{-1} for the UV-NVS film indicative of an insulating material.

UV-NVS films were incorporated into transistor structures through solution processing directly onto two terminal device substrates. The gate-source current was measured for a completed three terminal device featuring an epoxy electrode and can be seen in Figure 6.4B. Three terminal devices with UV-NVS solution processed dielectric films show leakage currents on the order of 10^{-6}A-10^{-7}A over

the range ±4V when tested without a bias across the third terminal. Gate to source leakage was measured at -2 x 10^{-7}A at -4V and a resistance Ω_{GS}=167MΩ extracted. Gate-drain leakage was measured at 2 x 10^{-6} A at -4V and a resistance Ω_{GD}=17MΩ extracted and seen in 6.4C. In comparison, the reduced Ω_{GD} is likely attributed to an increase overlap between the drain electrode and deposited gate epoxy, increasing the electrode surface area and reducing the resulting resistance.

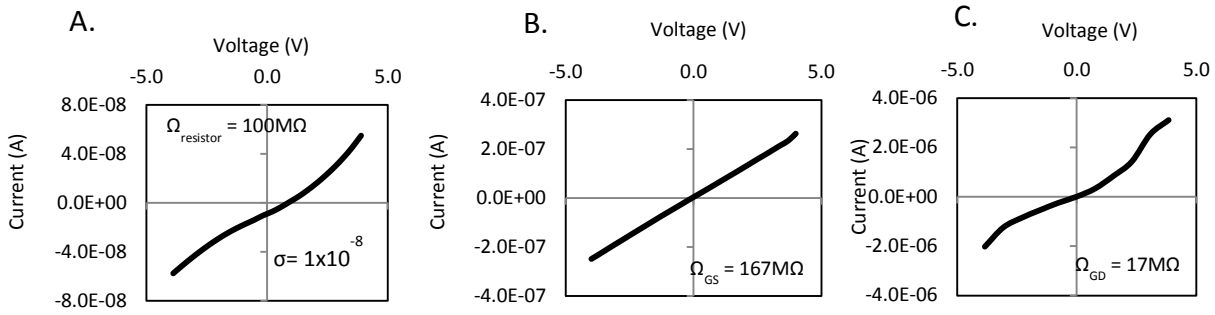

Figure 6.4. UV-NVS resistance measurements taken from leakage current-voltage characteristics for epoxy gated three terminal devices with UV-NVS spin coated dielectric material. Devices are an average compiled over 10 devices on 3 substrates. A. Current-voltage characteristic for a two terminal UV-NVS resistor cell. B. Gate-source leakage current. C. Gate- drain leakage current.

In order for device operation the resistance of the gate-source and gate-drain circuits need to be higher than the source-drain circuit providing an electrically conductive path between the injected charges at the source to conduct to the drain producing a measurable forward current. The measured Ω_{series} of fabricated two terminal devices has previously been shown to be on the order kΩ for thin film devices (as seen in §4.3) and provides a source-drain circuit at lower resistance than either gate circuits. UV-NVS films produce an electrically insulating surface with sufficient resistance to be electrically isolating for vertical transistors. The morphology of the surface was investigated through microscopy to observe the uniformity of the coating. Figure 6.5 shows the morphology of a completed UV-NVS spin coated device substrate.

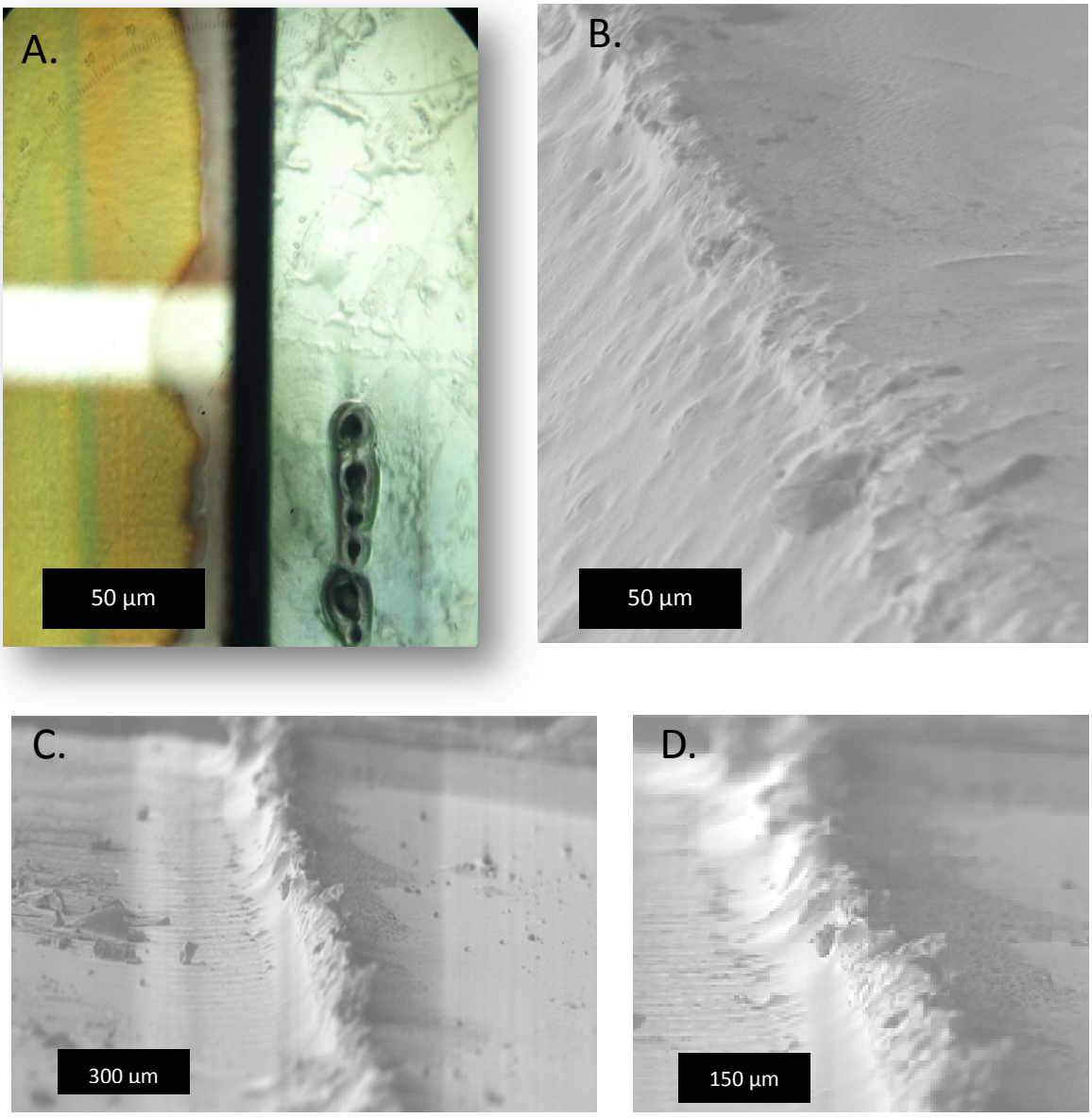

Figure 6.5.Microscopy images of UV-NVS coating on two terminal device substrates. A. Top-down optical microscope image of the cut edge with a UV-NVS coating completed over an aluminium electrode edge. B. Scanning electron microscope image of a coated cut surface C. Coated device substrate with polymeric active layer peeled off showing UV-NVS morphology over the cut edge. D. Zoomed in image of the morphology of UV-NVS at the cut edge.

Solution processing of UV-NVS films on device substrate produces substrates with an observable UV-NVS coating at the cut edge as seen in Figure 6.5A. Figure 6.5B shows an SEM image of the cut edge on a UV-NVS spun cast substrate. In order to observe the UV-NVS coating over the lip edge the P3HT polymeric layer was

removed from a completed substrate and imaged down the length of the cut seen in Figure 6.5C. UV-NVS spun cast films can be seen to be formed over the cut edge down the length of cut. The zoomed in image in Figure 6.5D shows the morphology of the film extending laterally over the cut edge. Solution processing of UV-NVS insulating films across machined transistor substrates shows insulating films which extend over the cut edge being formed across the machine cut surface. The films show resistances on the order of 100MΩS in the device structure showing the scope for the room temperature processing of dielectric films across a machine cut vertical wall transistor structure.

6.2.1 Failure Mechanism in UV-NVS Dielectric Films

SEM was used to gain an understanding of the microscopic topography over machine cut substrates. Through the use of a perpendicular sample mount (as discussed in Material and Methods § 2.3.3) images of two terminal device substrates with and without solution processed functional materials were evaluated down the cut axis. Figure 6.6 shows SEM images of fabricated two terminal device substrates. Imaging the cross section of the device allows for the topography to be understood across the cut surface and edge.

Figure 6.6A shows the cross section of a two terminal device substrate with a vertical wall introduced. The depth of the trench cut is measured at 500µm and appears consistent down the cut axis. Minimal schwarf debris is seen across the cut trench from the cutting process. Figure 6.6B shows the mechanical cut surface moving up to the edge of the top electrode. Undulations are visible across the cut surface casued from the cutting process. At the cut lip these undulations also appear and cause varied topography down the length of the cut at the lip edge.

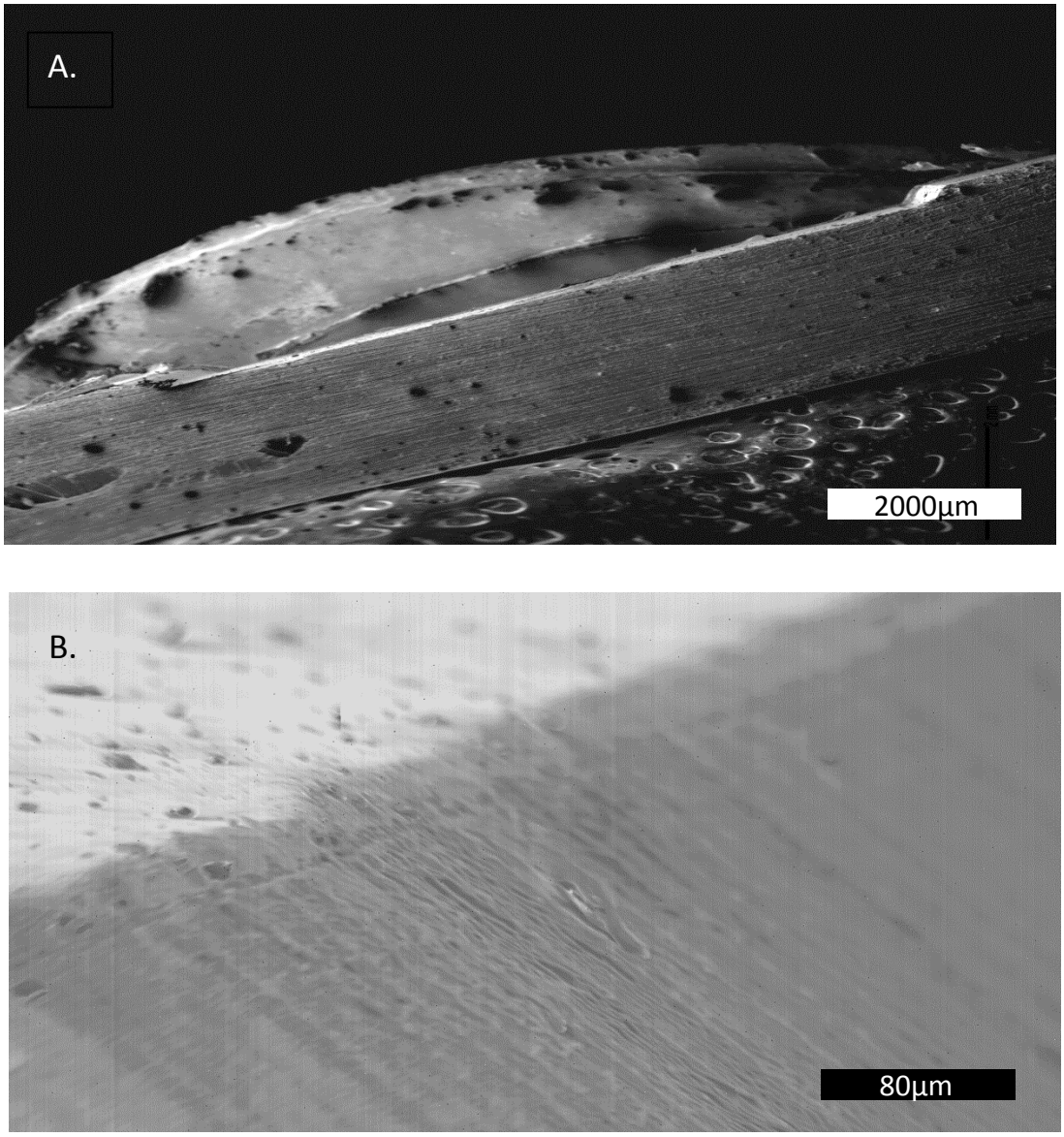

Figure 6.6. Scanning electron microscope images of two terminal device substrates before solution processing of a functional material. A. Macro scale Image taken down the axis of the vertical cut showing the vertical wall down the distance of the substrate. B. Zoomed in at the surface cut edge at the top electrode.

Due to the dimpled topography at the surface of the UV-NVS film it was possible to observe the distribution across the lip edge of the UV-NVS functional material. Processed two terminal device substrates were imaged using SEM and possible failure mechanisms identified. Figure 6.7A shows the cut edge with a UV-NVS dielectric functional film solution processed. When compared to Figure 6.6B. Figure 6.7A has reduced definition of the cutter undulations down the length of the cut suggesting a planarising film across the cut surface. Figure 6.7B shows a zoomed in

image at the cut edge of a two terminal device substrate with a UV-NVS dielectric functional film. The dimpled topography of the UV-NVS protective film is visible down the length of the cut on the cut surface and can be seen approaching the cut edge. At the cut edge the film can be seen coating across the machined surface and the cut edge. The distribution of the UV-NVS dimpled features across the variable topography at the cut edge is not homogenous or consistent. With the topographic dimples not present over the highest points of the topography at the cut edge suggesting incomplete coverage over the cut edge as a mechanism of failure.

Figure 6.7C shows a two terminal device substrate with UV-NVS functional film solution processed and imaged angled top down perspective along the length of the cut. Down the cut edge the periodic undulations from the cutter tool can be seen. Observing down the length of the cut regions of incomplete coverage can be observed. The accompanying optical microscope image seen in Figure 6.7D shows an observable diffraction pattern at the cut edge suggesting regions of variable thickness. Figure 6.7E shows a two terminal device substrate with UV-NVS functional film solution processed. The image taken down the length of the cut shows a fissure caused at the cut edge in the UV-NVS functional film. It is speculated shrinkage during UV curing caused by internal stress in the UV-NVS film results in cracking across severe topographic features across the cut surface.[19] As residual solvent is removed from the film further shrinkage would be occurring within the film with the amount of shrinkage dependent on the adhesion to the surface and thickness of the film. With film shrinkage not scaling linearly with UV-NVS film thickness under favourable wetting conditions.[16]

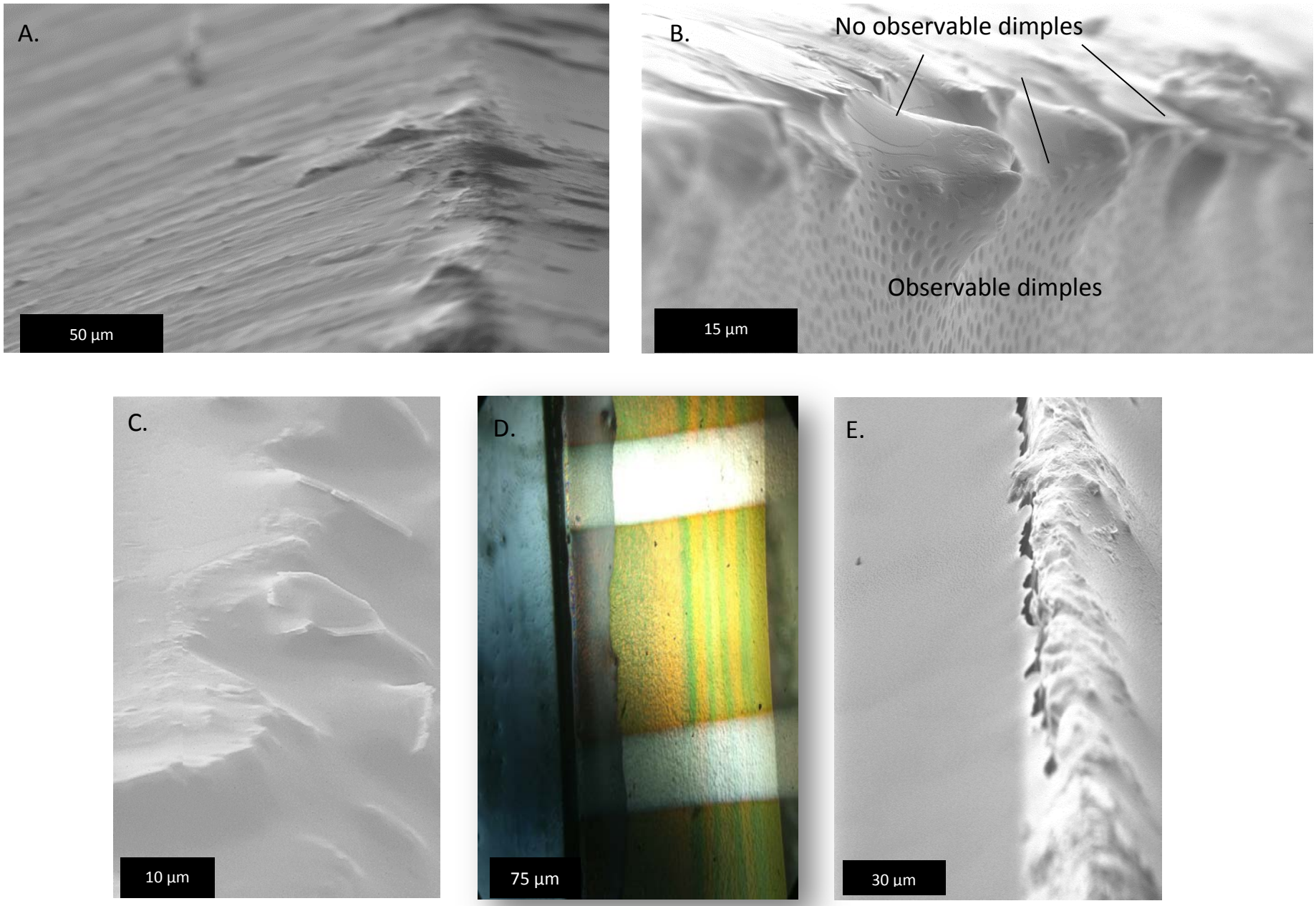

Figure 6.7. Scanning electron microscope images of solution processed UV-NVS dielectric functional films and observed failure mechanisms. A. Image taken down the axis of the vertical cut showing the vertical wall down the distance of the substrate with UV-NVS functional film. B. Zoomed in at the cut edge of the top electrode. C. Angled top-down view of the cut edge UV-NVS. D. Top-down microscopy image of a device showing poor wetting. E. Zoomed in at the cut edge microscopy image of observed film fissure.

Microscopy images of UV-NVS dielectric films show two failure mechanisms in completed devices. Regions of inconsistent coverage across severe topographic features caused by surface tension acting to pull the solution away from the edge. This failure mechanism is dependent on the viscosity of the applied liquid and the surface wetting properties between the liquid and the surface being coated.[20] And shrinkage upon UV curing causing fissuring down the cut surface and promoting incomplete coverage.[19] Both mechanisms are dependent on the wetting of the UV-NVS resin across the machine cut surface and the topography present across the surface. UV-NVS was developed for use as an optical coating on polycarbonate lenses and has been developed to provide favourable wetting chemistry for polycarbonate substrates. [16]As such, improving the failure rate of UV-NVS films is dependent on the topography across the cut surface and the wetting of UV-NVS across the electrode-active material multi-phase surface.

6.3 Fabrication of Vertical Transistors Incorporating UV-NVS

The effect of transistor fabrication on the two terminal source-drain circuit was investigated in order to optimise UV-NVS deposition and produce stable device behaviour. Fabrication of vertical transistor devices is described in §2.2 and was undertaken in three substrate batches with five devices on each substrate electrically characterised during fabrication to measure the impact of the fabrication step on the device electrical characteristics.

6.3.1 Standard Electrode Processing

Devices featuring asymmetric electrodes with a gold electrode matching the work function of the P3HT semiconductor and an aluminium electrode producing a Schottky barrier were used to study the source-drain current-voltage behaviour during fabrication of three terminal devices. Devices were fabricated with 30nm patterned gold source electrodes evaporated at 1 $A.s^{-1}$ at 10^{-7} Torr and electrically characterised during transistor fabrication. Figure 6.8 shows the current-voltage characteristics and simulation fit for a device during the fabrication of a three terminal device.

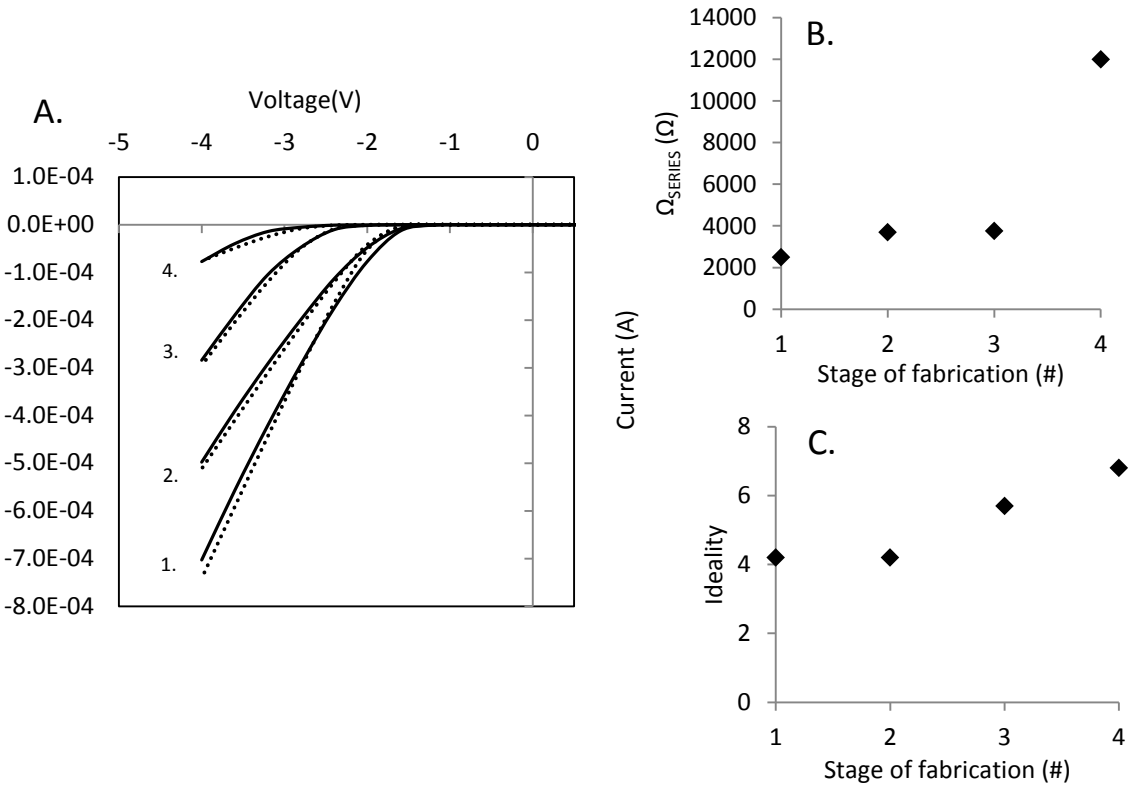

Figure 6.8. A. Current- voltage traces of a Schottky barrier diode undergoing processing towards a vertical transistor. 1. Initial current voltage trace. 2. Post machine cutting current-voltage trace. 3. Post dielectric film deposition current-voltage trace. 4. Post epoxy gate electrode deposition current-voltage trace. Dotted lines represent simulation model fits for corresponding equivalent circuit. B. Simulated series resistance changes during transistor fabrication. C. Simulated ideality factor across transistor fabrication.

During fabrication the source-drain circuit experiences changes in the device performance. Increases in series resistance are seen with simulated series resistance increasing from 2.5kΩ to 12kΩ shown in Figure 6.8B. An observed shift to higher turn on voltages is seen and is described by a change in the simulated ideality parameter for the devices seen in Figure 6.8C. The resulting current is seen to reduce to lower forward current magnitudes with higher observed with turn on voltages for device. Changes in device performance for the Schottky diode were measured across three substrates and are seen in Table 6.2.

After the introduction of a machine cut vertical wall a cumulative change in forward current to 71.7% ±9.9% of its initial forward current is seen to occur with an average turn on voltage of 2.4V measured. This reduction in forward current post machining

is attributed to a reduction in the operational area occurring during the cutting procedure leading to an increased series resistance. After processing of a UV-NVS dielectric functional film forward current magnitude is calculated to be 16.0% ±6.5% of the initial forward current value with a shift to higher turn on voltages to 3.4V observed. After the deposition of a gate electrode 4.3% ±0.9% of the forward current value was measured with an average turn on voltage of 3.8V. The result suggests that the fabrication of vertical transistors reduces the two terminal device performance and produces an unstable electrical device. The reduction of device performance was attributed to ambient processing and exposure of the operational area to environmental factors. In 2010 Egelhaaf *et al.*[21] studied the role of UV-VIS radiation on the degradation of P3HT. Egelhaaf *et al.*[21] prepared 100nm spin coated P3HT films and irradiated the samples at wavelengths across the UV-VIS range. Through a reaction chamber environmental variables temperature, humidity and partial pressure were controlled and a xenon lamp source used to generate the selected radiation wavelength. Egelhaaf *et al.*[21] established the degradation proceeds through a radical based mechanism driven by UV light and accelerated by increasing temperature and humidity. The exposure to UV leads to scission of C-C bonds and fragmentation within the P3HT molecule. Under this situation it has been shown that the alkyl groups and thiophene rings disappear leading to the formation of oxidised species. [22] Furthermore, Egelhaaf *et al.*[21] propose an empirical mechanism linking environmental variables to the rate of degradation.

$$\frac{-dE}{\varepsilon_\tau dt} = \frac{dn_T}{Adt} = \frac{\beta(po_2 \to \infty, \lambda, T) I_o(\lambda)}{1 + bT\, {p_{o_2}}^{-1}} + c(\, p_{o_2}, T) \qquad \text{Equation 6.1}$$

With E= absorbance of the film, ε_τ= the extinction coefficient for a thiophene unit, A= the unit area, n_T= number of moles of thiophene rings, I_o= the incident photon flux , p_{o_2}= oxygen partial pressure and β an effectiveness coefficient. From equation 6.1 it is shown that the intensity of the light is a key driver in the degradation rate. In order to improve the electrical stability an electrode pattern was devised that would reduce the exposure of the operational area to environmental factors that could result in the degradation of P3HT polymer.

Table 6.2 Measured Schottky barrier device forward-current during transistor fabrication for standard electrode devices.

Device	*Initial*		*Post machining*			*Post dielectric deposition*			*Post epoxy gate deposition*		
Substrate 1	I_{FWD} (A)	V_{ON}(V)	I_{FWD} (A)	V_{ON}(V)	I_{FWD}(%)	I_{FWD} (A)	V_{ON}(V)	I_{FWD}(%)	I_{FWD} (A)	V_{ON}(V)	I_{FWD}(%)
1	-2.2E-03	1.8	-1.0E-03	2.6	47.3	-4.9E-05	3.5	2.2	-4.8E-06	4.0	0.2
2	-8.1E-04	1.8	-5.1E-04	2.4	63.1	-4.0E-04	3.2	49.8	-1.4E-04	3.6	17.1
3	-4.4E-04	2.4	-2.0E-04	2.5	45.7	-4.7E-05	3.6	10.7	-3.3E-05	4.0	7.6
4	-8.6E-04	2.2	-6.5E-04	2.4	75.7	-1.7E-04	3.5	19.6	-3.2E-05	3.6	3.8
5	-7.4E-04	2.1	-3.9E-04	2.6	52.2	-6.9E-05	3.6	9.3	-2.2E-05	3.8	3.0
Substrate 2											
1	-6.0E-04	2.1	-7.6E-04	2.2	127.6	-2.3E-04	3.6	38.4	-2.9E-05	3.8	4.9
2	-6.3E-04	2.1	-5.5E-04	2.2	86.6	-1.0E-04	3.6	16.2	-1.4E-05	3.8	2.2
3	-6.7E-04	2.0	-4.6E-04	3.0	68.3	-7.2E-05	3.2	10.8	-3.0E-05	3.8	4.5
4	-7.1E-04	2.1	-6.7E-04	2.2	94.6	-1.3E-04	3.2	19.1	-2.8E-05	3.8	4.0
5	-6.3E-04	2.4	-5.8E-04	2.5	92.4	-6.3E-05	3.2	10.1	-1.0E-05	3.8	1.7
Substrate 3											
1	-7.0E-04	2.0	-4.9E-04	2.2	69.9	-1.0E-04	3.2	14.9	-4.3E-05	3.6	6.1
2	-8.0E-04	2.0	-6.1E-04	2.2	76.0	-1.6E-04	3.4	20.1	-4.9E-05	3.7	6.1
3	-7.3E-04	2.0	-3.7E-04	2.4	50.4	-2.9E-05	3.5	4.0	-3.5E-06	3.8	0.5
4	-8.8E-04	2.0	-5.6E-04	2.2	63.8	-7.2E-05	3.5	8.2	-1.2E-05	3.7	1.3
5	-8.9E-04	2.0	-5.4E-04	2.2	61.3	-5.7E-05	3.5	6.4	-8.2E-06	3.7	0.9

6.3.2 Encapsulating Electrode Processing

In order to reduce the exposure to ambient conditions and improve electrical stability an encapsulating electrode pattern was developed and studied. Figure 6.9 describes the standard electrode structure and compares it to the encapsulating electrode structure.

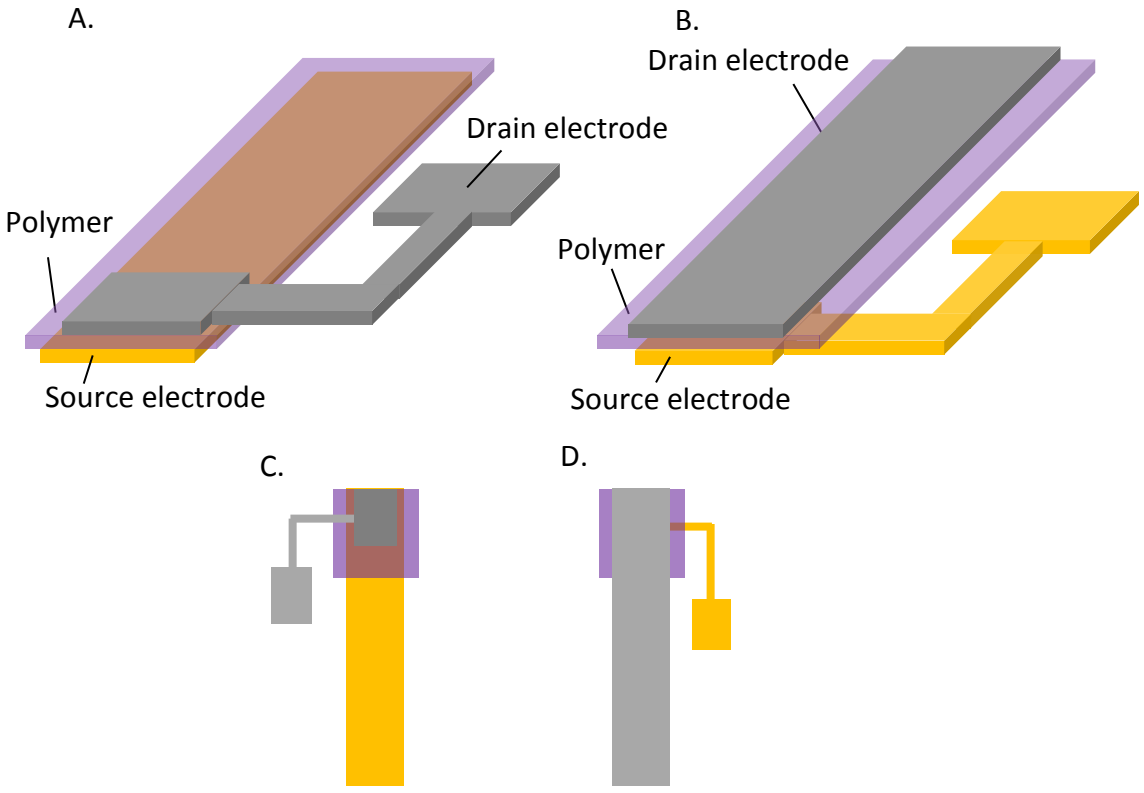

Figure 6.9. Graphical schematic of batch processed electrode patterns. A. Standard electrode pattern. B. Encapsulating electrode pattern .C. Top down schematic view of the showing standard electrode pattern D. Top down schematic view of the showing encapsulating electrode pattern.

Figure 6.10 shows the current-voltage characterisation and simulation fit for devices during the fabrication of a three terminal device featuring an encapsulating electrode.

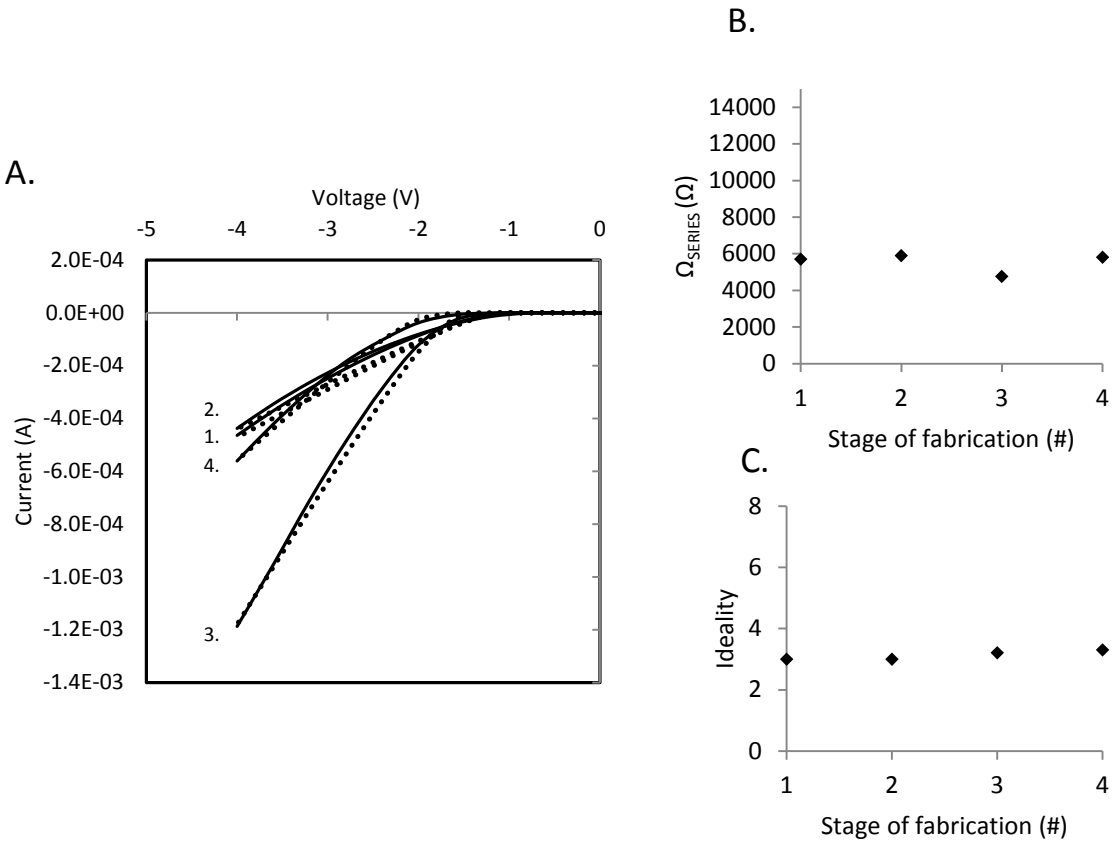

Figure 6.10. A. Current- voltage traces of an encapsulating electrode two terminal device undergoing processing towards a vertical transistor. 1. Initial current-voltage trace. 2. Post machine cutting current-voltage trace. 3. Post dielectric film deposition current-voltage trace. 4. Post epoxy gate electrode deposition. Dotted lines represent simulation model fits for corresponding equivalent circuit. B. Simulated series resistance changes during transistor fabrication. C. Simulated ideality factor across transistor fabrication.

Table 6.3 presents the forward current performance for devices featuring an encapsulating electrode pattern. The change in forward current was calculated for the processing steps for two terminal devices with encapsulating electrode and compared to the standard configuration. After the introduction of a machine cut a cumulative change in forward current was calculated to be 72.2% ±9.4% of its initial forward current value with an average turn on voltage of 2.1V. The value is comparable to the drop in forward current for standard electrode devices of 71.7% ±9.9% seen in Figure 6.8A. However, the average turn on voltage is seen to be comparably higher for the devices processed with the standard electrode pattern. After processing of the UV-NVS dielectric functional film forward current magnitude is calculated to be 146.9% ±36.9%of the initial forward current value with an average turn on voltage of 2.2V. After the deposition of a gate epoxy the cumulative

change in forward current is calculated to be 96.4% ±25.0% of the original current with an average turn on voltage of 2.4V.

Devices with an encapsulating electrode device show more reliable and improved device performance across transistor fabrication in comparison to standard electrode devices. Encapsulating electrode devices maintain a lower turn on voltage and more reliable forward current behaviour. Maintaining consistent device behaviour is essential to accurate transistor characterisation. The generation of transistor data requires a repeat voltage cycle for electrical characterisation. Understanding the stability of the two electrode platforms under a repeating voltage signal helps improve the resolution to extract transistor behaviour and understand the device stability.

Table 6.3. Measured device forward current during transistor fabrication for encapsulating electrode devices.

Device	*Initial*		*Post machining*			*Post dielectric deposition*			*Post epoxy gate deposition*		
Substrate1	I_{FWD} (A)	V_{ON}(V)	I_{FWD} (A)	V_{ON}(V)	I_{FWD}(%)	I_{FWD} (A)	V_{ON}(V)	I_{FWD}(%)	I_{FWD} (A)	V_{ON}(V)	I_{FWD}(%)
1	-5.7E-04	2.0	-4.4E-04	2.0	77.1	-1.1E-03	2.4	196.8	-6.1E-04	2.6	107.9
2	-4.9E-04	2.0	-3.9E-04	2.1	79.7	-8.1E-04	2.2	166.4	-5.0E-04	2.4	102.1
3	-3.4E-04	2.0	-2.7E-04	2.1	78.5	-7.5E-04	2.0	217.8	-4.4E-04	2.4	129.0
4	-5.7E-04	2.0	-5.0.E-04	2.1	87.3	-9.9E-04	2.2	174.3	-5.8E-04	2.5	102.4
5	-3.2E-04	2.0	-2.8E-04	2.1	88.5	-7.6E-04	2.2	239.0	-4.9E-04	2.4	152.4
Substrate2											
1	-8.9E-04	2.0	-8.0E-04	2.1	90.0	-1.0E-03	2.2	116.2	-6.6E-04	2.4	74.2
2	-2.7E-04	2.0	-2.6E-04	2.1	96.0	-5.2E-04	2.0	193.4	-3.4E-04	2.5	126.2
3	-4.3E-04	2.0	-4.6E-04	2.1	105.3	-8.4E-04	2.0	194.3	-5.4E-04	2.5	124.9
4	-8.4E-04	2.0	-4.6E-04	2.1	54.1	-7.2E-04	2.2	85.4	-3.0E-04	2.4	35.6
5	-7.1E-04	2.0	-6.7E-04	2.1	94.6	-1.4E-04	2.2	19.1	-2.8E-04	2.4	40.1
substrate 3											
1	-3.3E-04	2.0	-2.5E-04	2.1	75.6	-5.2E-04	2.1	157.8	-1.0E-04	2.4	31.5
2	-2.9E-04	2.0	-2.4E-04	2.2	81.0	-3.2E-04	2.1	108.8	-2.2E-04	2.4	73.4
3	-4.1E-04	2.1	-3.3E-04	2.1	81.4	-4.3E-04	2.2	105.1	-4.9E-04	2.5	121.8
4	-2.3E-04	2.0	-1.1E-04	2.1	48.0	-2.3E-04	2.2	97.8	-3.1E-04	2.4	135.9
5	-2.9E-04	2.0	-2.7E-04	2.1	91.0	-3.8E-04	2.2	130.6	-2.6E-04	2.4	87.9

6.3.3 Electrical Stability under Transistor Characterisation.

The stability of Schottky barrier vertical transistors during a transistor output test cycle was investigated and compared for two electrode configurations. A five trace test cycle seen in Figure 6.11A was used to reproduce a transistor test cycle and measure the changes in forward current between standard and encapsulating electrode devices without the application of a gate voltage. Figure 6.11B shows the normalised forward current behaviour for the two configurations across the test cycle for a device.

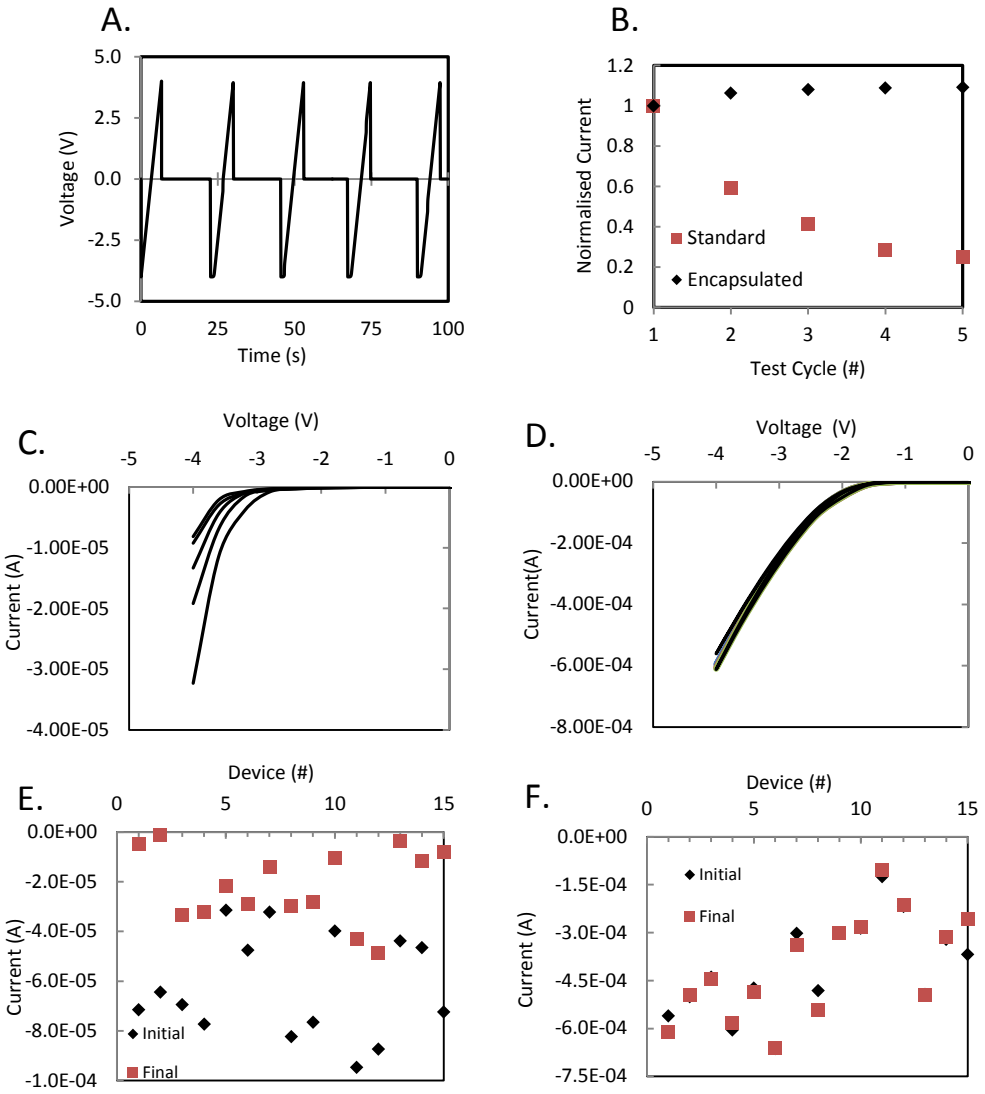

Figure 6.11. Forward current behaviour for three terminal devices incorporating a Schottky barrier for two electrode patterns A. Test cycle voltage input. B. Normalised forward current comparison for representative standard and encapsulating electrode devices. C. Forward quadrant current-voltage trace for a standard electrode device. D. Forward quadrant current-voltage trace for an encapsulating electrode device. E. Measured forward current at the beginning of the test cycle (black dot) and at the end of the test cycle (red square) for all 15 standard electrode devices. F. Measured forward current at the beginning of the test cycle (black dot) and at the end of the test cycle (red square) for all 15 encapsulating electrode devices.

The standard electrode device reduces in forward current across the test cycle dropping to 25% of the original measurement. The representative device with an encapsulating electrode experiences a marginal increase in the forward current behaviour within 9% of the original current. Figure 6.11C shows the measured forward current traces for a standard electrode device during the test cycle. Figure 6.11D shows the measured forward current traces for an encapsulating electrode device during the test cycle. The change in forward current at the beginning of the

test cycle compared to the end of the test cycle for fifteen devices can be seen in Figure 6.11E and Figure 6.11F respectively.

Across the test cycle the forward current is seen to drop by -3.9% ±5.6% on average for devices with an encapsulating electrode. In comparison devices with a standard electrode pattern show a forward current change of -63.7%±9.9%. The standard electrode device is seen to shift to higher turn on voltages with reduced current magnitude during the test cycle. This behaviour is consistent with changes in device behaviour during transistor fabrication seen in §6.3.1. In comparison the encapsulating electrode has reduced variation providing a more consistent platform with better device performance across the test cycle consistent with the improved performance across fabrication seen in §6.3.2.

During processing and testing fabricated devices experience changes in device performance. The use of an encapsulating electrode pattern improves the stability of devices and the reliability of transistor characterisation at the point of testing. The improvements are attributed to a greater encapsulation of the operational area resulting in less atmospheric exposure and increased electrical stability across fabrication.

6.4 Conclusions

In order to create vertical transistors with high lateral electric field strength the scaling possibilities of several dielectric materials were evaluated for producing dielectric films across a machine cut surface. UV-NVS, cytop, PMMA and $LiClO_4$: PEO were chosen as possible functional materials and solution processed with the short circuit failure rate calculated with respect to spin speed. Electrode composition is seen to affect the failure rate with symmetric gold-gold electrode devices showing greater failure rates compared to asymmetric gold-aluminium electrode devices. This is attributed to the formation of a native oxide on the aluminium electrode improving the wetting. UV-NVS and cytop were the best performed materials capable of creating insulating films across the machine cut topography with a UV-NVS failure rate of 60% in gold-gold devices and 20% in gold-

aluminium devices at 1000RPM spin speed. Cytop offered the lowest failure rate with a failure rate of 45% at 1000RPM in gold-gold devices and 20% failure rate at gold aluminium devices. Due to its ability to be processed at room temperature and low failure rate in gold-aluminium electrode devices at 1000RPM the PMMA based resin UV-NVS was chosen to be optimised for incorporation into vertical transistor devices.

Microscopy images of solution processed UV-NVS films across the machine cut surface show the formation of a film extending across the cut edge. In completed vertical transistor devices UV-NVS films produce gate-source and gate-drain circuits with resistances of Ω_{GS}=167MΩ and Ω_{GD}=17MΩ resulting in effective resistive films by spin coating films over machine cut topography. The performance of the source-drain Schottky barrier circuit was examined during UV-NVS processing. Fabrication of UV-NVS vertical transistor devices reduces device performance of the source-drain circuit with a cumulative drop in forward current to 4.3%±0.9% of the initial forward current value with an average turn on voltage of 3.8V measured. The drop in performance is attributed to ambient device processing and the UV exposure during curing.

An encapsulating electrode which reduced ambient exposure of the operational area was developed and tested. Encapsulated devices produce 96.4%±25.0% of the original current with an average turn on voltage of 2.4V post fabrication. Under a repeat voltage signal designed to replicate transistor characterisation encapsulated devices vary -3.9%±5.6% across the test cycle. In comparison devices with a standard electrode pattern show a forward current change of -63.7%±9.9% across the repeat signal. The encapsulating electrode limits the exposure to environmental dopants and improves device stability across device fabrication. This shows the benefits of an encapsulating electrode structure in improving device performance and stability in devices featuring ambient sensitive polymers. Resulting in an optimised P3HT vertical transistor platform that can be fabricated in ambient conditions featuring a solution processed dielectric.

References

1. Kim, F.S., et al., *Enhanced carrier mobility and electrical stability of n-channel polymer thin film transistors by use of low-k dielectric buffer layer*. Vol. 99. 2011: AIP. 173303.
2. Gusev, E.P., et al., *Ultrathin HfO2 films grown on silicon by atomic layer deposition for advanced gate dielectrics applications.* Microelectronic Engineering, 2003. **69**(2–4): p. 145-151.
3. Richard, P.D., et al., *Remote plasma enhanced CVD deposition of silicon nitride and oxide for gate insulators in (In, Ga)As FET devices.* Journal of Vacuum Science & Technology A, 1985. **3**(3): p. 867-872.
4. Collet, J., et al., *Low-voltage, 30 nm channel length, organic transistors with a self-assembled monolayer as gate insulating films.* Applied Physics Letters, 2000. **76**(14): p. 1941-1943.
5. Stassen, A.F., et al., *Influence of the gate dielectric on the mobility of rubrene single-crystal field-effect transistors.* Applied Physics Letters, 2004. **85**(17): p. 3899-3901.
6. Wang, G., et al., *Poly(3-hexylthiophene) field-effect transistors with high dielectric constant gate insulator.* Journal of Applied Physics, 2004. **95**(1): p. 316-322.
7. Majewski, L.A., et al., *High capacitance organic field-effect transistors with modified gate insulator surface.* Journal of Applied Physics, 2004. **96**(10): p. 5781-5787.
8. Rha, S.H., et al., *Vertically integrated submicron amorphous-In[sub 2]Ga[sub 2]ZnO[sub 7] thin film transistor using a low temperature process.* Applied Physics Letters, 2012. **100**(20): p. 203510.
9. Moradi, M., A.A. Fomani, and A. Nathan, *Effect of gate dielectric scaling in nanometer scale vertical thin film transistors.* Applied Physics Letters, 2011. **99**(22): p. 223503.
10. Peng, X., et al., *All-organic thin-film transistors made of alpha-sexithienyl semiconducting and various polymeric insulating layers.* Applied Physics Letters, 1990. **57**(19): p. 2013-2015.
11. Bao, Z., et al., *High-Performance Plastic Transistors Fabricated by Printing Techniques.* Chemistry of Materials, 1997. **9**(6): p. 1299-1301.
12. Rutenberg, I.M., et al., *Synthesis of Polymer Dielectric Layers for Organic Thin Film Transistors via Surface-Initiated Ring-Opening Metathesis Polymerization.* Journal of the American Chemical Society, 2004. **126**(13): p. 4062-4063.
13. Cheng, X., et al., *Air Stable Cross-Linked Cytop Ultrathin Gate Dielectric for High Yield Low-Voltage Top-Gate Organic Field-Effect Transistors.* Chemistry of Materials, 2010. **22**(4): p. 1559-1566.
14. Zhu, C., et al., *Investigation on interface related charge trap and loss characteristics of high-k based trapping structures by electrostatic force microscopy.* Applied Physics Letters, 2011. **99**(22): p. 223504.
15. Ortiz, R.o.P., A. Facchetti, and T.J. Marks, *High-k Organic, Inorganic, and Hybrid Dielectrics for Low-Voltage Organic Field-Effect Transistors.* Chemical Reviews, 2009. **110**(1): p. 205-239.
16. Treadway, G., *UV-NVS film requirements*, D. Gruszecki, Editor 2013: e-mail correspondence.
17. Walsh, C.B. and E.I. Franses, *Ultrathin PMMA films spin-coated from toluene solutions.* Thin Solid Films, 2003. **429**(1-2): p. 71-76.

18. García, B., et al., *Structural and Electrical Characterization of Isotactic PMMA Thin Films Deposited by Spin Coating.* Macromolecular Symposia, 2009. **283-284**(1): p. 342-347.
19. Decker, C., *Kinetic Analysis and Performance of UV-Curable Coatings*, in *Radiation Curing*, S.P. Pappas, Editor. 1992, Springer US. p. 135-179.
20. Fischer, K. and R. Suss. *Spray coating - a solution for resist film deposition across severe topography*. in *Electronics Manufacturing Technology Symposium, 2004. IEEE/CPMT/SEMI 29th International*. 2004.
21. Hintz, H., et al., *Photodegradation of P3HT−A Systematic Study of Environmental Factors.* Chemistry of Materials, 2010. **23**(2): p. 145-154.
22. Manceau, M., et al., *The mechanism of photo- and thermooxidation of poly(3-hexylthiophene) (P3HT) reconsidered.* Polymer Degradation and Stability, 2009. **94**(6): p. 898-907.

Chapter 7

7. Channel Enhancement in Machine Cut Vertical OFETs

Introduction

The switching performance and operating voltages of the transistor devices which comprise a circuit ultimately determine the circuit performance. To this end, reducing gate length and increasing operational area in transistor structures is known to improve the performance criteria and commercial feasibility of prospective devices.[1-3] In 2008 Yang *et al.* demonstrated a large area vertical architecture VOFET capable of mA current and an ON/OFF ratio of 10^3.[4]The layered structure operates in part due to penetration of the electric field through a thin metal electrode into the device active layer allowing a large enhancement region to form under relatively low operating biases. The work demonstrates the scope of vertical architectures to create field effect devices utilising the penetration depth to increase enhancement current through the conductive channel, however, the configuration is ultimately limited by the inherent need for a very thin conductive layer within the structure which will limit device power.

In order to improve device performance and create a more generally applicable architecture, a novel VOFET architecture is presented and studied for potential enhancement operation. The device structure allows for varied operational area and easily controlled gate length defined by the thickness of an active layer polymer film. The structure can be fabricated in ambient conditions without the use of lithography and incorporates a spun cast dielectric film.

7.1 Device Operation

7.1.1 Device Fabrication

The VOFET incorporates a 45^{o} gate created using a machine cut wall is shown in Figure 7.1. A polycarbonate substrate is employed and a two terminal vertical layered structure is deposited sequentially (Figure 7.1B) featuring 30nm thick contact electrodes. The mechanical properties of the plastic substrate facilitates a machine cut trench to be introduced with the operational area of the device determined by the width of the electrodes and the semiconductor thickness (Figure 7.1C). A 10µm thick dielectric layer is spin coated over the machine cut substrate seen in Figure 7.1D. An epoxy gate electrode is deposited manually over the functional film creating a capacitive cell (Figure 7.1E). An optical image of a completed device is seen in Figure 7.1F.

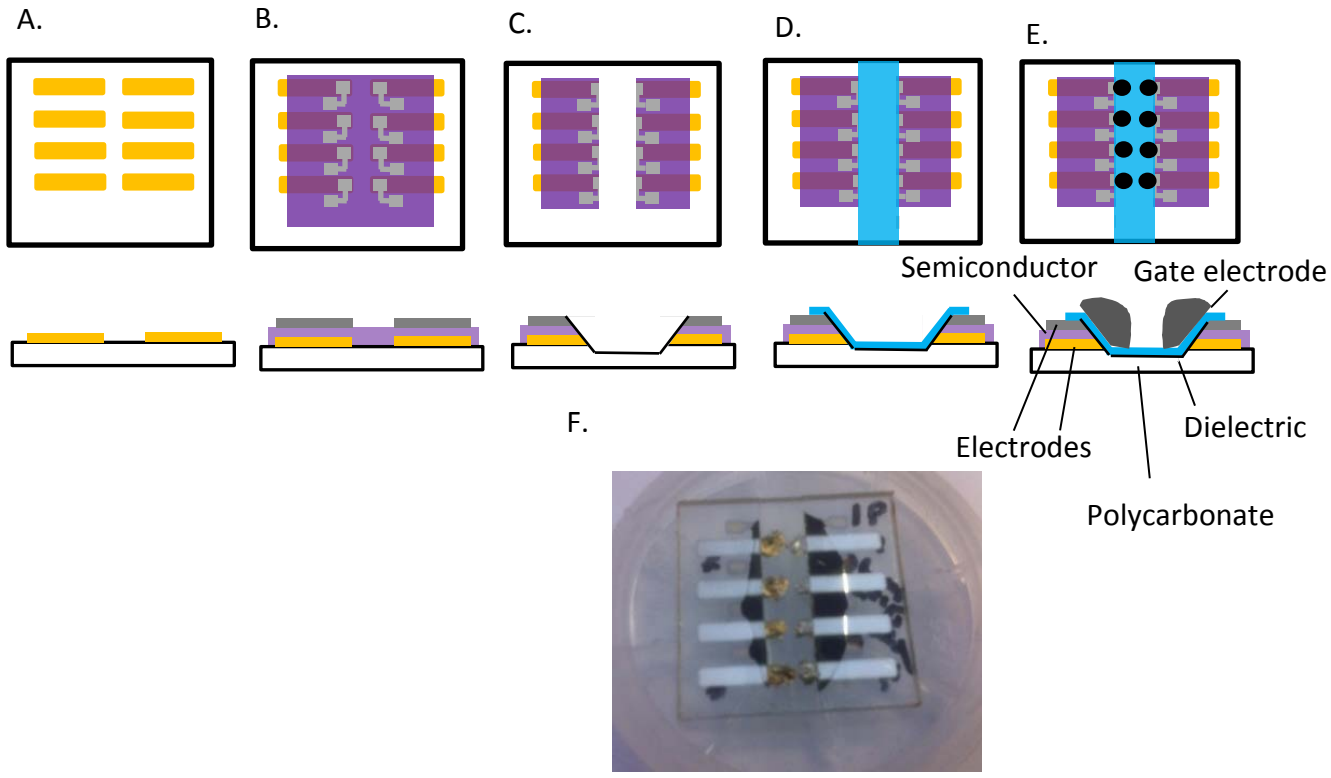

Figure 7.1. Machine cut VOFET fabrication. A. Commercial polycarbonate sheets are laser cut to 25.4mm^{2} with a working electrode deposited by means of sputtering or evaporation through a shadow mask. B. A semiconducting polymer is spin coated from solution onto working electrode and annealed with a second working electrode deposited through shadow mask. C. A CNC machine cutter introduces a vertical wall into the device architecture D. A dielectric functional film is spin coated across the surface. E. Silver epoxy gate electrode manually deposited. F. Optical image of a P3HT machine cut VOFET.

The structure has been optimised in line with findings in previous chapters to improve device stability, yield and dielectric deposition. The methodology allows for the scaling of gate length with the thickness of the spin coated semiconductor layer and control of the device operational area.

7.1.2 Principle of Operation

Unique to the architecture is an angled machine cut wall at an angle of 45° to the normal resulting in an angled interface at the dielectric-semiconductor interface seen in Figure 7.1. The penetration of the electric field into the active layer from the gate for the structure is expected to introduce polarisation through the material resulting in a region of increased conductivity known as an enhancement region that ultimately determines device performance.[5] In order to determine operational voltages, the electric field lines produced at the dielectric-active layer interface are sketched under various high-low bias conditions for the three terminal structure and presented in Figure 7.2. The enhancement channel is not expected to be symmetrical in the device and is dependent on which electrode is chosen for charge injection. Field lines indicate that greater channel enhancement will be possible using the bottom electrode for charge injection. Due to P3HT exhibiting p-type conduction[6]with holes the majority carriers the biasing conditions in Figure 7.2C and 7.2D are expected to allow for the creation of an enhancement region. Planar OFETs featuring P3HT devices have shown enhancement in the -/- quadrant and are studied under source high, gate low biasing conditions.[7, 8]

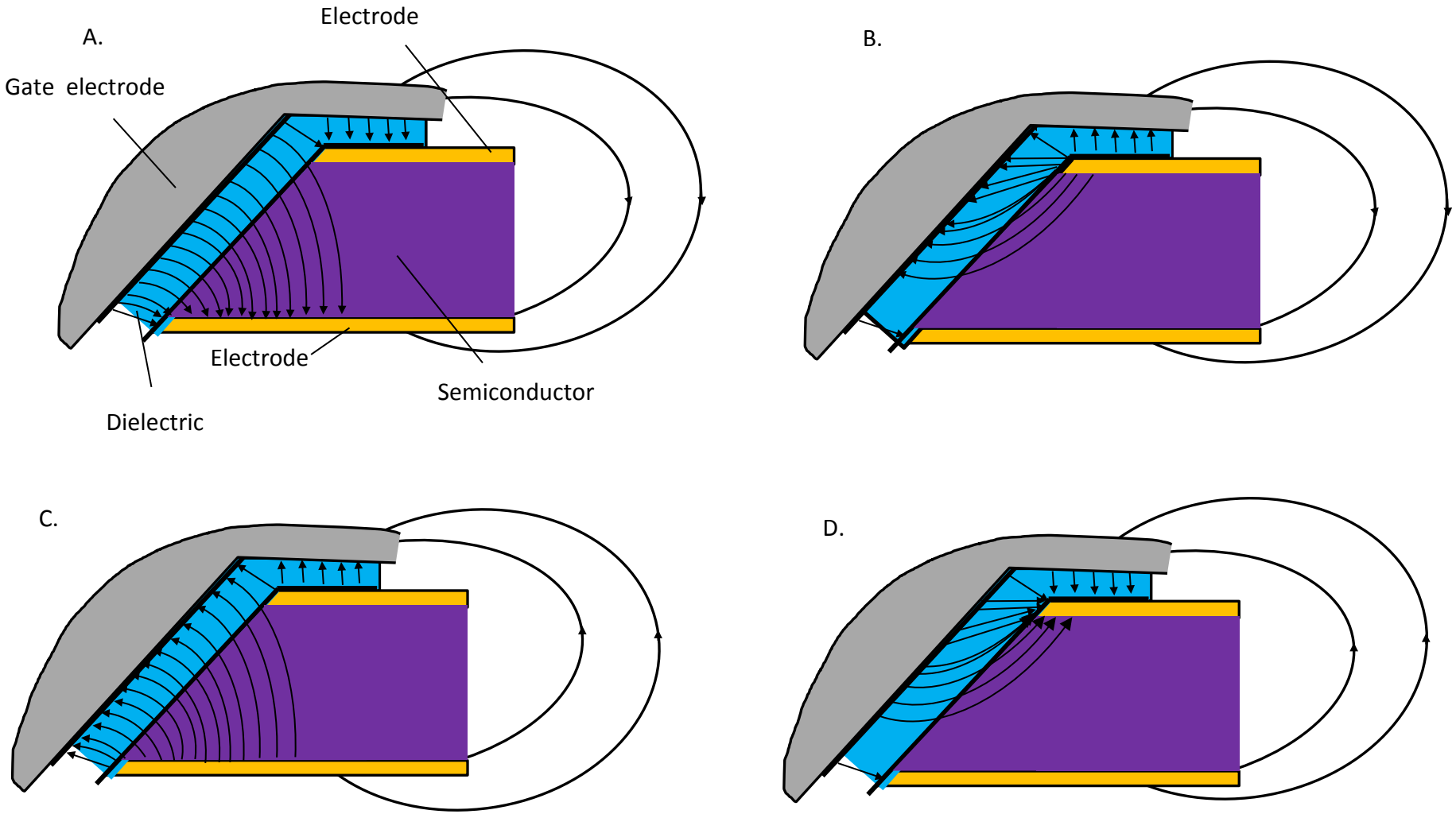

Figure 7.2. Cross-section schematic of a vertical device architecture with angled vertical wall and the resulting electric field lines under various three terminal operation biases. A. Source low, gate high operational biasing B. Source low, gate high operation with alternate charge injection electrode. C. Source high, gate low operational biasing. D. Source high, gate high operational biasing with alternate charge injection electrode. Electric field lines depict the force experienced on a positive charged particle.

An estimate of the electric field strength produced by the gate was calculated using a parallel plate capacitor approximation for a 20µm P3HT active layer device seen in Figure 7.3A. The electric field at a distance from the gate was calculated down the length of the source electrode. With the parallel plate capacitor distance, d calculated for the 45° gate electrode using the cosine law with the resulting electric field profile at five distances seen in Figure 7.3B.

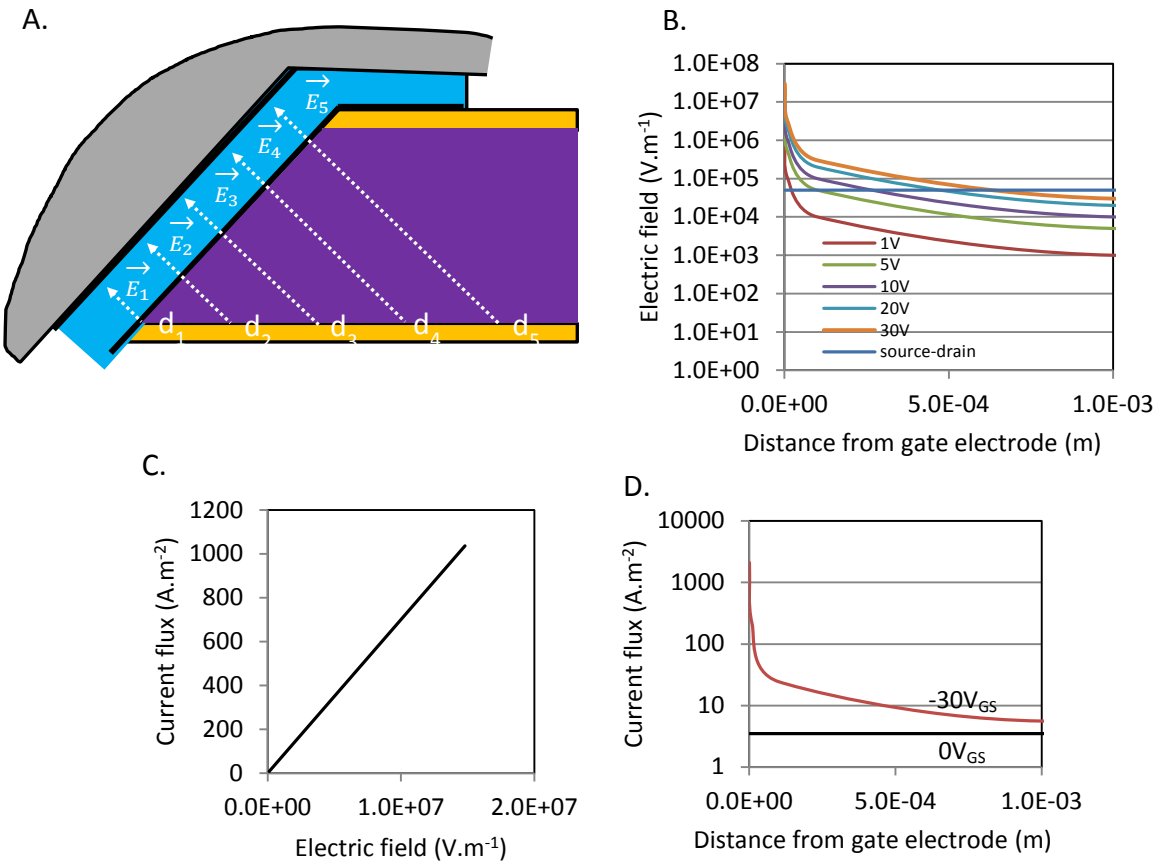

Figure 7.3. Electric field calculation for vertical VOFET with a 20µm active layer. A. Calculation schematic. B. Electric field profile incident into the channel under varied gate voltage, V_{GS} -$1V_{GS}$ (red line), -$5V_{GS}$, (green line), -$10V_{GS}$ (purple line), - $20V_{GS}$ (blue line), - $30V_{GS}$ (orange line). The source-drain electric field at an applied V_{DS}=1V (blue line).C. J vs. E curve for P3HT organic semiconductor. D. Current flux profile for the active layer at V_{GS}=0V (black line) at an applied V_{GS}= -30V.

An electric field magnitude on the order of 10^7 V.m^{-1} is calculated to be incident into the device active layer at an applied gate voltage -30V. In comparison at a source-drain operating bias of 1V, the source-drain electric field is calculated to be 5 x 10^4 V.m^{-1}. During an additional gate voltage the increase in field magnitude within the active layer is expected to produce a region of higher conductivity, increasing

the current flux of the P3HT active layer. The current flux vs. electric field behaviour for P3HT is seen in Figure 7.3C. With current flux increasing linearly under applied electric field over the range 0 $V.m^{-1}$ to 1.5 x 10^{7} $V.m^{-1}$. The resulting current flux profile within the device for an ON state (V_{GS}=-30V) and OFF state (V_{GS}=0V) can be seen in Figure 7.3B. A three order increase in the current-flux magnitude 10µm from the gate electrode. The calculation suggests a gate controlled enhancement region to be formed within the active layer resulting in an enhancement current.

The device structure features a large operational area producing a leakage current between source-drain during operation. Key to validating the structure is an enhancement current that is resolvable from the two terminal source-drain leakage current. The influence of the device dimensions operational area and active layer thickness on leakage current can be seen in Figure 7.4A and Figure 7.4B with drain leakage current increasing with increasing operational area. Leakage current is also seen to increase as active layer thickness is reduced. The device structure is capable of producing 0.9mA leakage at an operating voltage of -4V_{DS}. The high possible currents with the structure and low operating voltages make the structure a candidate for a Schottky barrier VOFET. Figure 7.3C shows the electrical performance of a large operational (1.5mm^2) area P3HT/Aluminium Schottky device. With the change in the conductivity of the device under incident electric field shown in Figure 7.4D and E.

The conduction of the device under forward bias conditions shows over the range 3 x 10^{-8} S to 3 x 10^{-4}S a change in conduction of four orders of magnitude under an incident electric field 1 x 10^{6} $V.m^{-1}$. Under reverse bias conditions the conductivity spans the range 3 x 10^{-8}S to 5 x 10^{-7}S increasing with increasing incident electric field. Under forward bias there is a threshold point at which conductivity increases rapidly. This threshold region represents the greatest rate of change in conductivity with respect to electric field. With P3HT conduction increasing until the intrinsic conductivity of the material is exceeded and charge injection is space charge limited. In order to realise a potential enhancement mode structure space charge limited current must be avoided. A device operating in the space charge limited regime is charge injection limited and defines the physical dimensions possible of

the active layer thickness of the device and operational biases in enhancement mode operation.

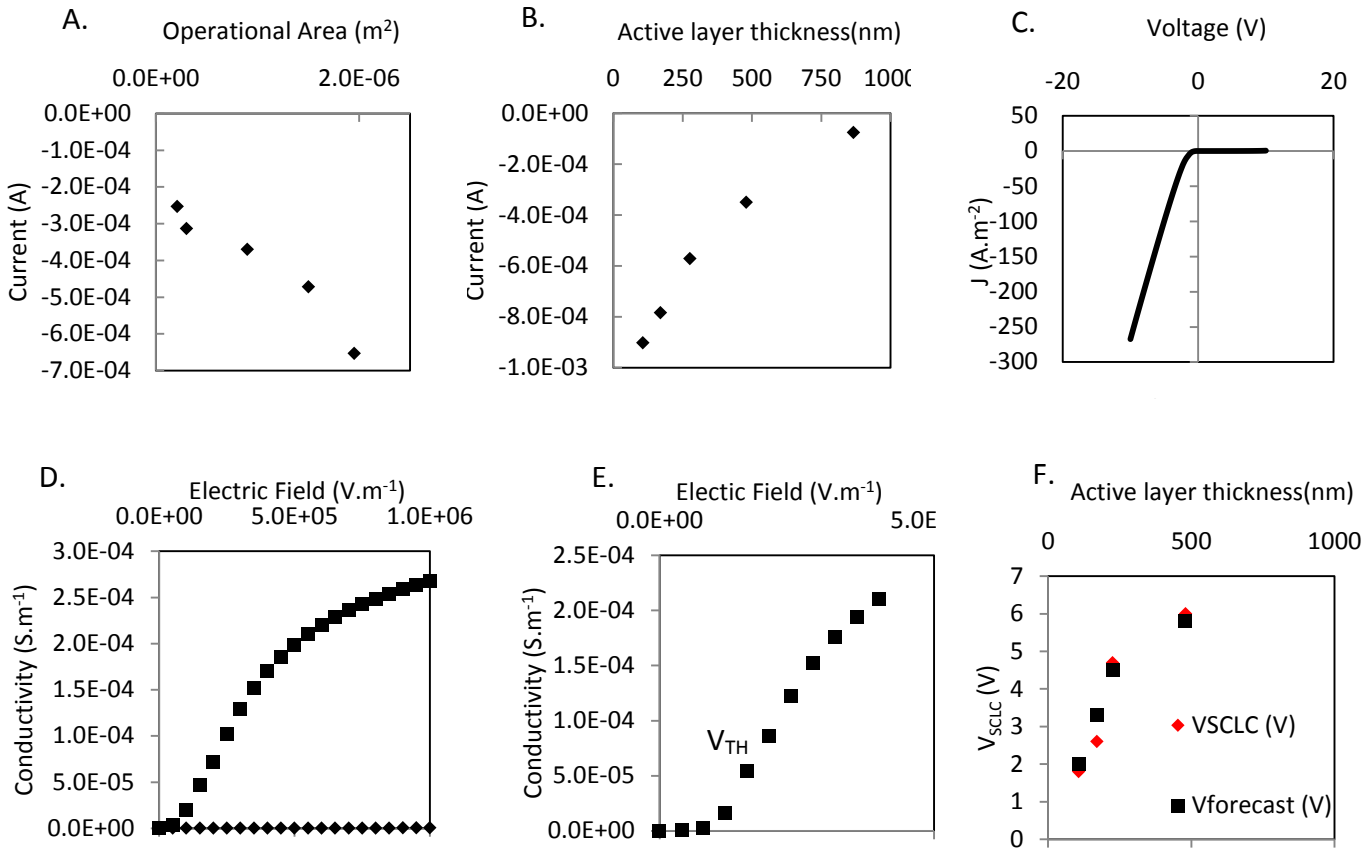

Figure 7.4. P3HT-Aluminium Schottky diode electrical characterisation. A. Influence of device operational area on forward current using a thin film (225nm) P3HT active layer B. Influence of active layer thickness on forward current. C. J vs. V current curve. D. Changes in conductivity state for the device under forward biasing (square marker) and reverse biasing (diamond marker). E. Changes in conductivity state at low electric field strengths F. Experimentally obtained space charge voltage values (red marker) compared to calculated values (black marker).

The space charge regime for P3HT was experimentally determined for P3HT extracting V_{SCLC} using the method outlined by Smetjek *et al.*[9] and is plotted with respect to active layer thickness in Figure 7.4D with the current-voltage traces supplied in Appendix C. An active layer thickness of 225nm, corresponding to a 1000RPM spin coated active layer will allow ohmic injection up to 4.5V whilst drop cast P3HT is not forecast to become space charge limited until a voltage of 100V is applied. In order to probe a structure for enhancement current a voltage range of

$\pm 4V_{DS}$ is selected, corresponding to the region of greatest change in conduction for the diode forward current and allowing ohmic injection for active layer thicknesses with two dimensions, corresponding to 225nm and 20µm active layer films.

7.1.3 Simulated Device Performance

The expected enhancement current is calculated for 225nm and 20µm active layer device dimensions and the electrical performance simulated and presented in Figure 7.5. A consistent Schottky barrier height is assumed and the total drain current is calculated using the electric profile shown in Figure 7.3D and the current flux vs. electric field relationship seen in Figure 7.3C. The role of penetration depth and its effect on device performance is shown in Figure 7.5E.

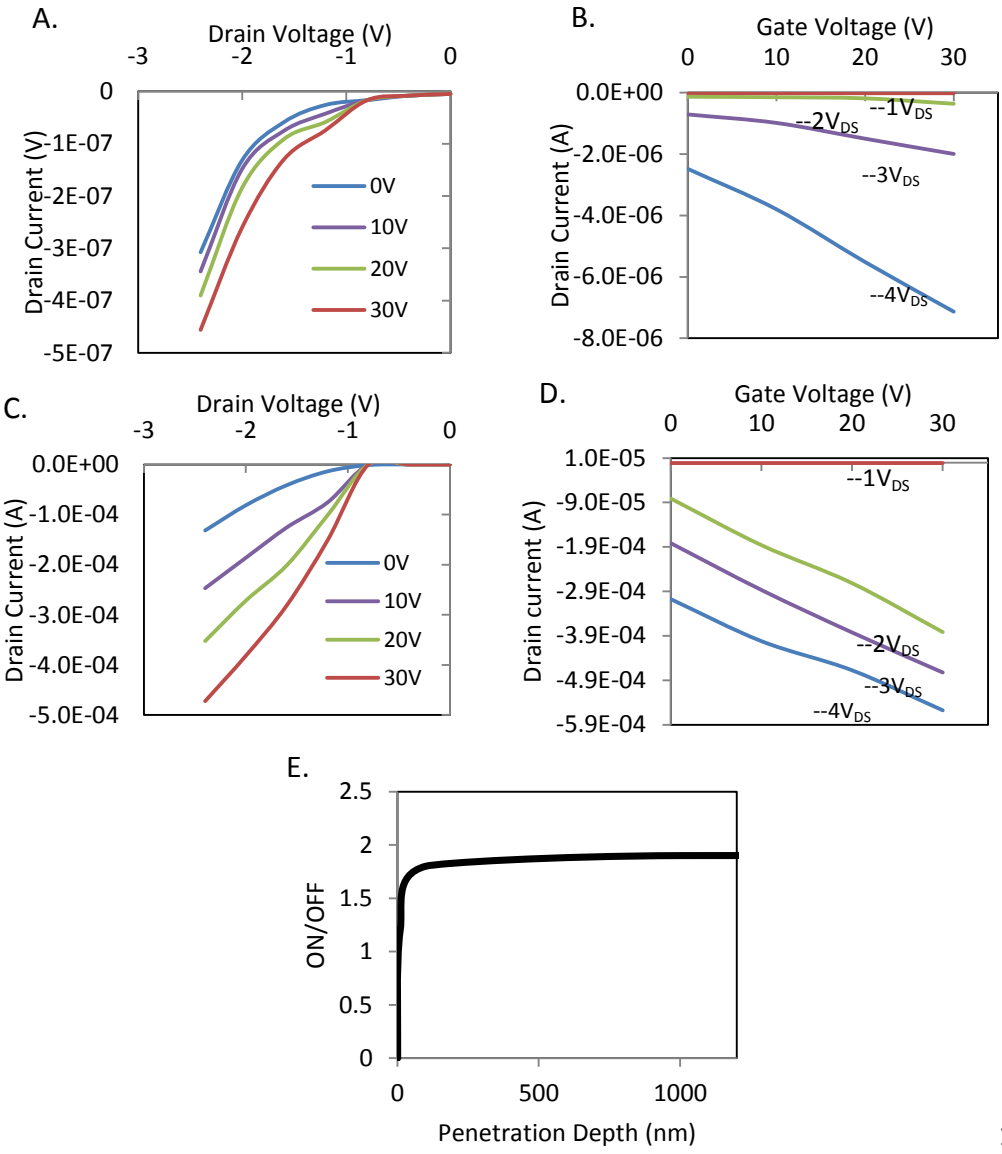

Figure 7.5. Simulated transistor performance. A. Output plot for 20µm active layer thickness. B. Transfer plot. C. Output plot for 225nm active layer thickness. D. Transfer plot. E. Role of penetration depth on transistor performance.

Figure 7.5A shows the output performance over the range $0V_{GS}$ to $-30V_{GS}$ for the 20µm active layer structure. Simulated performance shows enhancement current on the order of 10^{-7}A and an increasing drain current with increases in gate voltage at low voltages. At $0V_{GS}$ the channel series resistance, Ω_{series} is 120MΩ reducing to 60MΩ under an applied $30V_{GS}$. The transfer plot of the device over the range $0V_{DS}$ to $-4V_{DS}$ shows an on/off ratio of 2 seen in Figure 7.5B. Figure 7.5C shows the output performance over the range $0V_{GS}$ to $-30V_{GS}$ for the 225nm active layer structure. Simulated performance shows enhancement current on the order of 10^{-4}A. At $0V_{GS}$ the series resistance, Ω_{series} is 65kΩ reducing to 33kΩ $0V_{GS}$ under an applied $30V_{GS}$ with an on/off ratio of 2 seen in the transfer plot. The on/off performance for varying penetration depth of the lateral electric field is seen in Figure 7.5E. Sufficient depth is necessary for the device to experience transistor function.

The equivalent circuit presented in Figure 7.6A is proposed to describe the electrical performance of the Schottky barrier VOFET device. The change in the source-drain equivalent circuit from the $0V_{GS}$ OFF state to the $-30V_{GS}$ ON state for a 225nm active layer device is seen in Figure 7.6B and C respectively.

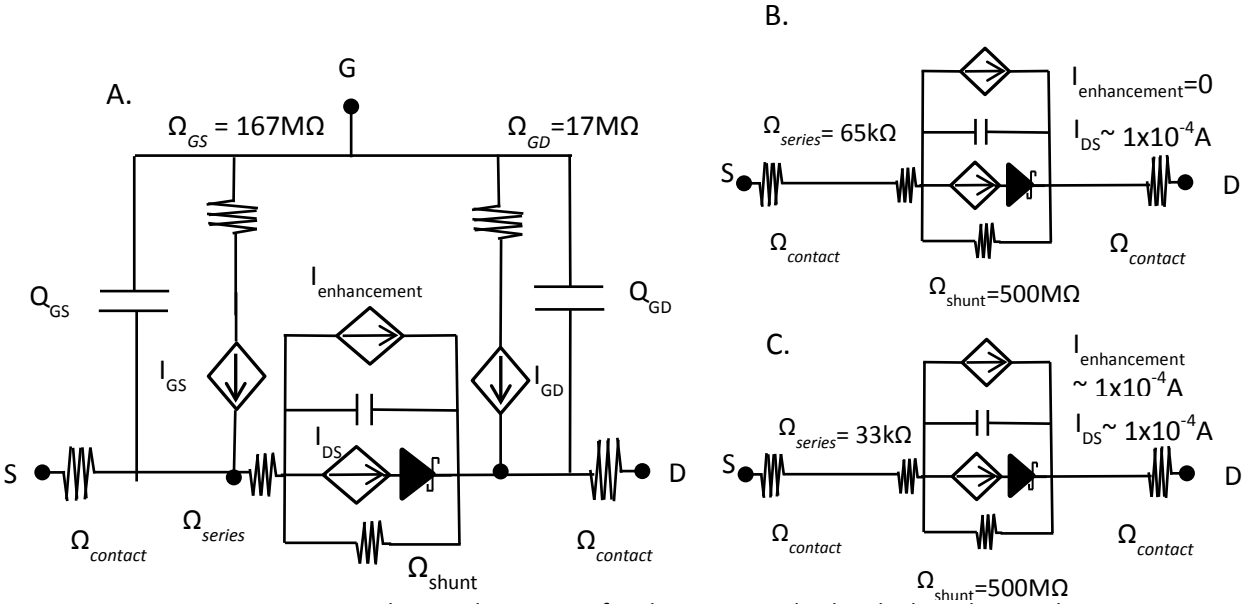

Figure 7.6. A. Proposed equivalent circuit for three terminal Schottky based OFET devices. B. Source-drain equivalent circuit with 0VGS gate bias. C. Source-drain equivalent circuit under an applied -30VGS gate bias.

Under an applied gate voltage the channel series resistance, Ω_{series} is reduced resulting in an increased total drain current. The enhancement current is described as a current in parallel with the two terminal leakage current. In both cases enhancement currents are on the order of leakage current suggesting real world devices with comparable dimensions should yield devices with a resolvable enhancement current.

7.2 Three Terminal Devices Based on Schottky Two Terminal Devices

7.2.1 Electrical Characterisation of VOFET Devices.

Fabricated devices underwent output characterisation with current-voltage traces V_{DS} vs. I_{DS} obtained for sequential gate voltages at 15s intervals over the range V_{DS}= ± 4V at a ramp of 0.65V.s^{-1}. The range ±4V was selected to provide adequate resolution for threshold behaviour, the range of greatest change in conduction within the proposed Schottky barrier device. Gate voltage was sequentially increased up to V_{GS} =-30V increasing the lateral electrical field magnitude by over a magnitude and creating a lateral field on the order of 1 x 10^7V.m^{-1}. The three terminal device schematic can be seen in Figure 7.7A with testing biases. In order to study the transient behaviour of the device two applied gate signals were applied with respect to time and drain current-voltage traces captured. A gate signal applying -30V_{GS} turning the device from an OFF (0V) to an ON (-30V) was used and can be seen in Figure 7.7B. And an ON/OFF signal switching between an OFF state (0V) and ON state (-30V) repeatedly seen in Figure 7.7C. Completed devices were tested in ambient conditions using the testing probe station described in Material and Methods §2.6.1. Current-voltage characteristics were measured using a contact probe station utilising a LabVIEW data acquisition GUI described in Materials and Methods §2.4.

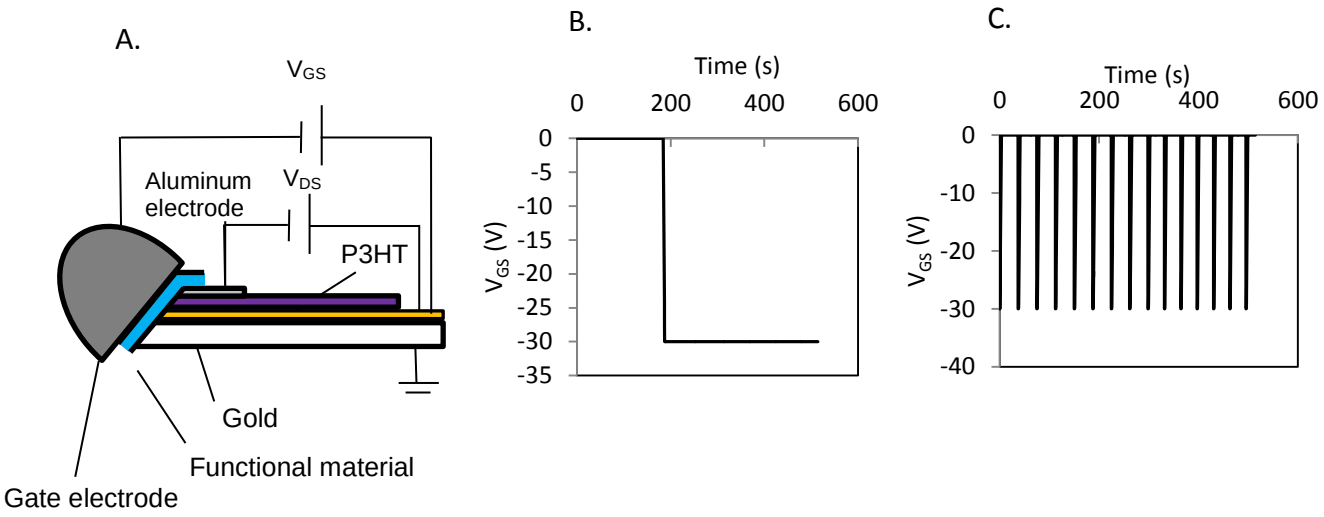

Figure 7.7. Planar schematic of two terminal Schottky substrates and gate input signals. A. Cross section and biasing schematic of a discrete device. B. Turn on gate signal input in which -30V_{GS} is applied turning the device from an OFF (0V_{GS}) to ON state C. -30V gate signal input turning the device from an OFF state to an ON state. Source-drain current were measured under the incident signals to determine drain current magnitude during the applied signal.

7.2.2 Thin Film Schottky Barrier VOFETs

A thin film Schottky barrier VOFET with an active layer thickness of 225nm was fabricated and electrically characterised with the output characterisation of the device shown in Figure 7.8. In the representative output plot Figure 7.8A forward current magnitude spans the range -4.85 X 10^{-4}A to -4.55 x 10^{-4}A with the measured drain current at -4V_{DS} plotted with respect to the applied gate potential in Figure 7.8B. The V_{ON} for the device was measured at 0.1mA and graphically extracted and plotted with respect to V_{GS} and is seen in Figure 7.8C. Graphical analysis of the output behaviour of the device suggests no increases in drain current magnitude or changes in V_{ON}, the diode on voltage.

In order to resolve any enhancement current the change in current, ΔI_{DS} was calculated for each output trace with respect to 0V_{GS}. An increase in drain would be a negative magnitude ΔI_{DS} and indicative of enhancement current. A positive ΔI_{DS} is a reduction in forward current at that point on the output trace. The ΔI_{DS} values

were calculated across the $4V_{DS}$ range and plotted on the same axis as the ΔI_{DS} for control devices. For a resolvable change in current to be measured the magnitude of ΔI_{DS} must be outside the variation in control devices. The output traces with their equivalent control traces can be seen in Figure 7.8D, E, F and G for the corresponding gate voltages of $-5V_{GS}$, $-10V_{GS}$, $-20V_{GS}$ and $-30V_{GS}$.

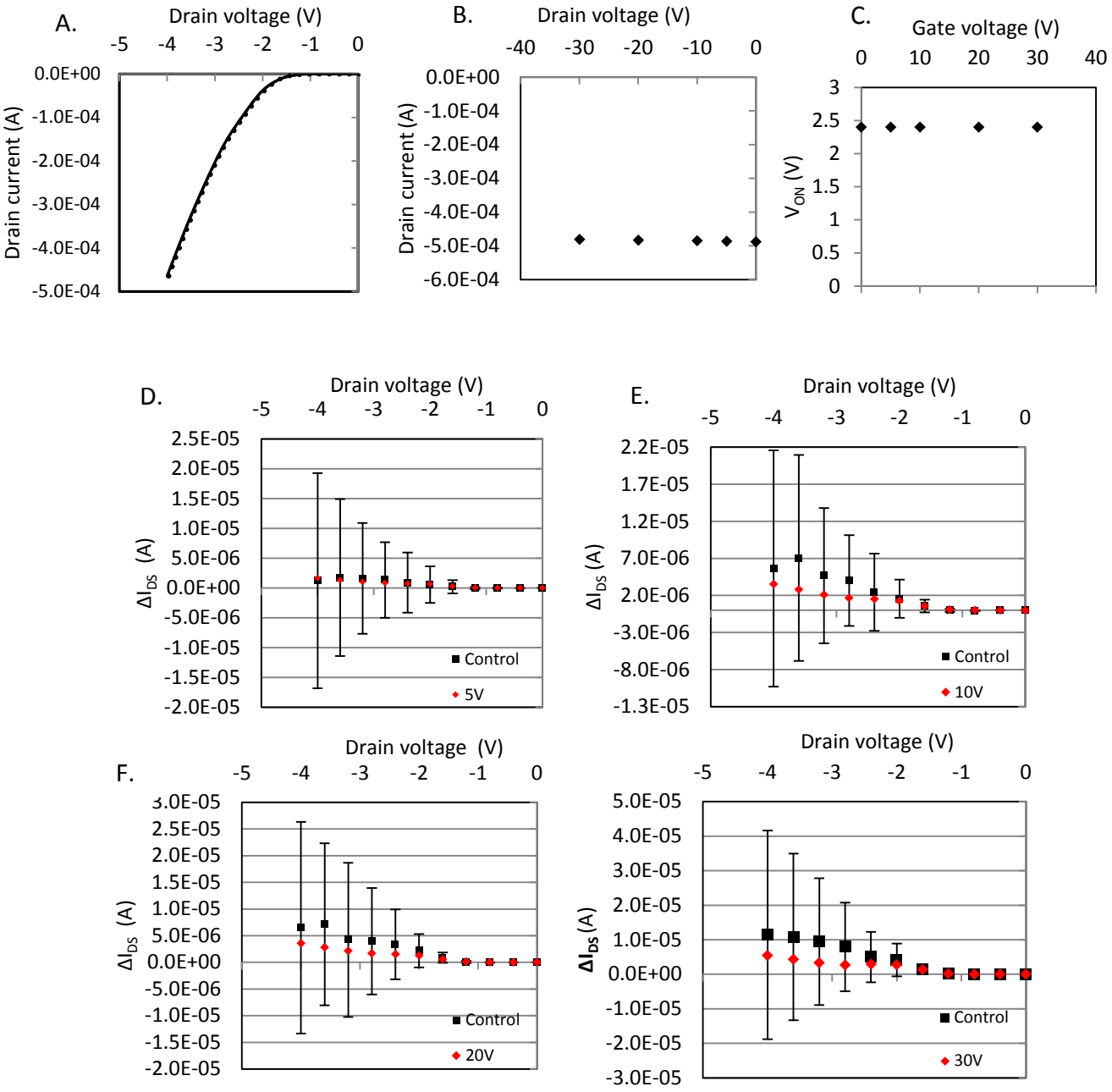

Figure 7.8. Electrical chracterisation of thin film schottky VOFET. A. Forward current output plot under application of a gate potential. B. Measured forward current with respect to applied gate voltage. C. Graphically extracted V_{ON} with respect to applied gate potential. D. Calculated ΔI_{DS} for $-5V_{GS}$ (red diamond) plotted with ΔI_{DS} for equivalent control trace (black square).E. Calculated ΔI_{DS} for $-10V_{GS}$ (red diamond) plotted with ΔI_{DS} for equivalent control trace (black square).F. Calculated ΔI_{DS} for $-20V_{GS}$ (red diamond) plotted with ΔI_{DS} for equivalent control trace (black square). G. Calculated ΔI_{DS} for $-30V_{GS}$ (red diamond) plotted with ΔI_{DS} for equivalent control trace (black square). Errors bars represent the standard deviation for a 68% confidence interval.

The plots of ΔI_{DS} vs. V_{DS} show positive ΔI_{DS} for each output trace across the range $0V_{DS}$ to $-4V_{DS}$.With the ΔI_{DS} magnitude within standard deviation of control devices indicating no enhancement current. In order to observe any time-based behaviour, devices were probed under the gate signals seen in Figure 7.7. The I_{DS} current-voltage behaviour was measured from 0V to -4V during applied $0V_{GS}$ OFF state (black marker) and $-30V_{GS}$ ON state (red marker) gate signal. The normalised drain current magnitude at $-1V_{DS}$, $-2V_{DS}$, $-3V_{DS}$ and $-4V_{DS}$ is seen in Figure 7.9.

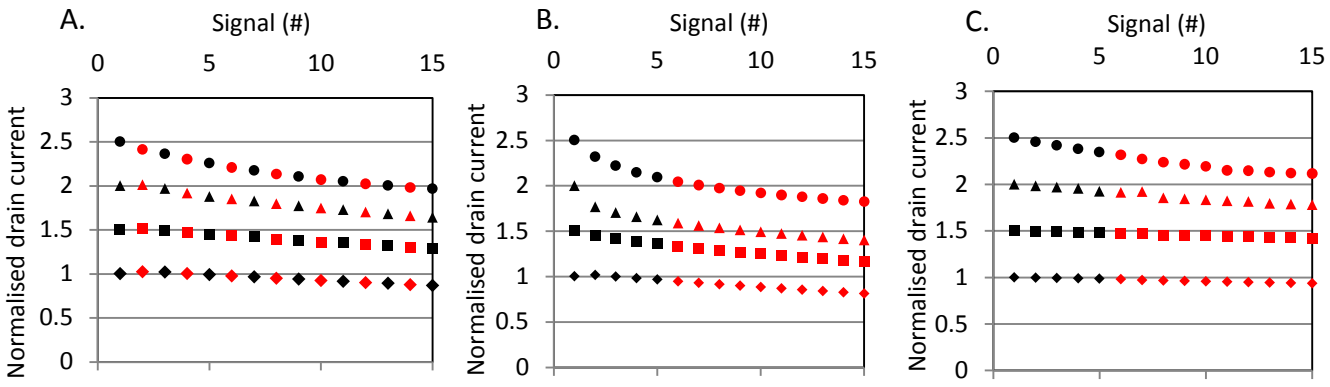

Figure 7.9. Normalised device drain current during applied gate signals A. OFF/ON gate signal input with OFF current (black marker) and ON current (red marker).B. Application of a gate potential, V_{GS}=-30V after five traces C. Application of a gate potential, V_{GD}=-30V after five traces. Each graph has the normalised current for $-4V_{DS}$ (diamond marker), $-3V_{DS}$ (square marker), $-2V_{DS}$ (triangle marker) and $-1V_{DS}$. Normalised currents for $-3V_{DS}$,$-2V_{DS}$ and $-1V_{DS}$ are offset by an interval of 0.5.

Figure 7.9A shows the device switched from an OFF state to an ON state repeatedly and the normalised forward current at $-1V_{DS}$, $-2V_{DS}$, $-3V_{DS}$ and $-4V_{DS}$. Any enhancement would be discerned by an increase in the normalised current during an $-30V_{GS}$ ON state measurement. The drain current of the device show no increases in drain current and trend to lower magnitude with no change under an ON or OFF gate bias consistently across the four V_{DS} potentials. Figure 7.8B shows the behaviour with the device in an OFF state and switching ON through an applied gate potential of $-30V_{GS}$ after five traces. No increases in drain current are observed with switching from the OFF state to the ON state for 10 traces designed to observe a time based enhancement current region being formed within the device.

The field line sketches presented in Figure 7.2D suggests biasing the devices with respect to the drain electrode, V_{GD} may allow for lateral field penetration into the Schottky junction of the device and possible channel enhancement. The alternate biasing regime was examined for enhancement operation with drain current behaviour showed in Figure 7.9C. The deviations in drain current were measured under an applied V_{GD}= -30V with the device going from an OFF state to an ON state after 5 traces. The drain current behaviour shows a strong correlation with the behaviour under an applied V_{GS} with no increases in drain current at an applied gate voltage and drain current trend consistent between the OFF state and ON state measurements.

The trend towards lower drain current magnitudes is consistent with stability testing of devices under output characterisation in §6.3.3 and general ambient testing (Appendix C.3) of P3HT devices and is the result of ambient exposure degrading the electrical properties of the device under repeat testing. The behaviour is described as a time varying series resistance in source-drain equivalent circuit. With the drain current contribution in the device described through a parallel transistor diode circuit with the equivalent circuit for a thin film device presented in Figure 7.10A. The low series resistance of the thin film active layer is potentially masking enhancement current due to high leakage currents. In order to improve the resolvability of possible enhancement current device the active layer thickness was maximised to 20µm with the expected equivalent circuit in Figure 7.9B.

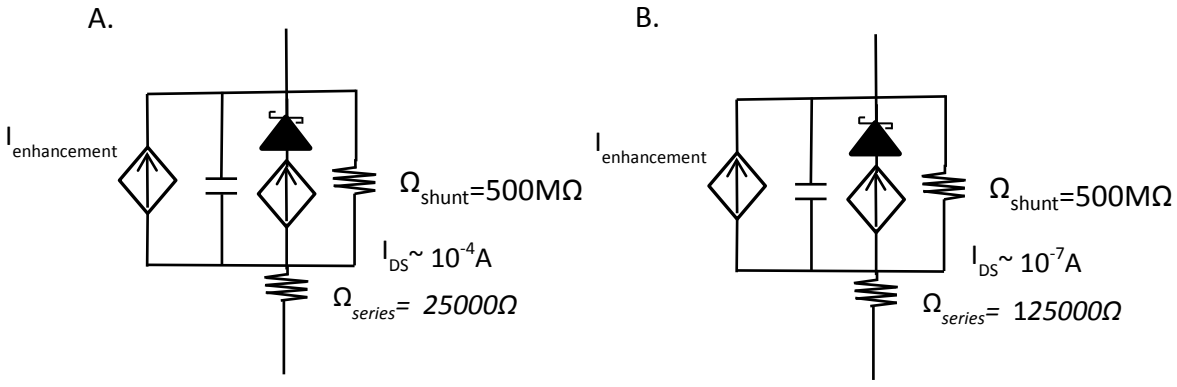

Figure 7.10. Proposed equivalent circuit describing the parallel currents contributing to the drain current. B. Source-drain equivalent circuit for a thin film schottky showing series resistance and OFF state currents. C. Source-drain equivalent circuit with labelled series resistance and OFF state current for drop cast three terminal devices. The current magnitude at -4V_{DS} is used to represent

7.2.3 20µm Active Layer Schottky Barrier VOFETs

A drop cast Schottky barrier VOFET with 20µm active layer was fabricated and electrically characterised and can be seen in Figure 7.11. In the output plot drain current magnitude spans the range -4.0X 10^{-6}A to -2.8 x 10^{-6}A for a 20µm thick active layer and is plotted in Figure 7.11B. A two order reduction in drain currents compared to thin film devices. The V_{ON} for the device was measured at 0.1µA and graphically extracted and plotted with respect to V_{GS} and is seen in Figure 7.11C. The ΔI_{DS} vs. V_{DS} plots with their equivalent control traces can be seen in Figure 7.11D, E, F and G for the corresponding gate voltages of $-5V_{GS}$, $-10V_{GS}$, $-20V_{GS}$ and $-30V_{GS}$.

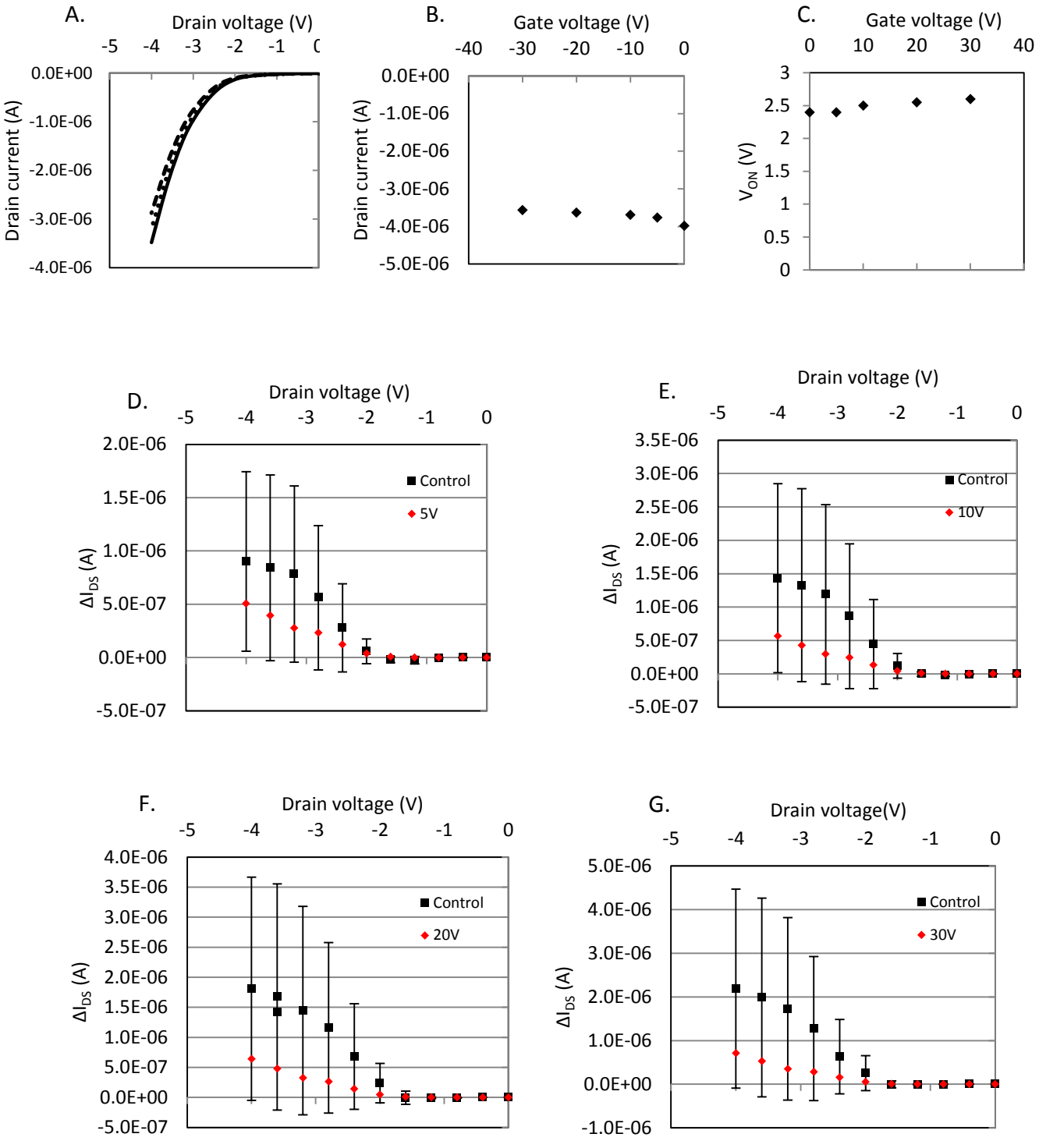

Figure 7.11. Electrical chracterisation of 20µm active layer schottky barrier VOFET. A. Forward current output plot under application of a gate potential. B. Measured forward current with respect to applied gate voltage. C. Graphically extracted V_{ON} with respect to applied gate potential. D. Calculated ΔI_{DS} for $-5V_{GS}$ (red diamond) plotted with ΔI_{DS} for equivalent control trace (black square).E. Calculated ΔI_{DS} for $-10V_{GS}$ (red diamond) plotted with ΔI_{DS} for equivalent control trace (black square).F. Calculated ΔI_{DS} for $-20V_{GS}$ (red diamond) plotted with ΔI_{DS} for equivalent control trace (black square). G. Calculated ΔI_{DS} for $-30V_{GS}$ (red diamond) plotted with ΔI_{DS} for equivalent control trace (black square). Errors bars represent the

The ΔI_{DS} values for each data point were plotted on the same axis as the ΔI_{DS} for equivalent control traces during transistor characterisation. The changes in current show similar behaviour to thin film devices with no ΔI_{DS} point falling beyond the standard deviation of control devices. However, ΔI_{DS} variation in control devices is reduced for all traces when compared to thin film devices. This reduction in the standard deviation between the two gate length structures provides greater scope to resolve device behaviour and is attributed to the reduced current produced by the device.

The structure was probed under varied gate signals with the normalised drain current presented in Figure 7.12. The I_{DS} current-voltage behaviour was measured from $0V_{DS}$ to $-4V_{DS}$ during applied $0V_{GS}$ OFF state and $-30V_{GS}$ ON state gate signals. The normalised drain current magnitude at $-1V_{DS}$, $-2V_{DS}$, $-3V_{DS}$ and $-4V_{DS}$ is seen in Figure 7.12 for the applied gate signals.

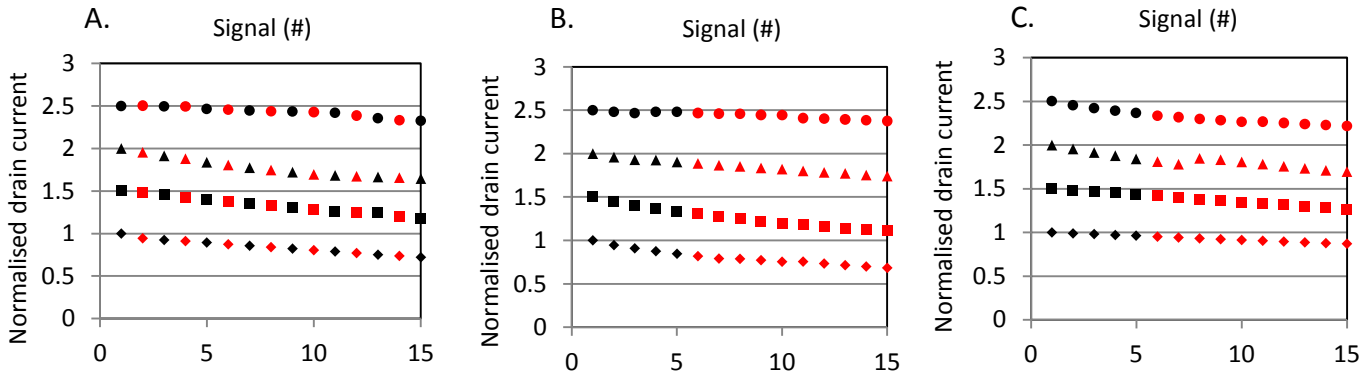

Figure 7.12. Normalised device drain current under applied gate signal for 20µm active layer VOFETs.A. OFF/ON gate signal input with OFF current (black marker) and ON current (red marker).B. Application of a gate potential, V_{GS}=-30V after five C. Application of a gate potential, V_{GD}=-30V after five traces Each graph has the normalised current for $-4V_{DS}$ (diamond marker), $-3V_{DS}$ (square marker), $-2V_{DS}$ (triangle marker) and $-1V_{DS}$. Normalised currents for $-3V_{DS}$,$-2V_{DS}$ and $-1V_{DS}$ are offset by an interval of 0.5.

The behaviour during time based gate signals shows strong correlation with thin film structures. Under all three gate signals drain currents are seen to show a reduction in magnitude across gate input signal. After the application of an ON $-30V_{GS}$ voltage the drain current shows no increase for either structure or biasing

regime. The device performance is consistent with the measured control devices under an applied test cycle in §7.2.1 and ambient processing (seen in Appendix C.3).

P3HT active layer devices show significant variation in control devices reducing the resolution for observing an enhancement current or Schottky barrier lowering during electrical characterisation. This variation is the result of ambient exposure of P3HT and was previously observed during stability testing in §6.3.3 and ambient device testing (supplied in Appendix C.3). As a result, the two terminal leakage current is potentially masking any created enhancement current in the structure. In order to realise transistor behaviour in the structure decreased leakage current and electrical stability is required.

7.3 PCDTBT Active Layer Devices

poly[N-9'-heptadecanyl-2, 7-carbazole-alt-5,5-(4,7-di-2-thienyl-2',1',3'benzothiadiazole (PCDTBT) polymeric material was investigated as the device active layer. PCDTBT is a highly temperature and ambient stable p-type conducting polymer with lower intrinsic conductivity compared to P3HT.[10] PCDTBT has a reported ON/OFF ratio of 10^6 compared to the measured ON/OFF ratio of 10^4 for P3HT.[10] The use of the material as an active layer was investigated with PCDTBT two terminal devices fabricated with 20µm active layer thickness and electrically characterised. The two terminal source-drain behaviour was electrically characterised and is shown in Figure 7.13A.

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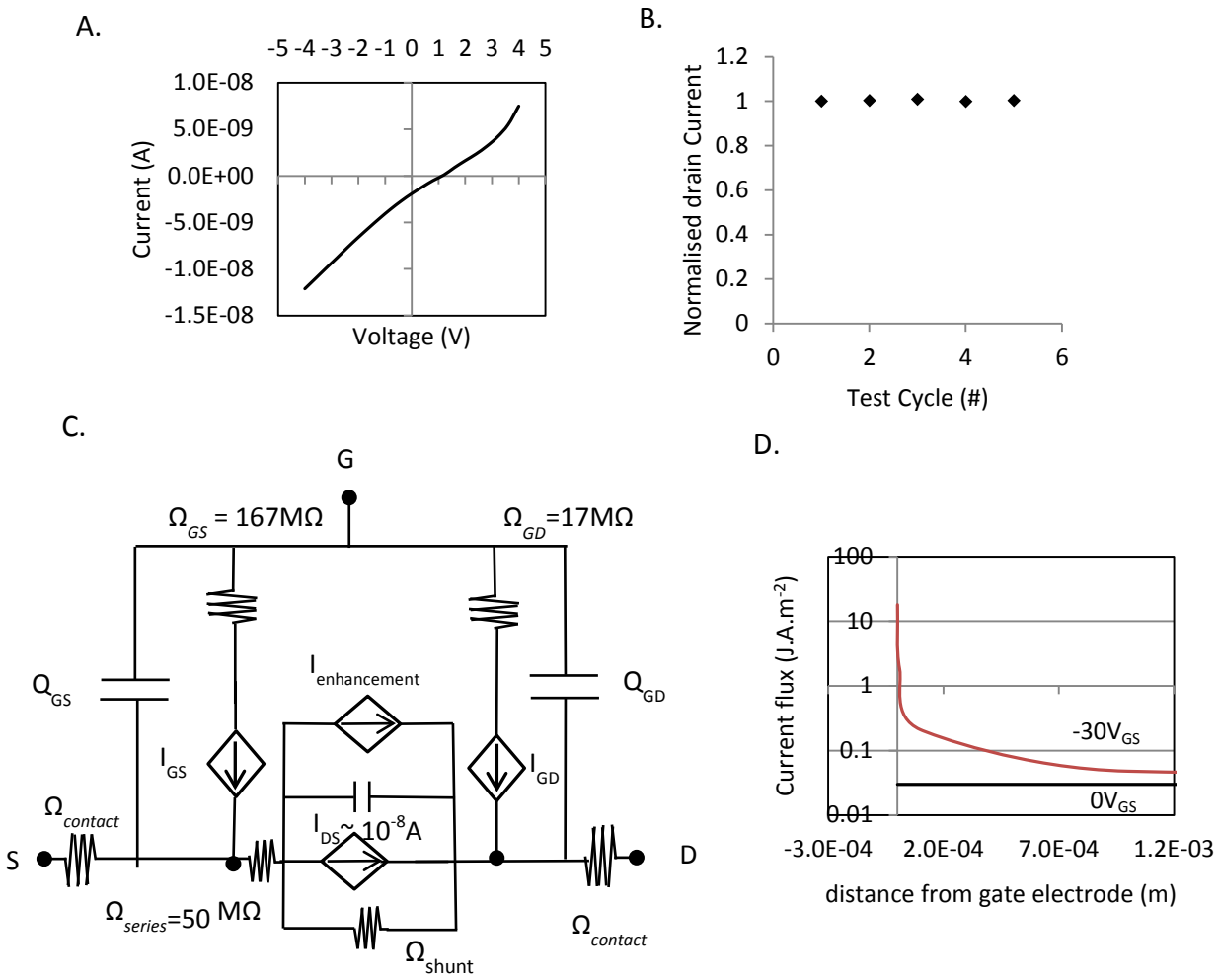


Figure 7.13. A. Proposed equivalent circuit for PCDTBT based OFET devices. B. Source-drain equivalent circuit for a thin film schottky showing series resistance and OFF state currents. C. Source-drain equivalent circuit with labelled series resistance and OFF state current. D. Current flux profile for the active layer at V_{GS}=0V (black line) at an applied V_{GS}= -30V.

Two terminal PCDTBT active layer devices show ohmic charge injection in the -/- quadrant with asymmetric gold-aluminium electrodes. The current is reduced by two orders of magnitude compared to P3HT devices with equivalent device architecture effectively reducing leakage currents. The PCDTBT devices were tested under the transistor output test cycle to act as a control and the can be seen in Figure 7.13B. Completed three terminal PCDTBT devices show excellent stability at the point of testing with no significant deviation in the measured drain current. The

proposed equivalent circuit for the source-drain circuit can be seen in Figure 7.13C. Under incident electric fields the PCDTBT is expected to increase in flux seen in Figure 7.13D. The high stability and low leakage currents make PCDTBT an ideal candidate material to observe enhancement current in the structure.

PCDTBT drop cast devices were tested for transistor behaviour as p-type enhancement mode devices using output plot characterisation and probed under the two gate signals discussed in §7.1.2 . Electrical characterisation for PCDTBT VOFETs can be seen in Figure 7.14.

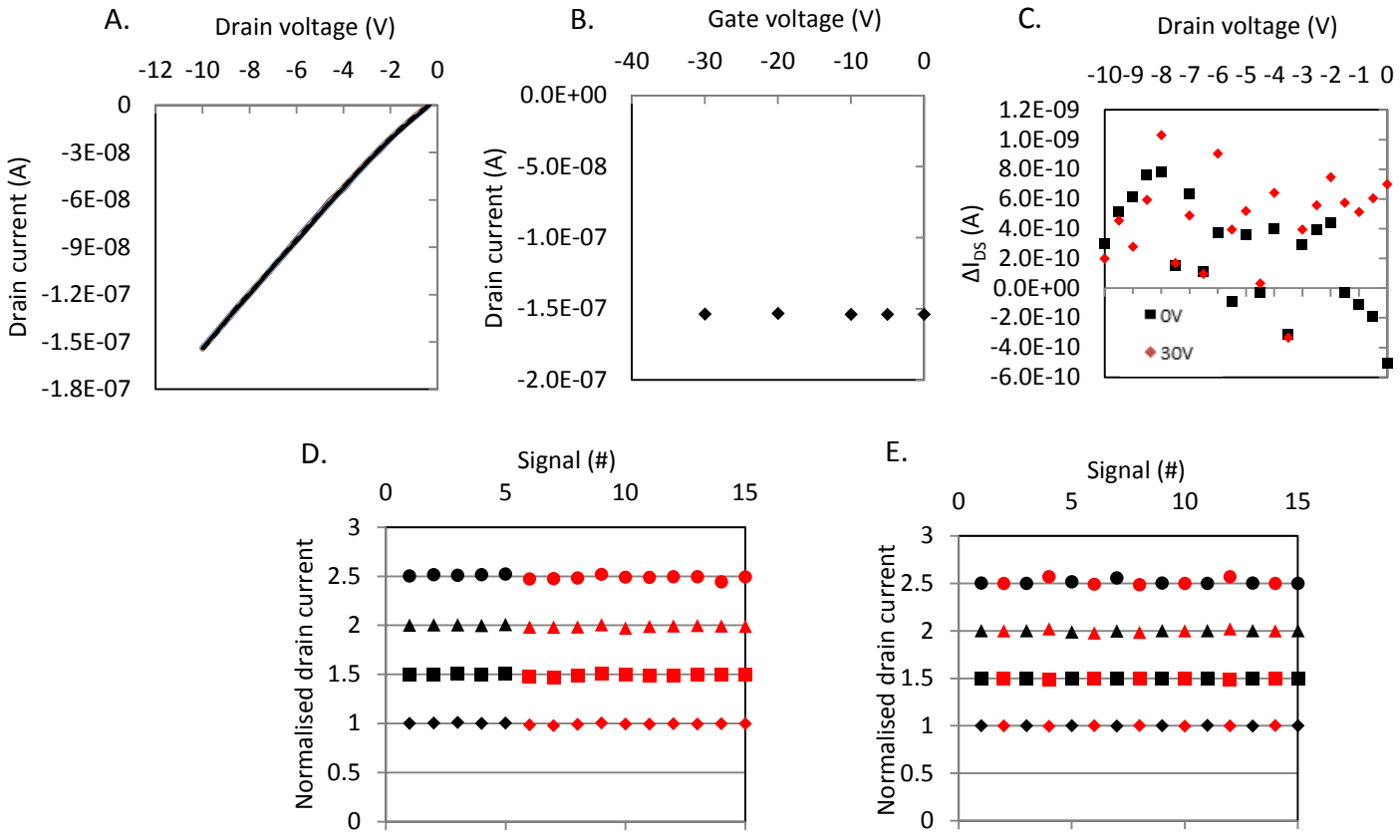


Figure 7.14. Output electrical chracterisation of a PCDTBT VOFET devices. A. Forward current output plot under application of a gate potential. B. Measured forward current with respect to applied gate voltage. C. ΔI_{DS} vs. V_{DS} for $0V_{GS}$(black square) plotted on the same axis as $-30V_{GS}$(red diamond). D. Application of a gate potential, V_{GS}=-30V after five traces with OFF forward current (black marker) ON forward current (red marker) E. OFF/ON gate signal input with OFF current (black marker) and ON current (red marker).

Graphically the output plot for drop cast PCDTBT devices shows no changes to forward quadrant behaviour. The measured drain current at $-10V_{DS}$ for applied gate

potential $5V_{GS}$, $10V_{GS}$, $20V_{GS}$, $30V_{GS}$, is plotted in Figure 7.14B. The ΔI_{DS} for the output plot is plotted for $-30V_{GS}$ on the same axis along with a $0V_{GS}$ trace. Changes between each trace are on the order of a nanoamp. With increasing gate potential the drain current ΔI_{DS} behaviour shows no meaningful negative values. Under time based gate signals the drain current shows no enhancement behaviour. Due to the high stability of the PCDTBT and resulting devices an enhancement current of nanoamps would be resolvable given the magnitude of ΔI_{DS} between successive traces and control samples. However resulting devices show no change in current magnitude correlated with applied gate voltage. The result suggests no enhancement current being generated in the device active layer suggesting poor lateral field penetration into the channel within the device structure.

7.4 Machine Cut Interface

The machine cut interface plays a critical role in device operation forming the capacitive couple at the gate electrode. During machine cutting variations to device architecture were observed and discussed in §5.2. The architectural changes are seen in Figure 7.15 and can be categorised as polymeric adhesion failures resulting in the structure shown in Figure 7.15A or gold adhesion failures resulting in the structure shown in Figure 7.15B. The resulting architecture show deviations from idealised structure that result in changes to the lateral field lines are sketched.

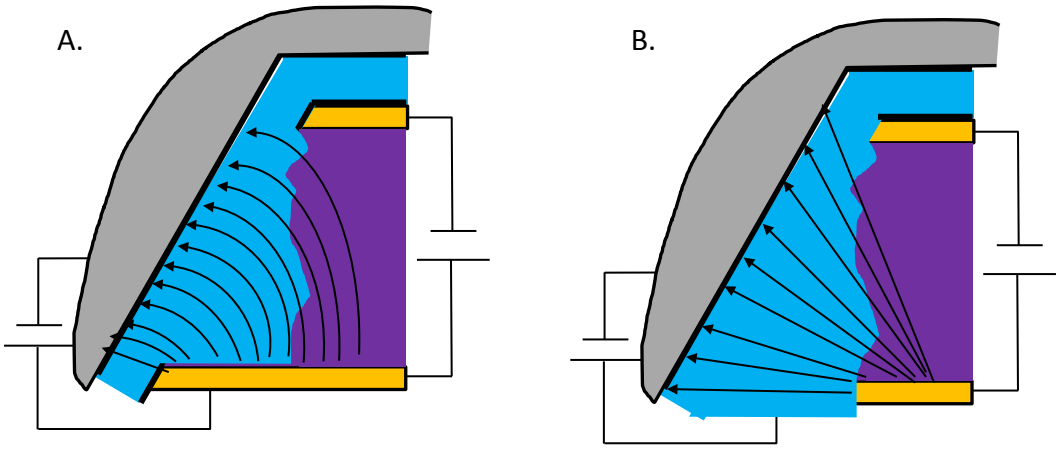


Figure 7.15. A. Polymer delamination at the polymer-gold interface and B. Gold delamination at the gold-polycarbonate interface. The architectures represent deviations from the ideal device architecture resulting innon-ideal lateral electric fields.Schematic depiction of possible lateral electric fields and resulting charges induced at the semiconductor-dielectric interface.

In both instances increases in the thickness of the dielectric are expected. Increasing the thickness of the dielectric film leads to a reduction in lateral electric field magnitude incident into the active layer. Reducing the likelihood of an enhancement current being produced during operation. A further consequence of the lateral friction during machine cutting is tearing of polymeric chains within the P3HT material. The scale of these tears and the resulting topography introduces a roughness at the dielectric-semiconductor interface increasing the gate length of the device.

In 2004 Sirringhaus *et al.*[11] examined the influence of the dielectric-semiconductor interface roughness on device properties. Devices were made using the p-channel polymer poly(9,9-dialkylfluorene-alt-triarylamine) and a 40-60nm cross-linked bisbenzocyclobutene derivative with pre patterned 15nm gold source and drain electrodes with 3nm Cr adhesion layer. The device used poly (3,4-ethylenedioxythiophene):poly(styrene sulfonic acid) (PEDOT:PSS) as a gate electrode. Using vertical phase separation in ternary solutions of the semiconducting polymer, gate-dielectric and solvent self-aligned semiconductor-polymer dielectric bilayers were fabricated within the device. Through varying the speed of the solvent removal roughness at the phase separated interface could be controlled. In Figure 7.16 the effect of interface roughness on the resulting field effect mobility of fabricated devices can be seen for three roughness scales.

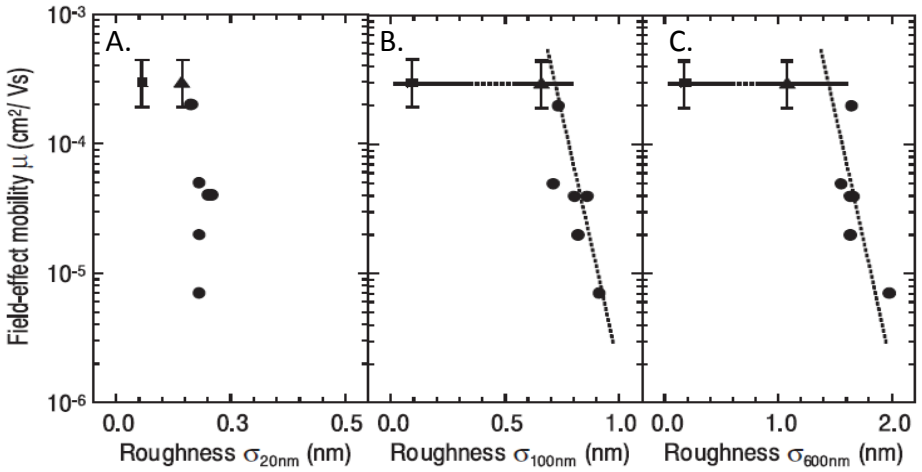


Figure 7.16. Linear regime μ_{FET} with respect to interface roughness over three legnth scales with an evaluated gate field 2-3 $MVcm^{-1}$ as produced by Sirringhaus *et al.*[16] A. δ_{20nm} B. δ_{100nm} C. δ_{600nm}. Straight lines are used as a visual guide of correlation.

Sirringhaus *et al.*[12] found that field effect mobility was constant for low interface roughness values with a critical roughness threshold determined as the point at which μ_{FET} reduces dramatically with respect to roughness, δ.. The work of Sirringhaus *et al.*[12] shows roughness at the semiconductor-dielectric interface in OFETs needs to be limited for device operation and can reach a critical point post which a device may not operate as intended. With the machine cut observed to create lateral damage on the order of microns, the roughness of the resulting interface in three terminal devices post machine cutting is a key issue that needs addressing with further optimisation required.

7.5 Conclusion

A three terminal device architecture featuring an angled machine cut vertical wall was examined for operation as an enhancement type VOFET. The device is seen to produce current on the order of 1 x 10^4 A at -4V using a P3HT semiconducting layer with an operational area up to 2 x $10^{-6}m^2$ achievable. Due to the large operational area a mechanism of operation featuring a Schottky barrier in the equivalent circuit was hypothesised with channel enhancement and field induced barrier lowering simulated as possible modes of operation. Simulation of the structure for two active layer thicknesses- 225nm and 20µm shows a device with an on/off performance of 2 producing enhancement currents on the order 10^{-4}A for 225nm active layer and 10^{-7}A for a 20µm active layer at low voltages. It should be noted the simulation does not account for any possible Schottky barrier lowering which has the scope to greatly improve performance but does show a resolvable enhancement current is possible with the two architectures.

Schottky barrier VOFETs were fabricated with active layer thicknesses on two scales-225nm and 20µm and electrically characterised for enhancement behaviour. The output characterisation showed no graphically observable enhancement or barrier lowering for the device structure. To resolve any enhancement current, the incremental change, ΔI_{DS} between each output curve was calculated and compared

to control devices. The changes in current output for both devices were within standard deviation of control devices. The devices were probed to resolve a time based channel enhancement using two gate signal inputs, a repeat OFF/ON (-$30V_{GS}$/$0V_{GS}$) gate signal and a turn on signal with baseline OFF state for five traces turning the device to an ON state of -$30V_{GS}$ for ten traces. The drain current showed no increases under either time based signal and trended towards lower magnitudes. The trend was consistent with the device stability prior to testing and the general repeat testing of P3HT devices. The resulting standard deviation in control devices, attributed to ambient processing is a key hurdle in resolving transistor behaviour utilising P3HT active layers.

The air stable, low intrinsic conductivity, p-type polymer PCDTBT was introduced as an active layer material and used to fabricate 20µm active layer devices. The devices showed linear current-voltage behaviour replicating a traditional planar p-type OFET. The device structure was electrically characterised and probed using the same analysis as P3HT devices and showed no enhancement current. Ultimately, PCDTBT was capable of resolving an enhancement current on the order of nanoamps and was processed in ambient conditions. However, the result suggests a shortcoming in the device architecture, with the sum lateral electric field not penetrating into the operational area sufficiently to meet simulated expectations.

The machine cut interface and the capacitive couple formed is of critical importance in future investigations. The lack of enhancement current means the lateral electrical field incident on the active layer is not penetrating into the active layer sufficiently to produce an enhancement region. A key shortcoming of the machine cut interface is variations from ideal architecture produced by delamination occurrences during machine cutting resulting in regions with significant dielectric thickness variation and interfacial roughness. Effectively reducing the sum lateral field and not producing a field effect device. Further optimisations to the machine cut interface are necessary to help understand the lateral field penetration depth for the device structure and potential device performance.

References

1. Sirringhaus, H., *25th Anniversary Article: Organic Field-Effect Transistors: The Path Beyond Amorphous Silicon.* Advanced Materials, 2014. **26**(9): p. 1319-1335.
2. Stutzmann, N., R.H. Friend, and H. Sirringhaus, *Self-Aligned, Vertical-Channel, Polymer Field-Effect Transistors.* Science, 2003. **299**(5614): p. 1881-1884.
3. Noh, Y.-Y., et al., *Downscaling of self-aligned, all-printed polymer thin-film transistors.* Nat Nano, 2007. **2**(12): p. 784-789.
4. Li, S.H., et al., *Solution-processed poly(3-hexylthiophene) vertical organic transistor.* Applied Physics Letters, 2008. **93**(21).
5. Ben-Sasson, A.J., et al., *The Mechanism of Operation of Lateral and Vertical Organic Field Effect Transistors.* Israel Journal of Chemistry, 2014. **54**(5-6): p. 568-585.
6. Brutting, W., *Physics of Organic Semiconductors* ed. Wiley. 2006. 554.
7. Yang, F.Y., et al., *High-performance poly(3-hexylthiophene) top-gate transistors incorporating TiO2 nanocomposite dielectrics.* Organic Electronics, 2010. **11**(1): p. 81-88.
8. Yildirim, F.A., et al., *Gate insulators and interface effects in organic thin-film transistors.* Organic Electronics, 2008. **9**(1): p. 70-76.
9. NeŠpůrek, S. and P. Smejtek, *Space-charge limited currents in insulators with the Gaussian distribution of traps.* Czechoslovak Journal of Physics B, 1972. **22**(2): p. 160-175.
10. Cho, S., et al., *A Thermally Stable Semiconducting Polymer.* Advanced Materials, 2010. **22**(11): p. 1253-1257.
11. Sirringhaus, H., *Device Physics of Solution-Processed Organic Field-Effect Transistors.* Advanced Materials, 2005. **17**(20): p. 2411-2425.
12. Chua, L.L., et al., *Observation of Field-Effect Transistor Behavior at Self-Organized Interfaces.* Advanced Materials, 2004. **16**(18): p. 1609-1615.

8. Summary & Conclusion

In order to improve the prospects for organic electronics, a vertical three terminal device was fabricated featuring solution processed functional films and machine cut vertical wall architecture. The platform allows for the deposition of polymer solutions from a variety of solvents to be deposited on plastic substrates with preferable mechanical properties in comparison to silicon. For this to be achieved a UV-NVS resin buffer layer successfully eliminated environmental stress cracking to underlying polycarbonate substrates and produces a surface with favourable wetting for chlorinated solvents allowing for over coating subsequent thin films. With evaporation technology yields on the order of 80% were reached for thin film two terminal polycarbonate devices. This resulted in reliable production of two terminal devices with variable electrode configuration on polycarbonate substrates, the first reported polymeric devices on polycarbonate.

Key to resolving transistor behaviour under characterisation is a stable two terminal equivalent circuit. As such devices were optimised to produce reliable forward current behaviour. Variations in the performance and equivalent circuit were greatest in immediately tested devices. This was shown to produce a changing equivalent circuit up to 150 mins post electrode deposition with device ON/OFF performance improving over that period. Devices stored in vacuum for twenty hours prior to testing show minor changes in the equivalent circuit and improved performance under immediate testing compared to immediately tested devices. The result suggests a time varying series resistance element in the equivalent circuit post electrode deposition due to Schottky barrier formation at the P3HT/Aluminium interface. Highlighting the need for optimised storage and handling of polymeric devices in reliable performance. A statistical analysis of fabricated devices was undertaken resulting in a statistically derived equivalent circuit for the batch processing.

CNC mechanical cutting was used to produce a machine cut through device substrates resulting in a vertical wall capable of being used as an interface in a three

terminal device. Machine cutting resulted in devices with no macro scale damage and consistent electrical performance post processing. Cutter tracking speed was seen to influence the adhesion failures. Adhesion failures were caused by delamination of gold at the gold-substrate interface and polymer at the polymer-gold interface introducing deviations from idealised device architecture. At lower spindle head tracking speeds both adhesion failure mechanisms increase and decrease as spindle head speed was increased. Conductive AFM mapping was used to investigate the cut edge with electrical conductivity observed to the edge of the P3HT material. The resulting conductivity map of the cutting procedure shows torn polymer at the cut edge on the order of microns. However electrical continuity across the material suggests the feasibility of the cutting procedure in creating vertical wall architectures. Solution processing of UV-NVS films across the cut surface was seen to produce a film over the cut edge that proved electrically insulating with a resistance of 167MΩ between gate and source. Resulting in a three terminal device able to be fabricated in ambient conditions with solution processed functional films.

During device fabrication changes to the two-terminal equivalent circuit were observed with two terminal diode devices trending towards reduced forward current behaviour and high on voltages. An encapsulating electrode configuration greatly reduces degradation of device performance during the fabrication of transistor devices featuring the UV cured dielectric film. Any resolvable transistor behaviour is required to be statistically resolvable from the variation of the device post processing.

The device performance was simulated as an enhancement mode device and showed an on/off ratio of 2 and enhancement currents on the order of 10^{-4}A for 225nm active layer device and 10^{-7}A for 20µm devices. However, the fabricated devices with these dimensions showed no observable enhancement in forward current under output characterisation and no statistically significant current change between traces across the output range. In order to resolve a time based enhancement current, time varied gate input signals switching the device from an OFF ($0V_{GS}$) to an ON ($-30V_{GS}$) state were applied to the device and the normalised

drain current measured across the output range. The testing showed no enhancement current under the time based gate signals. Using a lower intrinsic conductivity material such as PCDTBT in the active layer improves the resolvability of an enhancement current. It does this by reducing the parallel two terminal current contribution during device operation with PCDTBT device featuring leakage currents on the order of 10^{-8}A. Displaying ohmic injection the PCDTBT devices showed excellent stability under ambient condition with stability on the order of nA between traces. PCDTBT devices with 20μm active layer thickness were electrically characterised and showed no enhancement current.

Due to the low variation and electrical stability of PCDTBT the device structure was ultimately capable of resolving an enhancement current on the order nanoamps. Under varied gate lengths and active layer material composition the structure did not produce resolvable enhancement current.. Due to the large operational area of the device a key question is the penetration depth of the electric field produced by the gate and incident onto the device operational area with the polymeric active layer attenuating the field as neither a metal nor insulator. With simulations suggesting the electric field was sufficient to produce a resolvable enhancement current the device shortcomings appear to be related to the semiconductor-dielectric interface. Reported literature shows interface roughness on the order of nanometres sufficient to reduce field effect mobility and device performance. The roughness of the machine cut polymer is unclear, however lateral tears have been observed across the interface. These tears and adhesion failures Introduce deviations to the device architecture across the semiconductor dielectric interface producing variable thickness of the solution processed dielectric layer and deviations from ideal device geometry resulting in a reduced sum lateral electric field. New cutting technologies that result in low roughness cut surfaces or improvement of the existing cut surface would help realise the structure further.[4-6]

Secondly, a larger lateral field magnitude could be achieved through scaling of the dielectric functional film or use of high dielectric constant dielectric materials. Atomic layer deposition has been shown to create conformal dielectric films of high

capacitance materials such hafnium oxide at thickness on the order of nanometres.[1-3] While this may not lead to an optimised device in itself, it may overcome interface factors and lead to an operational device. Despite the relatively high cost of atomic layer deposition due to precursor gases and vacuum deposition necessary it would provide further fundamental insight into the structure feasibility. As it stands, improving the machine cut and the resulting interface and dielectric scaling are immediate opportunities to increase the sum lateral electric field and realise a three terminal field effect device within the structure.

References

1. Ou-Yang, W., et al., *High-performance organic transistors with high-k dielectrics: A comparative study on solution-processed single crystals and vacuum-deposited polycrystalline films of 2,9-didecyl-dinaphtho[2,3-b:2[prime],3[prime]-f]thieno[3,2-b]thiophene.* Applied Physics Letters, 2012. **101**(22): p. 223304.
2. Chung, Y., et al., *Low-voltage and short-channel pentacene field-effect transistors with top-contact geometry using parylene-C shadow masks.* Applied Physics Letters, 2010. **96**(13): p. 133306.
3. Gusev, E.P., et al., *Ultrathin HfO2 films grown on silicon by atomic layer deposition for advanced gate dielectrics applications.* Microelectronic Engineering, 2003. **69**(2–4): p. 145-151.
4. NOMURA, M., et al., *Study on Micro End Milling Using Precise Cutting Force Measurement.*
5. Nomura, M., et al. *Study on Machining Accuracy in Micro-Endmilling*. in *Key Engineering Materials*. 2012. Trans Tech Publ.
6. Kumeria, T., L. Parkinson, and D. Losic, *A nanoporous interferometric micro-sensor for biomedical detection of volatile sulphur compounds.* Nanoscale research letters, 2011. **6**(1): p. 1.

Appendix A. Physical Chemistry of Two Terminal Devices on Polycarbonate Substrate

A.1. Spin Coated P3HT Thickness

Controlling the thickness of the P3HT layer will provide a means to reduce the gate length and scale the device architecture. AFM was used to measure the film thickness of P3HT films obtained from prepared films with varying spin speed from 100RPM- 3000RPM. Films were prepared on glass slides on top of a 30nm gold layer. A scalpel was used to scratch the film and create a step height over which the film thickness could be could be measured using the AFM height image cross section. Operating in tapping mode, the AFM was used to image over the scratch height and measured the displacement between the top of the cut and the bottom of the cut, providing a value for the step height and the thickness of the film. An example step height measurement is seen below in Figure A.1.

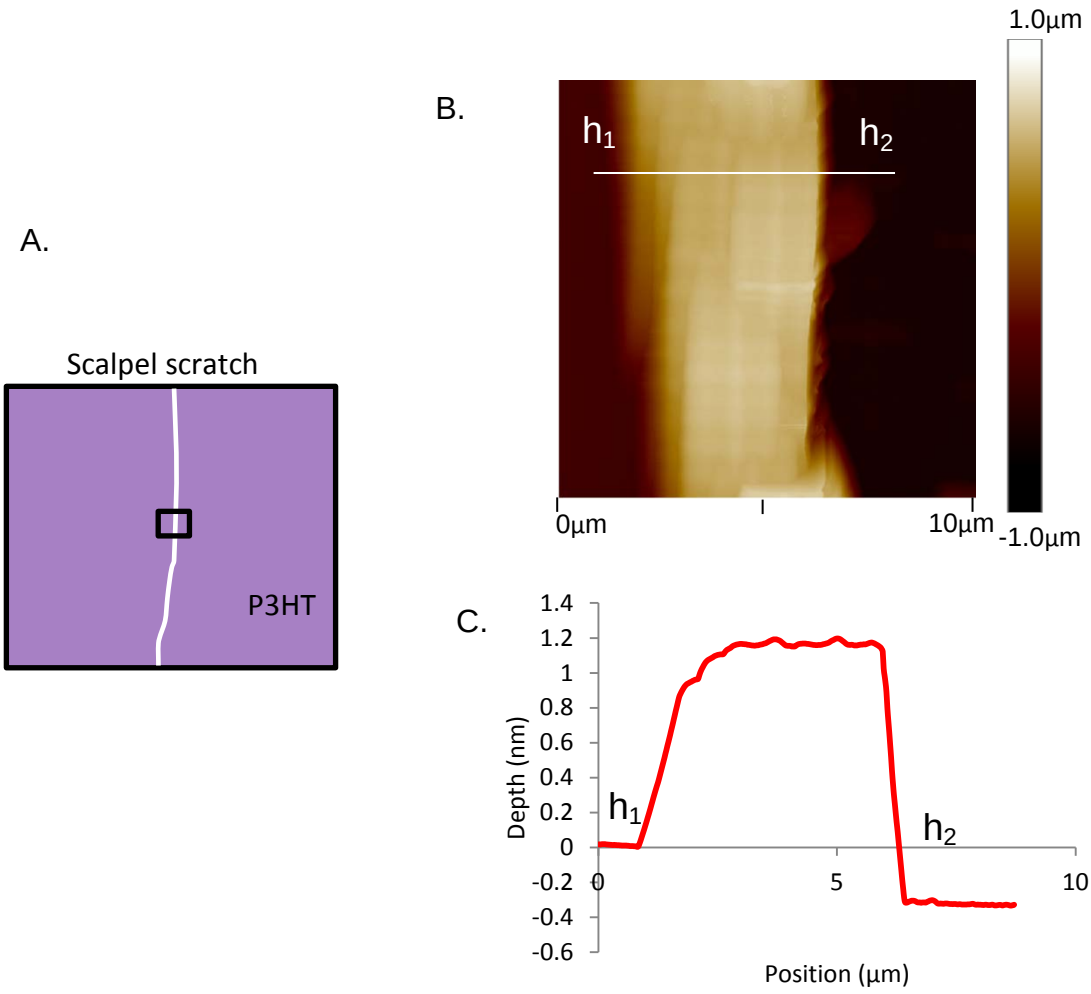


Figure A.1.Example of P3HT step height calculation. A. Schematic of scratched sample. B. Example height profile obtained across scalpel cut. C. 2D section analysis showing step height (nm) vs. position analysis. A step height of 276nm was obtained in this example.

The Three step height were calculated for each sample with 5 spin speeds being tested- 100RPM, 500RPM, 1000RPM, 2000RPM and 3000RPM. The spin speed curve for two solvents- 1,2- dichlorobenzene and Toluene were measured over this range and the thickness compared. The thickness measured for films under varied spin speed is presented in Figure 3.12.

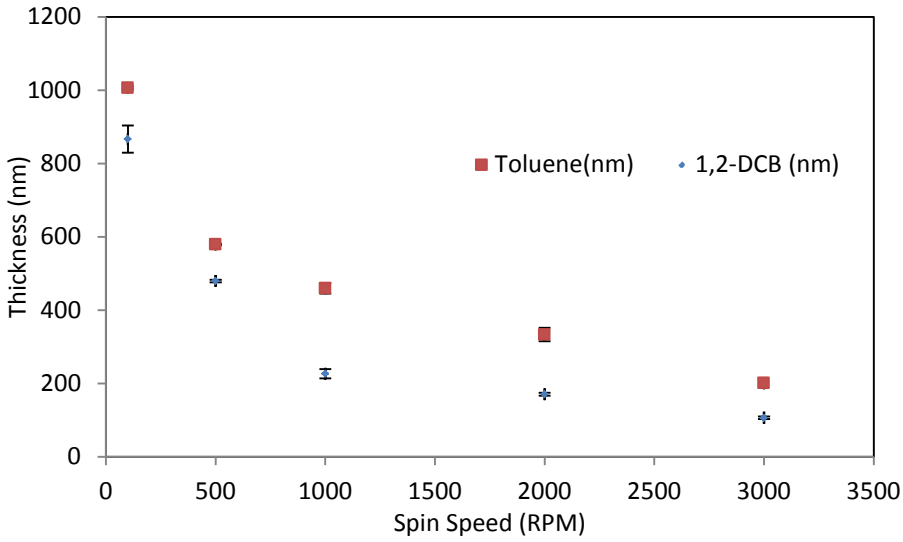


Figure A.2. Plot of measured film thickness (nm) vs. spin speed (RPM) for P3HT thin films prepared using 3% w/v 1,2- dichlorobenzene solvent (red dot) and toluene (blue dot). Error bars are the relative error calculated over three trials.

With increasing spin speed the thickness of the films is reduced when both toluene and 1,2 –DCB is used as the solvent. With spin speed curves showing a parabolic trend with film thickness increasing rapidly as spin speed reduces below 1000RPM. To determine the thickness of drop cast films, drop cast films were prepared by pipetting a controlled volume on a glass slide with 30nm gold layer. 10µL of solution was dropped on the surface and allowed to dry in Nitrogen environment. Samples were snap frozen in liquid nitrogen and mounted perpendicularly on a custom scanning electron microscope (SEM) sample mount and the cross section was imaged for solutions drop cast out of 1,2-dichlorobenzene and Toluene. Three locations where the interface was free from glass debris were chosen and value averaged. Films created by the drop casting of polymer solution were seen to be 18.3 ± 2.6 µm for films prepared using 1,2- dichlorobenzene. Whilst films prepared using Toluene solvent had a thickness of 21.8 ± 3.4 µm. Drop cast SEM images are presented further in Appendix A.2.Through varying the spin speeds and the method of deposition a range of P3HT thicknesses from 200nm through to several microns was achieved. The controlled deposition of varying thicknesses of polymer film allows the study of various gate length device configurations in a vertical, out-of plane device architecture.

A.2. Drop Cast Film Thicknesses

The thickness of drop cast films was probed through scanning electron microscope and showed a visible contrast between the glass slide and drop cast film. Using the scale bars was used to obtain a measure of drop cast film thickness. However, It must also be considered that the sample is sitting with an inherent angle, masking a portion of the interface. Due to these factors a clear image of the film interface is difficult to achieve, drop cast films are on the order of several microns. The cross section of a drop cast P3HT aliquot on glass side is seen in Figure A.3.

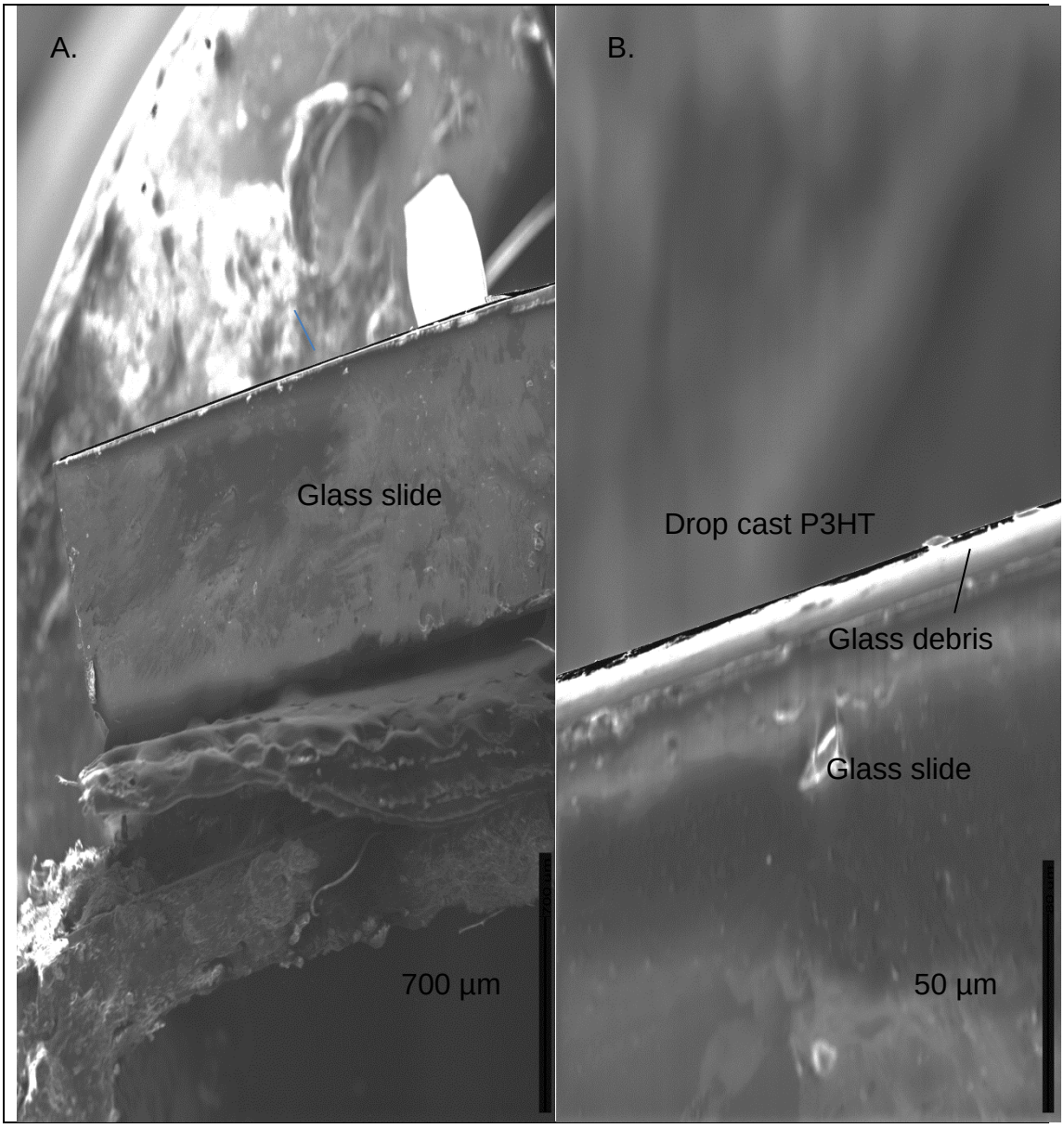


Figure A.3 – Cross section SEM images of drop cast 30mg/mL P3HT films on liquid nitrogen snapped glass slide.

A.3. Influence of Processing on Wetting of Working Electrodes

A quantitative understanding of the wetting properties is key to the preparation of thin polymeric films and can be obtained through contact angle measurement. A measurement of the angle between a liquid droplet (typically water) and substrate at the three phase (solid, liquid, and atmosphere) interface provides a measure of the materials contact angle. A contact angle < 90 ^{o} corresponds to a hydrophilic or wettable surface, a contact angle > 90 ^{o} corresponds to a hydrophobic poorly wetting surface. [1] This study aims to establish the contact angle and wetting of gold thin films under two conditions- cleaned gold prepared by cleaning in Pyroneg solution at 70°C for 30mins followed by rinsing in de-ionised water followed by reagent grade Ethanol and evaporated gold that has not been cleaned and was as deposited. An understanding of the behaviour of the two different gold systems will allow for the improvement of handling procedure allowing for the immediate spin coating of polymer films onto gold electrode after deposition. Figure A.4 shows the comparison between measured contact angle with respect to time for measurements conducted on cleaned (blue dots) and evaporated (red dots) gold thin films with water droplet.

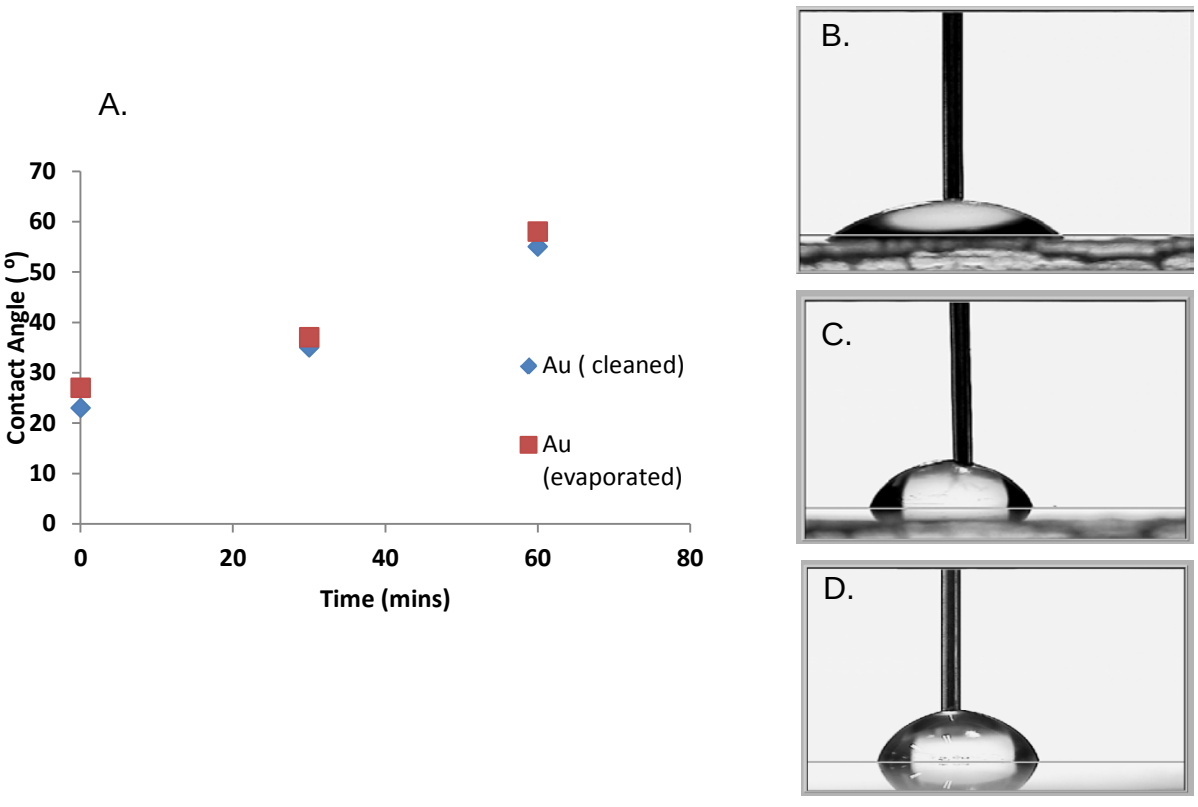


Figure A.4. Contact angle vs. time for evaporated (blue dots) and evaporated (red dots) gold samples. Example digital capture of obtained contact angle droplets for A. 1,2-DCB on cleaned Au after 30mins. B. 1,2-DCB on UV-NVS cleaned surface after 60mins C. Pyroneg cleaned UV-NVS with water D. Cleaned Au with water droplet.

Cleaned gold samples show an initial contact angle of 23^{o} indicating a hydrophilic surface. Evaporated films show an initial contact angle of 29^{o} also indicating a hydrophilic surface. Over the 60 min period the contact angles were seen to increase for both systems. With a contact angle of 35^{o} for cleaned gold compared to evaporated gold which had a contact angle of 37^{o}. Over the 60min experimental period the contact angle of cleaned gold was seen to further increase to 45^{o} with evaporated gold rising to 48^{o}. Both samples- cleaned gold and as deposited gold were seen to increase over the trial period whilst showing very similar contact angle. This suggests that s evaporated gold films produces clean, wettable surfaces. And that a cleaning step is not necessary for devices to immediately be solution processed after metal deposition.

Appendix B. Schottky Device Parameter Extraction and Simulation of Equivalent Circuits.

B.1. Parameter Extraction

Beginning his work on electron emission from metals in 1901, Owen Richardson observed the temperature assisted emission of bound electrons from a metal. Whereby bound electrons when provided kinetic energy via light radiation were seen to breach the energy barrier to the vacuum level emitting from the material, discovering the photoelectric effect.[2] The release of bound electrons was seen to be related to the amount of thermal kinetic energy incident on the sample and with increasing thermal energy the amount of electrons emitted increased.[3]

A mathematical model incorporating field- enhanced thermionic emission was later developed from Richardson's work to explain the electric field assisted emission of charges from electron guns, known as Schottky emission. The Schottky emission model is used to describe the current-voltage behaviour over a potential barrier assisted by an electric field.

The field enhanced- thermion emission model was the basis for the Shockley ideal diode equation, named after William Shockley which allowed the extraction of a barrier height through examination of the saturation current shown in Equation B.1.

$$\boldsymbol{I = I_0 \exp(\frac{V}{nkT})} \qquad \text{Equation B.1}$$

With I = drain current (A), I_0 = reverse saturation current (A), V= potential difference (V), n= ideality, k= Boltzmann constant and T= temperature.

The equation for the reverse saturation current, I_o is provided by:

$$\boldsymbol{I_0 = A\, A^{**} T^2 \exp(-\frac{q\varphi_B}{kT})} \qquad \text{Equation B.2}$$

With A= cross sectional area (cm^2) A** = Richardson constant for a free electron= 120 $A/cm^2\ K^2$, and $\boldsymbol{\varphi_B}$ = potential barrier height (eV).

Through the ln I vs. V plot and extrapolation to the origin a value for the barrier height can be obtained when the temperature, Richardson constant, majority carrier and area are known. The linear segment of the ln I vs. V plot is extrapolated over a domain kT/q< < V << IR to obtain a barrier height at the intersection of the y-axis. The empirical use of the Richardson constant in current-voltage characteristics was first examined in 1965 by Crowell[4] and showed the role of interface properties, crystal alignment and temperature had on calculating the barrier height. A 1% error in device variables could lead to a 30% error in the Richardson constant suggesting poor validity with high variability in examined devices. In 1979 Norde further developed parameter extraction based on the laws developed by Richardson which allowed improved reproducibility over a range of device resistances and allowed barrier height from non-ideal diodes with high series resistance. [5] Norde developed a mathematical function using a modified version of the field enhanced thermionic emission model Shockley equation to account for series resistance seen in Equation B.3 and B.4.

$$\boldsymbol{I = I_0 \exp(\frac{V-IR}{nkT})} \qquad \text{Equation B.3}$$

$$F(V) = \frac{V}{2} - \frac{1}{\beta} \ln\left(\frac{I}{A\,A^{**}T^2}\right)$$ Equation B.4

In 1985 Yasamura et.al showed how the Norde function can be used to determine series resistance along with a barrier height over a range of ideality values through the Norde function.[6] In 1986 Cheung et.al [7] showed an approach to use a single forward current-voltage trace to determine series resistance, barrier height and ideality from modification of the original Norde Function.

This work hopes to achieve an understanding of device parameters- ideality and series resistance through the simulation of a proposed device equivalent circuit. The development of a circuit simulation provides a tool to examine and predict the behaviour of our devices in real world application. And in the development of a three terminal electrical platform provides a lumped sum element to be introduced into an equivalent circuit for a three terminal equivalent circuit. Furthermore, experimental current-voltage traces can be fitted to a simulated data, linking the behaviour of laboratory devices to an equivalent circuit. Through the simulation a current-voltage trace can be fitted to obtained experimental data. Through the fitting values equivalent circuit elements can be obtained and evaluated. This approach allows for a real world tool that can be expanded as required to describe further future devices built with this platform.

Numerical simulation has been used to probe the inhomogeneity of the Schottky barrier and the variations from the thermionic emission model, [8] and field effect dependent mobilities via Monte Carlo simulation.[9]

B.2. Simulation

Simulating programme with integrated circuit emphasis (SPICE) is an open source simulation language utilised for circuit simulation of integrated circuits with extensive use in integrated circuit fabrication, electrical engineering and physical sciences. SPICE was developed in 1973 at Harvard University by Professor Donald O. Pederson. In 1971 Pederson et.al had issued lead the development of Computer

Analysis of Nonlinear Circuits, Excluding Radiation (CANCER) the precursor to SPICE to allow the analysis of circuit transient behaviour through nodal analysis. [10]CANCER was an open access program that utilised non-linear systems of equation from resulting nodal analysis to simulate the time dependent response from a circuit. The on-going evolution of CANCER resulted in the SPICE programming language which has become an open source tool for the study and fabrication of integrated circuits and has been modified and incorporated into simulation programs for study in semiconductor devices,[11] organic electronics[12] and nanotechnology.[13] One such program is National Instruments Multisim 9.0, a graphic based simulation suite that features SPICE as its simulation algorithm.

B.3 Computational Algorithm Overview

A flow chart for the procedural solving of a SPICE circuit through iterative simulation is presented below in Figure B.1.

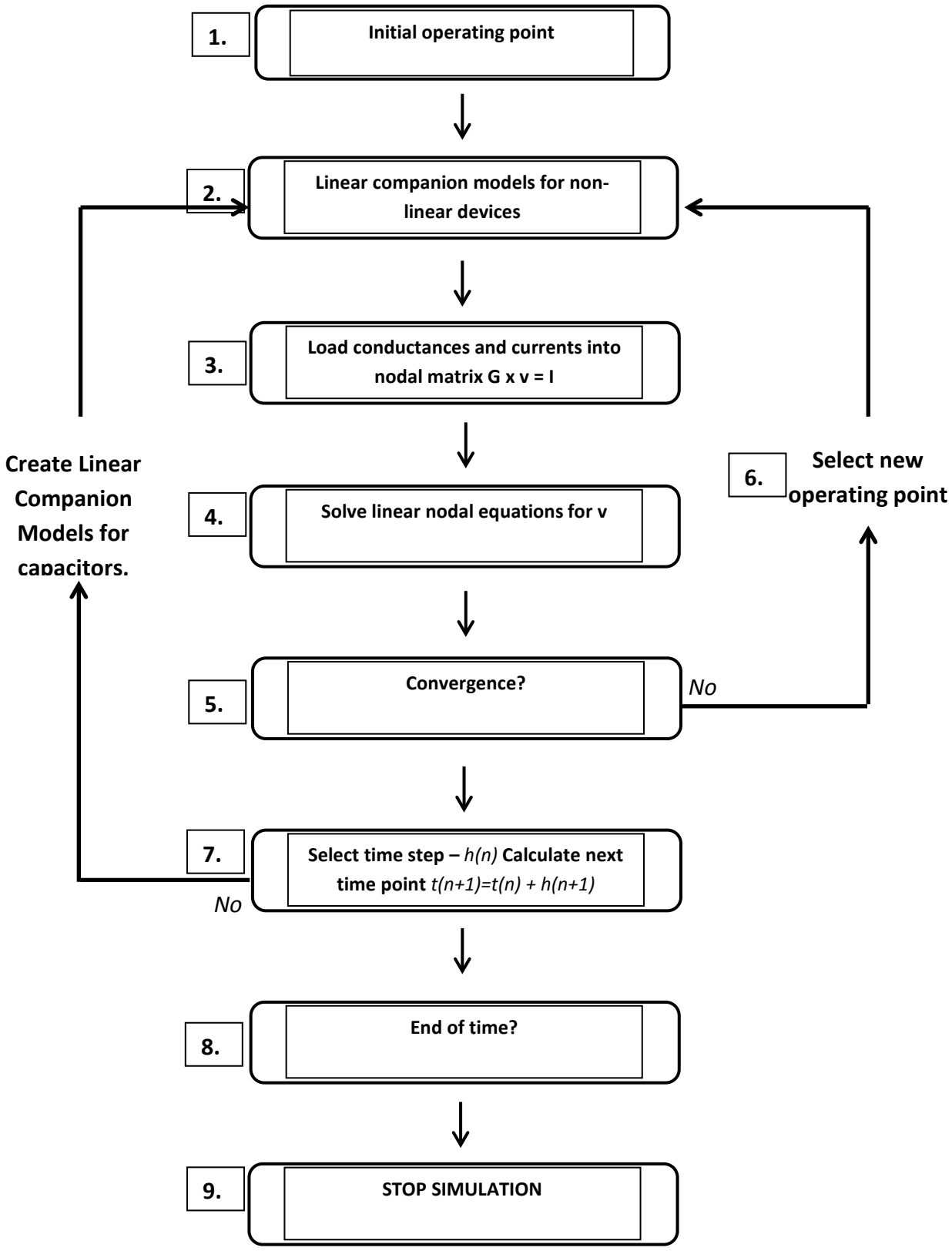


Figure B.1. SPICE computational flow chart describing the nodal analysis undertaken in a transient analysis and the iteration steps for determining a complete time analysis.

The computational algorithm proceeds by setting an initial operating point voltage for nodal elements in the circuit. Linear companion equations are generated and describe the behaviour of non-linear circuit elements (energy storage elements such as capacitance and inductance) at the operating point. Nodal analysis proceeds across steps 3-4 with a nodal matrix G where nodal equations are solved for the circuit voltages across nodal points within the circuit. Steps 2-6 show the iteration process for a solution to the non-linear circuit equations, within a ±0.1% tolerance or ±6pA error of convergence conditions to establish nodal operating voltages throughout the circuit.

The work undertaken in this thesis focuses on the response of an electrical circuit in response to time. A programmed input signal that varies over time allows for accurately replicating laboratory-based voltage ramps used for testing. A time based transient analysis is performed through the combination of the inner loop (steps 2-6) and the time step iteration loop (steps 7-9) to create equivalent linear models for non-linear elements. Linear circuits are simulated through the use of the outer loop, bypassing blocks 2 and 5. After determining the initial operating voltage energy storage components are transformed into linear models for solving through the nodal matrix.

B.4 Multisim 9.0

Multisim 9.0 is an electronic schematic capture environment capable of circuit simulation through the SPICE algorithm. A graphics user interface (GUI) allows the user to construct a circuit schematic visually utilising a database of electronic components. The response is then simulated through the SPICE algorithm. The Multisim schematic used to evaluate the equivalent circuit presented in Figure B.2.

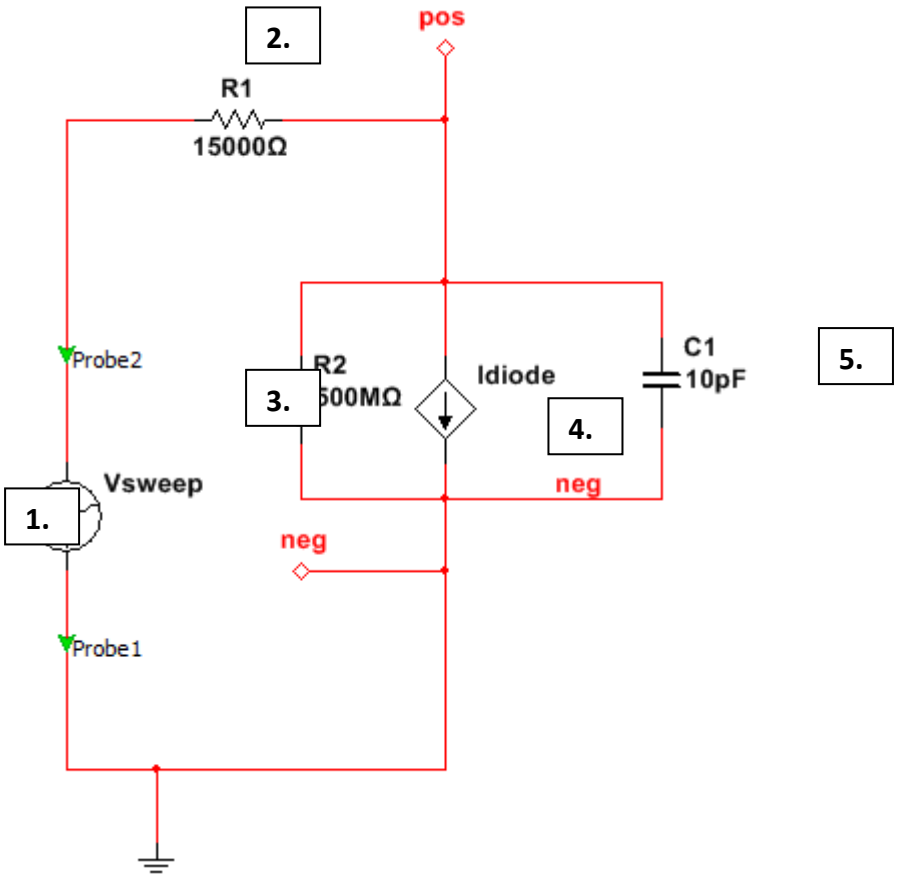


Figure B.2. Multisim 9.0 electronic circuit schematic for Schottky diode with functional elements labelled 1. Piecewise linear voltage, 2. Resistor 3. Resistor 4. ABM current source. 5. Capacitor.

The schematic consists of 5 functional elements

1. Piecewise linear voltage (volts): Allows for the input of custom voltage sweeps that can be broken down into linear segments with respect to time. The use of this element allows for the simulation of ramps as they were used in laboratory experimental data.
2. Series resistor, Ω_{series} (ohm) an element representing the contact resistance and channel resistance.
3. Parallel resistor, Ω_{shunt} (ohm) an element allowing for the shunt resistance to be evaluated.
4. ABM current source: A current source representing the Schottky diode. Based on the thermionic emission and Shockley ideal diode law seen in Equation 3.2. With a value for the reverse saturation bias set to $1 \times 10^{-12} A$.

5. Parallel capacitor, $cap_{junction}$ (farad): A capacitive element representing the junction capacitance.

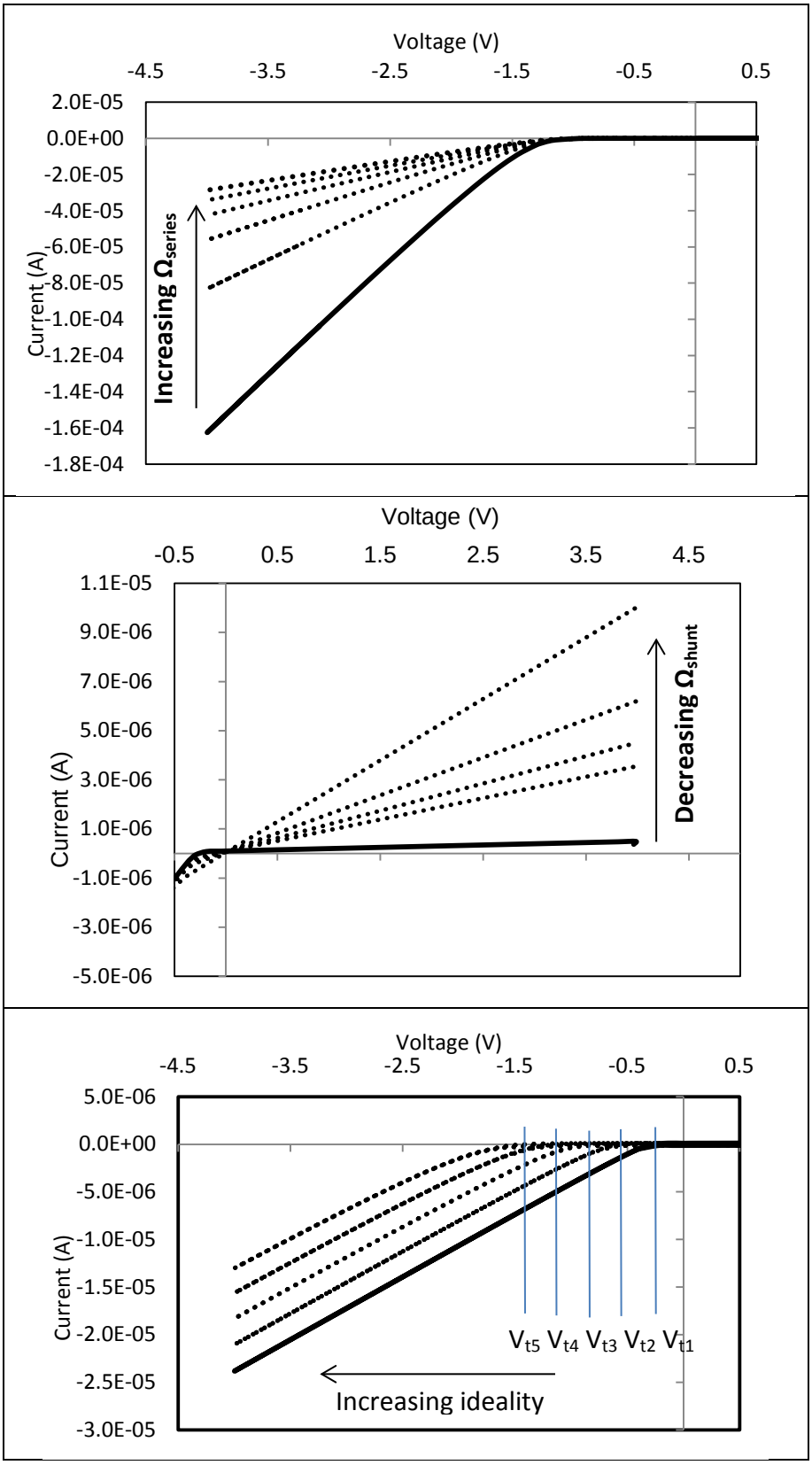
By introducing an ideal diode element into the equivalent circuit it allows for the simulation of voltage-current response and the influence of series resistance Ω_{series}, ideality *n* , shunt resistance Ω_{shunt} and capacitance $cap_{junction}$ on current-voltage characteristics.

B.6 Understanding Diode Equivalent Circuit

The Multisim schematic in Figure B.2 was used to better understand device variables on current voltage response. The simulation schematic allows the magnitude for components to be set and for a current-voltage trace to be obtained. Measuring current-voltage traces with simulated physical device variables. Equivalent circuit variables series resistance Ω_{series}, shunt resistance Ω_{shunt}, ideality *n* and capacitance $cap_{junction}$ values were input and current-voltage curves simulated. Transient analysis was performed with a programmed input signal providing a (+) to (-) 4 volt linear ramp taking 8s for the sweep resulting in a voltage ramp of 1V/s (Piecewise linear voltage Figure B.2 Element 1).

Series resistance was studied through varying the series resistor element Ω_{series} (Figure B.2 Element 2). Series resistance Ω_{series} was varied over the range 15kΩ-90 kΩ to observe the influence of series resistance on forward current in two terminal devices. Figure B.3A. shows the influence of a changing series resistance Ω_{series} with Ω_{shunt}, *n* , $cap_{junction}$ kept constant. Shunt resistance was varied through the parallel resistor Ω_{shunt} (Figure B.2 Element 5) over a range of 0.25MΩ-10 MΩ with Ω_{series}, *n* and $cap_{junction}$ kept constant. The ideality term was varied in the ABM current source (Figure B.2Element 4) with the ideality term in the current equation (Equation 3.7) being simulated over the range n= 1 to n= 5 in 0.5 increments. The parallel capacitance was varied through the parallel capacitor (Figure B.2 Element 5) over 0F to 100nF and studied through a hysteresis sweep. Figure B.3 shows the simulated

current-voltage characteristics with varied series resistance, ideality and shunt resistance generated through simulation of the proposed equivalent circuit.



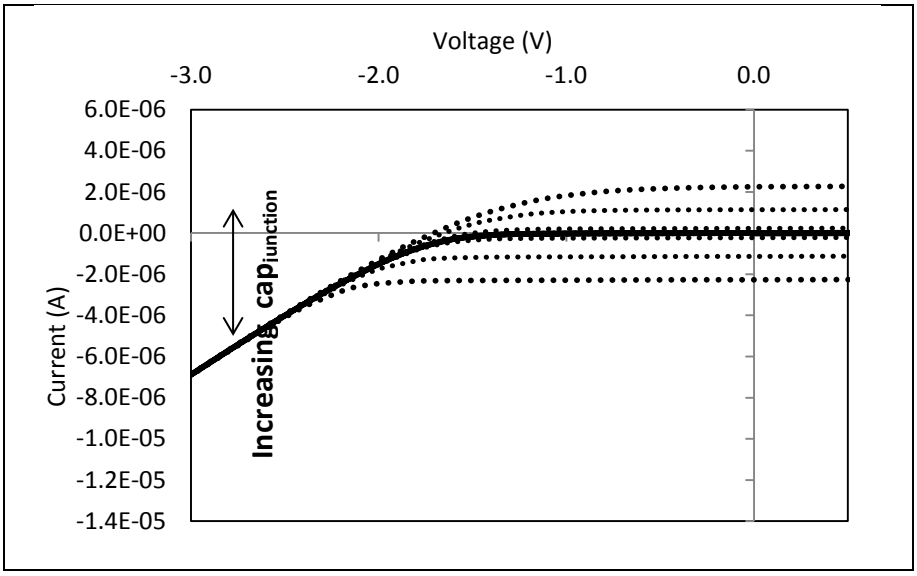


Figure B.3. Simulated current-voltage traces. A. Influence of ideality on current-voltage characteristic. B. Influence of shunt resistance on current-voltage characteristic. C. Influence of series resistance on current voltage characteristic. D. Influence of junction capacitance on current voltage characteristic.

Through simulation over a range of series resistance forward current is seen to decrease with increasing series resistance and can be seen in Figure B.3A. Over the series resistance range 15kΩ-90 kΩ the forward current (-/- quadrant) is seen to be -1.6 x 10^{-4} A at 15kΩ to -3 x 10^{-5}A at 90 kΩ. The effect of an increase in series resistance on forward current is plotted Figure B.4. The relationship between forward current and series resistance is seen to be non-linear.

The simulation of shunt resistance over the range 0.25-10MΩ is seen in Figure B.3B. The shunt resistance is seen to have no impact on forward current values. However with an increasing shunt resistance the magnitude of the reverse current is seen to reduce. At 0.25 MΩ a reverse current of 1 x 10^{-5}A is simulated decreasing to 5 x 10^{-7}A at 10 MΩ.

The simulation of ideality over the range *n*=1 to *n*=5 is seen in B.3C. A changing ideality term sees forward current curves shift towards larger voltages across the x-axis. This result is an increase threshold voltage (V_t) with increasing ideality. The role of ideality in forward current is plotted in Figure B.4A. With increasing ideality the forward current values are seen to increase linearly over the range *n*=1 to *n*=- 5.

The simulation of junction capacitance over the range 0F to 100nF is seen in Figure B.3D. Increase in capacitance sees forward current remain consistent at high voltages. However at the origin an increasing in capacitance can be seen with an increase in non-zero current. The direction of the sweep is seen to play a role in the sign of the non-zero current with sweeps (+) to (-) in direction resulting in an increased positive current and sweeps (-) to (+) showing an increasing negative current at 0V with increasing capacitance.

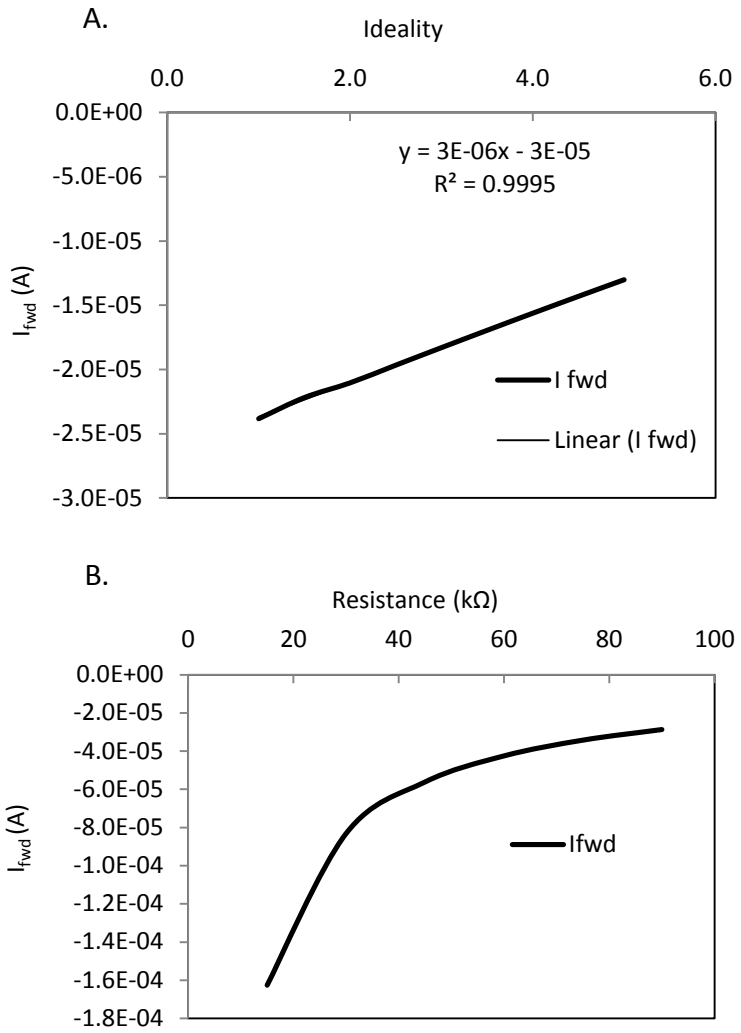


Figure B.4. Plotted forward current relationship A. I_{fwd} vs. ideality *n* and B. I_{fwd} vs. Ω_{series}. A linear regression fit is used in A.

Series resistance, capacitance, shunt resistance and ideality are seen to play a part in the shape and magnitude of forward and reverse currents in current-voltage

behaviour. Being able to simulate experimental current-voltage traces will allow a value for the series resistance, shunt resistance, capacitance and ideality to be obtained. The procedure for fitting a simulated result with an experimental result will be shown along with a means to provide a quality of fit for the fitted data with the experimental data will be shown.

B.7. Curve Fitting and Quality of Fit.

Through the fitting of simulated current-voltage traces with real world experimental traces an equivalent circuit that describes experimental data is obtained. In order to measure the validity of a simulated fitting a metric by which the fitted current-voltage traces can be compared to experimental traces is required. Two numeric approaches were used- Pearson's chi squared test and the Microsoft Excel correlation function. Simulated current-voltage values were exported into Microsoft Excel and allowed for direct comparison. A variation of Pearson's chi squared seen in Equation B.7 produced a fit measure between a simulated and experimentally obtained trace.

$$r^2 = \sum_{i=1}^{n} \frac{(O_i - E_i)^2}{E_i} \qquad \text{Equation B.7}$$

With, O_i = simulated current, E_i= experimental current.

For two sets of current-voltage data, the value for the simulated O_i is directly compared to the experimental result E_i and summed over the entire data set**.** The summed result provided a measure of the curve fit. With the lower the number, the better the obtained fit. The Excel correlation function is described below in Equation 3.8.

$$Correl\,(x, y) = \frac{\sum(x-\bar{x})(y-\bar{y})}{\sqrt{\sum(x-\bar{x})^2 \sum(y-\bar{y})^2}} \qquad \text{Equation B.8}$$

With $\bar{x}$ the mean value of the measured array x, and $\bar{y}$ the mean value of the array y.

In combination, Pearson's chi-squared and the correlation functions are used to provide an evaluation of the quality of fit of the simulated current-voltage response to the simulated response of a proposed equivalent circuit. Through ensuring a high quality of fit equivalent circuit variables can be extracted and used for the evaluation of experimental data.

Appendix C. Device Electrical Characterisation and Testing

C.1 Probe Contact Station Statistics

Table 4.1 shows the percentage of devices that were scratched resulting in the loss of electrical contact for devices measured the probe contact station and the previous testing arrangement.

Table C.1. Percentage of electrodes damaged

Testing	**Electrode failure %**
Previous Testing	20
Probe Contact Station	4

Devices tested using the probe contact station would experience electrode damage that prevented electrical testing in 4% of devices tested. The electrodes appear scratched and to restore electrical contact conductive paste was used to build up the electrode. Previous attempts to test devices encountered 20% loss of devices to electrode scratching. The probe station was seen to improve the losses during testing of samples and improved the testing protocol of this work.

C.2 Influence of testing period on Annealed Devices.

The effect of the testing period between each electrical trace on vacuum rested devices was studied to determine the influence of repeated testing on forward current variation. Vacuum rested devices were transferred into inert atmosphere for testing and allowed to rest for 30mins to provide as little fluctuation as possible. To fully determine the influence of the period of testing six devices were electrically tested under each testing period and the forward current variation measured as the difference between the forward current at the beginning and end of the testing experiment. The average variation in forward current with respect to the period of testing is seen below in Figure 4.16.

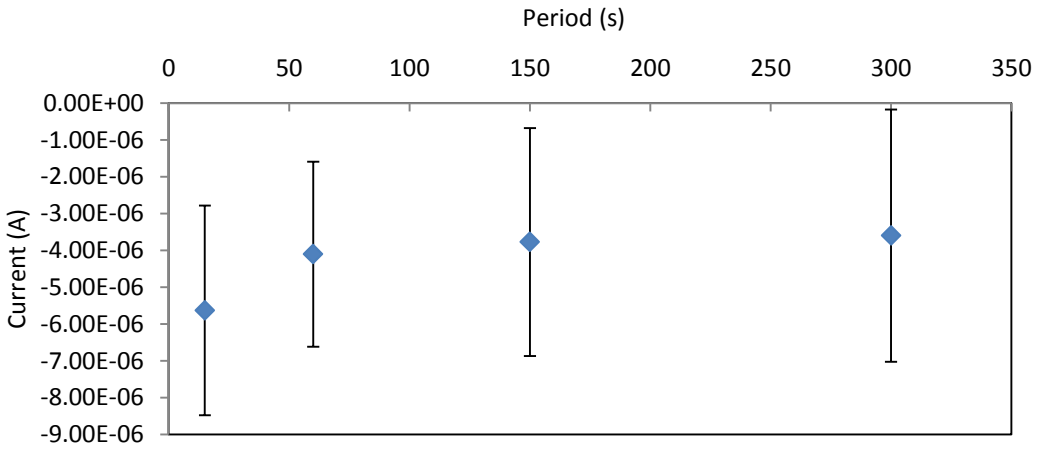


Figure C.1. Forward current variation with respect to trace period. Error bars represent stand error.

Devices show a variation in the range of -5.63x 10^{-6} A to -3.6 x 10^{-6} A. These values correspond to approximately 1% of total current over the 30min period of testing. The role of the testing period seems to be irrelevant in influencing the forward current in these devices.

This result suggests that the period of testing contribution potentially less than 1% to total currents and is a small contributor to the run to run variation in these devices. A period of 15s allows for greater data acquisition and potentially reduces the role of various exposures when testing in transistor configuration and as such is

seen as an appropriate period. The role of period of testing and the influence of transistor curves will be re-evaluated later in this work.

C.3 P3HT Device testing under ambient conditions

The stability of devices under ambient testing was examined. A two terminal substrates is exposed and a discrete device on the substrate measured after exposure times of 1, 4, 8 and 20 hours exposure to ambient atmosphere. A 60min stress test was performed to replicate device testing in which devices were tested every 60 seconds for 1 hour over the range ± 4V. The traces for each device are measured and then compared to measure deviation between the electrical characteristics due to testing conditions. The forward current change across the experiment for each exposure period is plotted over the test period with the initial measurement after exposure (referred to as 0min) and the final trace in the 60min characterisation (referred to as 60min) and presented in Figure C.2.

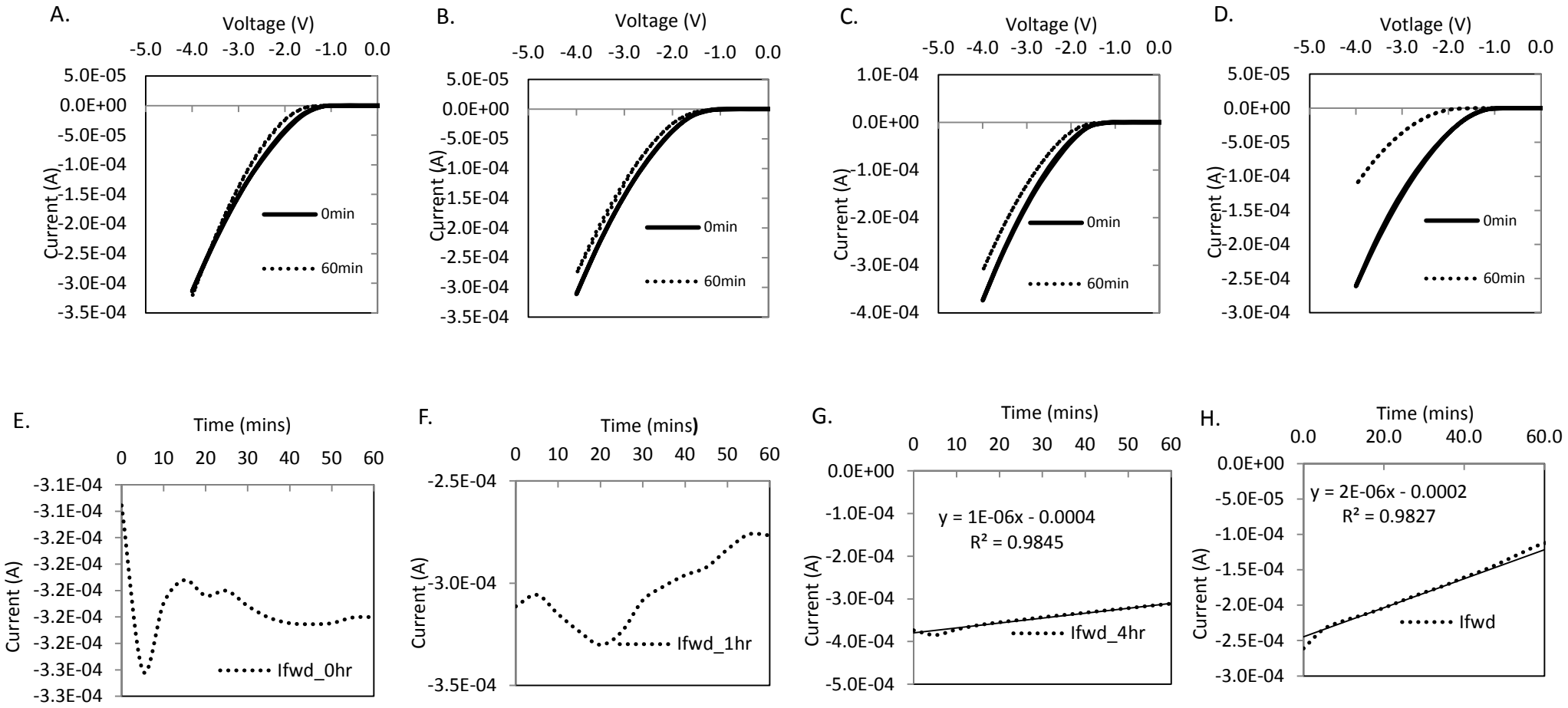


Figure C.2. 60min device stress test in ambient conditions showing forward current electrical characterisation after ambient exposure. A. Initial 60 min stress test B. 60min stress test after 1 hour ambient exposure C. 60min stress test after 4 hours ambient exposure D. 60min stress test after 20 hour ambient exposure. Forward current trend during the 60min stress test period. E. Initial 60 min device stress test. F. 60 min stress test after 1 hour exposure stress test G. 60min stress test after 4 hour exposure stress test. H. 60 min stress test after 20 hours exposure.

A general trend can be seen in the changes occurring during stress testing. Shifts in forward current characteristic shape with the threshold voltage shifting towards higher voltages characteristic of ta change in diode ideality and a reduction in current can be seen to occur. At 0hr an ideality factor shift of Δn= 0.3 is seen to occur, however the forward current total remains comparable with the initial value seen in Figure C.2A. After 1 hour exposure a reduction in forward current from -3.1 x 10^{-4} A to -2.8 x 10^{-4} A over the testing period is measured and can be seen in Figure C.2B along with an increasing shift of the curve to larger diode on voltage with an ideality factor shift Δn= 0.35. After 4 hours exposure a reduction in forward current from -3.7 to -3.1 x 10^{-4} A over the testing period is measured and can be seen in Figure C.2C. The observed ideality shift is calculated to be Δn= 0.55. After 20 hours exposure a reduction in forward current from -2.6 to -1.1 x 10^{-4} A over the testing period is measured and can be seen in Figure C.2D.

The observed ideality shift is calculated to be Δn= 1.8. The shift in ideality factor over the stress testing period is graphed with respect to exposure time and can be seen in Figure C.3.

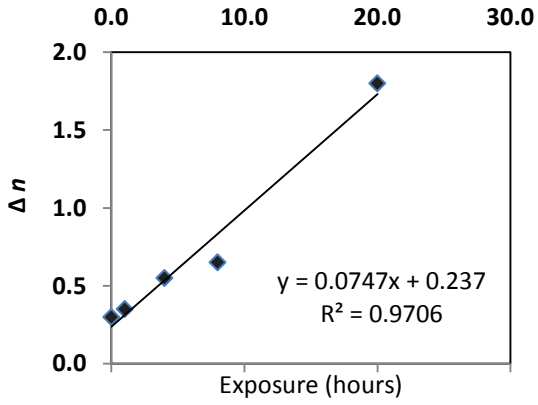


Figure C.3. Shift in the ideality factor with respect to exposure time. A linear fit is applied to the data and a regression r^2= 0.97 calculated.

The change in ideality factor over the testing period is seen to increase with increasing exposure time. A strong correlation with a linear fit is observed. Extrapolating the equation of fit *y= mx + c* with *m=* slope of the line the rate of change in the ideality factor during a repeated testing block is calculated to be 0.07Δn.hr^{-1} exposure to ambient conditions.

This trend follows the simulated expectations of an ideality shift. Testing in ambient condition shows once devices have been exposed for long enough the principal degradation method is a shifting ideality and reduction in forward currents during testing.

C.4 Space Charge Limited Currents in Two Terminal Devices

When the intrinsic conductivity of a material is exceeded under electrical conduction injected charges will form a space charge region and deviations from ohmic conduction occur. In 1972 Smetjek *et al.*[14] described the mechanics for space charge current emission for an insulating material with a Gaussian trap energy-voltage distribution. [14] Smetjek *et al.*[14] show that under space charge emission the current voltage relationship precedes $I \alpha V^n$. With n dependent on the temperature and the width of the Gaussian trap states. It has been reported an electric field on the order of 1×10^5 $V.cm^{-1}$ will result in space charge limited current in P3HT polymeric devices.[15] Figure C.4 calculates the magnitude of the electric field over a range of applied potential voltage under film thicknesses resulting from two terminal processing using the sequential processing methodology.

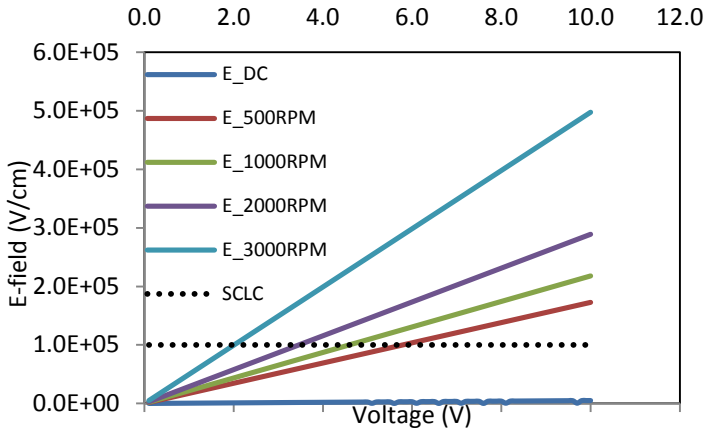


Figure C.4. Calculated electric field strength with respect applied potential voltage. The electric field strength is calculated using thickness measurements acquired in §3.X.X. The electric field is calculated for several thicknesses drop cast film of thickness ~20µm (dark blue line). 500RPM spun cast films of thickness 479.6nm ± 3.51nm (red line). 1000RPM spun cast films of thickness 276.4nm± 2.51nm (green line). 2000RPM spun cast films of thickness 170.1nm ± 17.7nm (purple line). 3000RPM spun cast of thickness 106.2nm ± 3.2nm (light blue line). The electric field strength of 1×10^5 $V.cm^{-1}$ is labelled as a dotted line.

A dotted line shows the electric field strength of 1 x 10^5 V.cm^{-1}. The intercept between the dotted line and the trace for a selected thickness will provide a calculated value in which the two terminal device conducting channel will be space charge current limited. Devices with a film thickness of 106.2nm ± 3.2nm (light blue line) had a calculated space charge regime of 1.9V. Devices with a film thickness of 276.4nm± 2.51nm (green line) had a calculated space charge regime of 4.6 V. Devices with a film thickness of 479.6nm ± 3.51nm (red line) had a calculated space charge regime of 5.8V. Drop cast films with a film thickness on the order of 20µm were not forecast to become space charge limited within the range 0V-10V. Graphical extrapolation of the Log J vs. Log V characteristic can be used to determine the charge injection regime.[16-18] calculated space charge limited voltage was compared with measured current-voltage traces. The Log J vs. Log V curves for current-voltage traces are shown below in Figure C. 5.

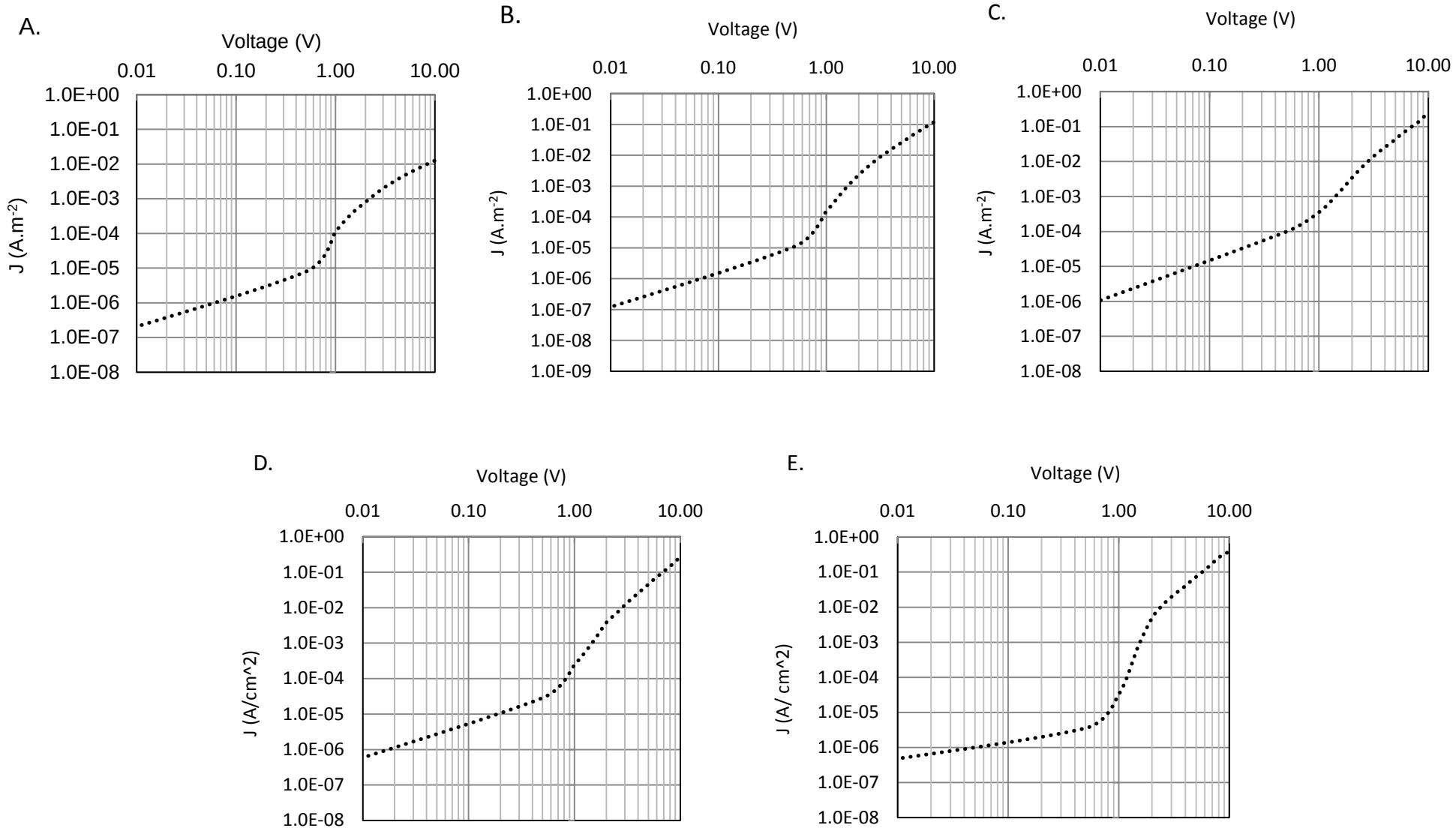


Figure C.5. log J vs. log V plots for Schottky barrier devices with varied active material thickness .A. Drop coat B. 500 RPM C. 1000RPM D. 2000 RPM. E. 3000RPM.

Observing the Log J vs. Log V curves in Figure C.5 three regimes can be distinguished at high spin speeds. At low voltages < 0.7V an ohmic relationship I α V is observed across all thicknesses. At V.0.7 V current increases quickly with the relationship I α V^m. Beyond this an inflection point can be observed most prominently graphical analysis was used to extract the space charge voltage regime for experimental current voltage traces.

C.5 Time Based Device Performance

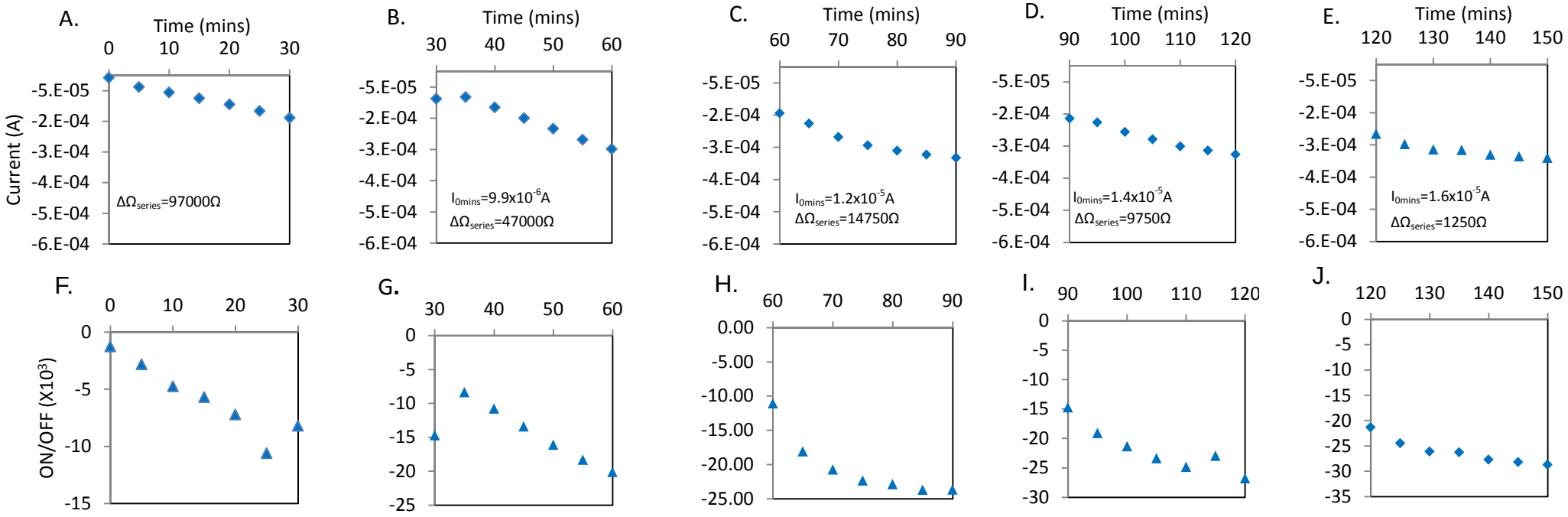


Figure C.6. Forward current increases in newly minted devices as a function of time over 30mins of testing. A. Forward current over 30mins after electrode deposition. Forward current over 30mins for a device 30mins after electrode deposition. C. Forward current over 30mins for a device 60mins after electrode deposition. D. Forward current over 30mins for a device 90mins after electrode deposition. E. Forward current over 30mins for a device 120mins after electrode deposition. The corresponding ON/OFF performance is presented in F,G,H,I and J respectively.

Table C.3- extracted series resistance over the course of the experiment

	I_{0min} (A)	n_{0min}	Ωseries $_{start}$ (Ω)	I_{30min} (A)	n_{30min}	Ωseries $_{finish}$ (Ω)	ΔΩseries (Ω)
Dev1	-3.6E-05	2.8	125000	-1.4E-04	2.8	28000	97000
Dev2	-8.7E-05	2.8	62000	-2.5E-04	2.8	15000	47000
Dev3	-1.4E-04	2.8	28000	-2.8E-04	2.8	13250	14750
Dev4	-1.6E-04	2.8	23500	-2.8E-04	2.8	13750	9750
Dev5	-4.8E-04	2.8	10000	-6.6E-04	2.8	8750	1250

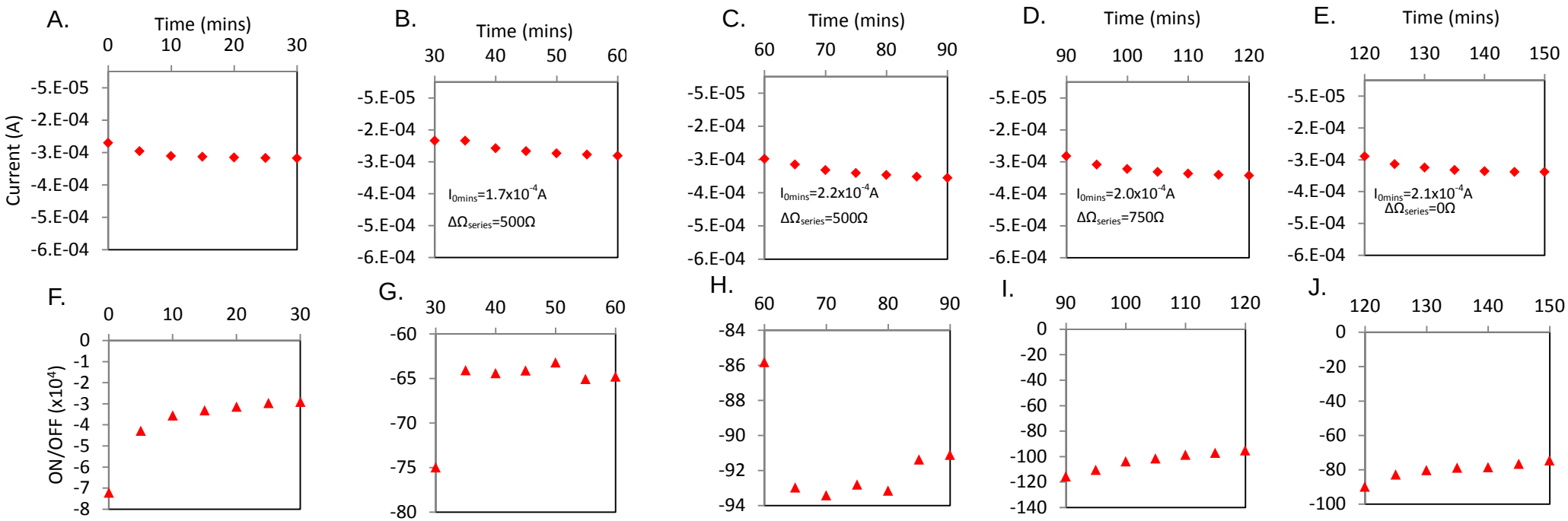


Figure C.7. Forward current increases in devices 20hours after electrode deposition over 30mins of testing. A. Forward current over 30mins after electrode deposition. Forward current over 30mins for a device 30mins after electrode deposition. C. Forward current over 30mins for a device 60mins after electrode deposition. D. Forward current over 30mins for a device 90mins after electrode deposition. E. Forward current over 30mins for a device 120mins after electrode deposition. The corresponding ON/OFF performance is presented in F,G,H,I and J respectively.

Table C.4.Extracted series resistance over the course of the experiment

	I_{0min} (A)	n_{0min}	Ωs_{start} (Ω)	I_{30min} (A)	n_{30min}	Rs_{30min} (Ω)	ΔRs(Ω)
Dev1	-2.2E-04	3.2	20500	-2.7E-04	3.3	18000	2500
Dev2	-1.8E-04	3.3	15000	-2.3E-04	3.3	14500	500
Dev3	-2.5E-04	3.3	23000	-3.1E-04	3.3	23500	-500
Dev4	-1.6E-04	3.3	15500	-1.7E-04	3.4	14750	750
Dev5	-2.3E-04	3.3	15500	-2.9E-04	3.3	15500	0

Appendix D. Supplementary Electrical Characterisation

D.1 Two Terminal Schottky Barrier Devices on Flexible PET Substrate

A roll-to-roll compatible, high throughput process for producing planarised transparent electrodes developed by Stapleton *et al.*[21] was investigated for incorporation with layered structures of metal and polymer. The lift-off technique was adapted for use with a silicon substrate, allowing the fabrication of devices on silicon and through a lift-off procedure using a resin adhesive the layered structures on the silicon master are transferred onto a flexible PET substrate. Production of devices on flexible substrate provides scope to utilise the unique material properties of the substrate in unique fabrication methods for potential transistor devices and application specific uses such as flexible displays. The schematic for the process can be seen in Figure 4.12.

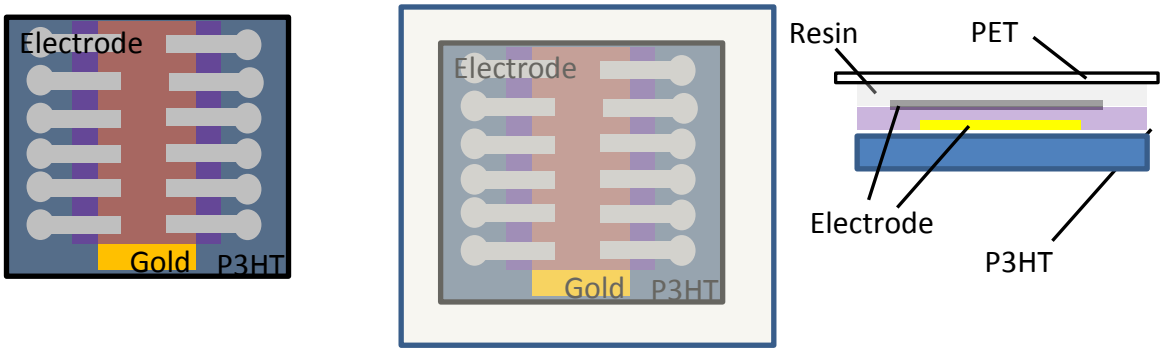


Figure D.1. Lift-off technique for the fabrication of layered structures on flexible PET substrate.

Devices were fabricated on silicon in nitrogen environment featuring a communal gold electrode with a spun cast 220nm P3HT thin film deposited and finished with an aluminium top electrode. The completed substrates were electrically characterised and statistics compiled to test the feasibility of the reel to reel

technology to produce devices. The device operational area was varied through graduated electrode width over the range 0.1mm-0.8mm examining for any area based effects. Figure 4.13 shows the yield of devices for layered structures with electrode thicknesses 30nm and the distribution of short circuit and open circuit devices over 48 devices on three substrates.

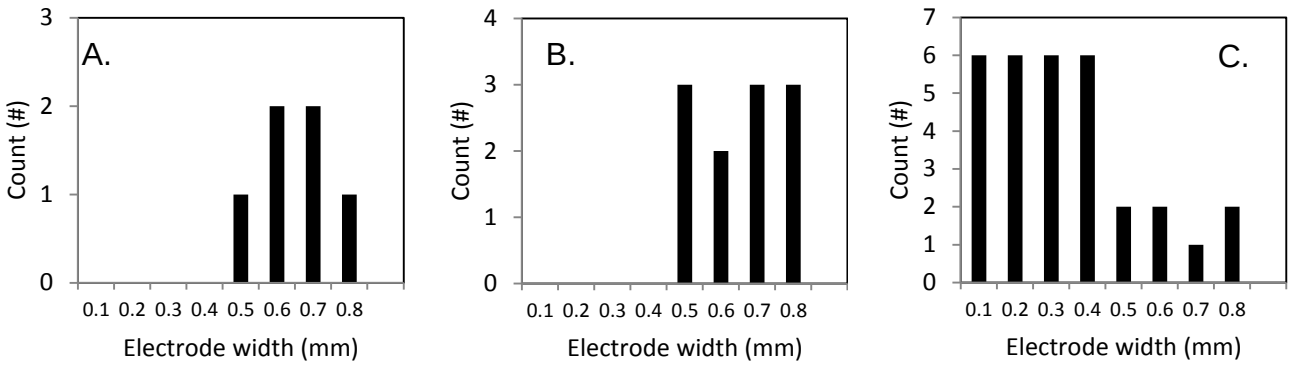


Figure D.2. Histogram plots for lift-off technique in the fabrication of layered device structures on flexible PET substrate.

Devices fabricated with 30nm electrodes show a device yield of 6 devices (12.5%) and were produced at electrode widths 0.5mm or greater. This result demonstrates the feasibility of fabricating layered structures on flexible substrates incorporating thin metal films using the reel to reel scalable lift off technique. 11 devices were observed to have short circuited with short circuits also appearing in devices with electrode widths 0.5mm or greater. Predominantly devices were seen to present as an open circuit with 32 devices. The operational area was examined under optical microscope to gain information on the failure mechanism and can be seen in Figure D.3.

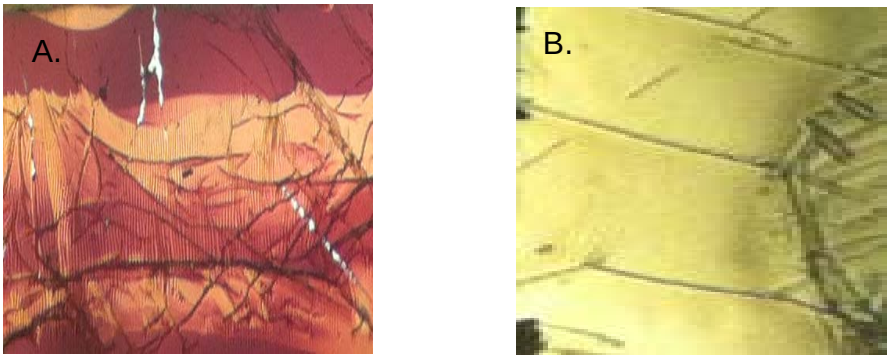


Figure D.3. Lift-off technique for the fabrication of layered structures on flexible PET substrate.

Electrodes processed through the lift-off technique are seen to have fracturing across the metal electrode. A likely result of bending forces produced during the peeling off of the PET substrate from the silicon master. The fracturing of the electrodes could lead to a loss of electrical continuity across the electrode and lead to the observation of an open circuit during electrical characterisation. The lift-off technique was analysed for devices fabricated with 100nm thick electrodes and can be seen in Figure D.4.

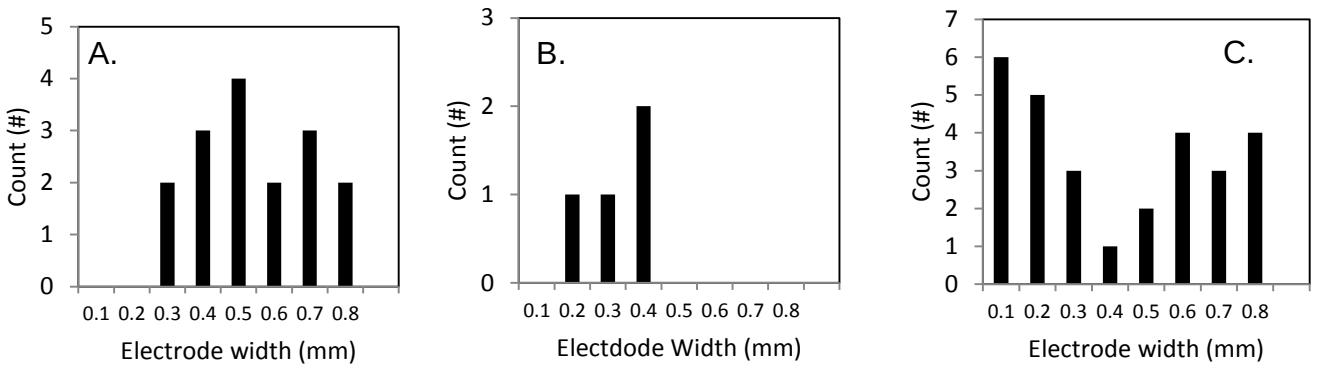


Figure D.4. Histogram plots for lift-off technique in the fabrication of layered device structures on flexible PET substrate.

Devices fabricated with 100nm electrodes show a device yield of 16 devices (33%) and were produced at electrode widths 0.3mm or greater. 4 devices were observed to have short circuited with short circuits appearing in devices with electrode widths 0.4mm or narrower. Predominantly devices were seen to present as an open circuit with 28 devices. It is speculated the increase in electrode thickness reduces the susceptibility to fractures through the electrode resulting in a reduction in open circuits and increase in functional devices. Observed short circuits may have been present on this silicon substrate prior to application of the lift-off technique may have occurred during the deposition of layers due to surface particulates on the silicon substrate. During processing the adhesion of the layered structure on the silicon relative to the adhesion on the resin is of key importance. It was observed

that cleaned pristine silicon hampered the successful transfer between the silicon and PET devices resulting in partial transfer of the deposited layers on the resin adhesive and incomplete devices. To this end, surface modification of the silicon surface may be a viable avenue of future work to improve yields and the scope of the technology. Furthermore, the interaction between the binding and the polymer may have resulted in diffusion into the operational area at the edge of the electrodes increasing the resistance potentially explaining the poor yields of narrow electrode devices.

Devices were successfully fabricated using a lift-off technique allowing for layered structures incorporating thin metal films to be fabricated on flexible plastic substrates. Low device yields were largely due to the formation of open circuits between the layered structure, the likely result of fracturing of metal electrodes and loss electrical continuity across the electrode surface. Despite the low yields, several promising avenues have been identified to help realise the technology.

Appendix E. CNC Machine Cutting

E.1. Reducing Operational Area

With three terminal Schottky barrier devices featuring P3HT polymer as the active channel showing no channel enhancement during device testing several measures were taken to improve the three terminal platform to improve potential three terminal behaviour. Reducing the OFF state current between the source and the drain increases the scope for observable field enhancement being observed during applied gate potential. Reducing the operational area of the structure is expected to reduce the OFF state current produced. The resolution and capabilities of the manually aligned machine cutting procedure were examined in order to reduce the

operational area of the resulting machine cut two terminal devices. Devices were fabricated with inverted electrode pattern with 30nm gold electrode evaporated at 1 Å.s^{-1} at 10^{-6} Torr. 1% w/v PCDTBT in 1,2-dicholorbenzene solution was drop cast with a 10µL aliquot deposited on the polycarbonate-gold electrode surface in controlled nitrogen atmosphere. Films were left for 60mins and then transferred onto a hot plate and annealed at 150°C to remove residual solvent. A gold electrode was deposited at 1 Å.s^{-1} at 10^{-6} Torr. The width of the trench machine cut into device substrates was increased as seen in Figure E.1A. shows a schematic representation of the machine cut before optimisation and the resulting 3 device forward current average is seen in Figure E.1B. After optimisation to increase the trench width a width of 65mm was achieved and can be seen in Figure E.1C. The resulting three device average forward current can be seen in Figure E.1D.

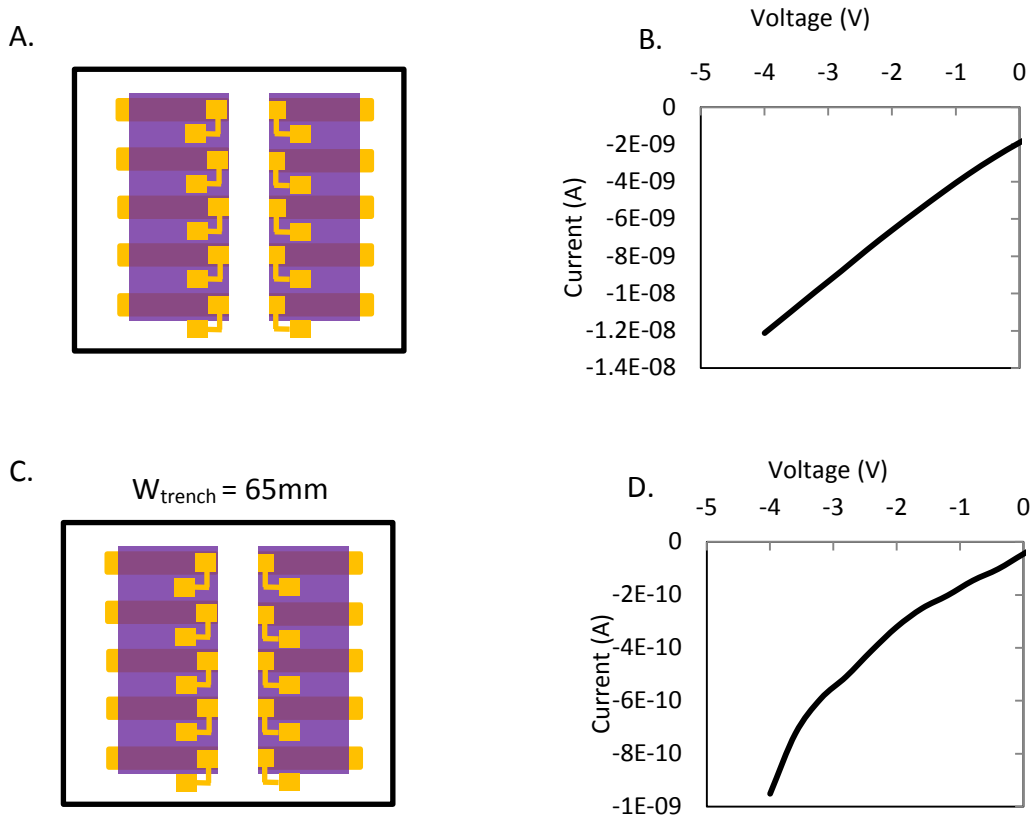


Figure E1. Reduction of operational area through increased trench width. A. Initial machine cut trench with width w= 42mm. B. 3 device average forward current with trench width = 42mm C Reduced operating area device with increased trench width of 62mm. C. 3 device average forward current with trench width= 65mm.

Drop cast PCDTBT devices with machine cut trench widths of 42mm produce a forward current magnitude of 1.2 x 10^{-8}A at -4V with a calculated operational area of 1.3x10^{-6} m^2. The equivalent device with P3HT discussed in § 7.X produces a drain current of -4 x 10^{-6} A. The reduction in drain current is attributed to the lower intrinsic conductivity of the PCDTBT which should improve the visibility of the enhancement channel induced drain currents under electrical characterisation. With a trench width of 65mm devices produce a forward current of -1 X 10^{-9} A with an operational area of 9 x 10-^{7}m^2. With the wider machine cut trench a reduction in forward current is observed the order of a magnitude of the total drain current. The device of that area is decreased by 30 % and forward current is reduced to 8% of the previous total current. The lack of a direct relationship between decreasing area and decreasing forward current may be attributed to variation in the thickness of compared devices in PCDTBT material.

Further reductions in the operational area are limited by the electrode pattern of two terminal devices. In order for contact pads to be accessible during device testing an electrode pattern with a contact pad with narrow interconnect was designed. Due to design consideration the narrow interconnect allows a reduction in the cross sectional overlap at the electrode edge. A thickness distribution was determined through C-AFM in § 5.X which reduced thickness towards the electrode edge, in order to limit short circuit occurrences and improve device yields reducing the cross sectional edge is considered favourable. At larger trench widths (W_{trench}> 70mm) the inter-connect is removed by the machine cutting path and device testing not capable. For further operational area reductions to occur an alternative pattern will need to be incorporated into the three terminal electrical platform to allow wider trench widths and reduced operational areas to be achieved. The three terminal platform with manually machine cutting procedure allows for control over the device operational area through the increase in programmed machine cut trench width. Further improvements in operating area require an alternate electrode pattern with interconnect positioning away from the machine cut edge allowing for wider cut paths programmable.

Appendix F. Lateral Channel Charge Distribution

Assuming a constant voltage potential profile across the length of the channel the charges in the channel can be described by Equation F.1.

$$Q_{channel} = -C_{Insulator\,(V_{GS}-V_T)} \qquad \text{Equation F.1}$$

Assuming a non-uniform distribution of potential and charges across the semiconductor-dielectric interface requires an adaptation with an effective capacitance at the interface describing the capacitance at a point and is described in equation F.2.

$$C_{Insulator} \Rightarrow C_{Insulator\_effective} = C_{Insulator\_effective}\,(V_{GS}, y) \qquad \text{Equation F.2}$$

Using the Poisson equation and boundary condition for the electric field over which to integrate over the boundary conditions and an equation for the electric field can be described by Equation F.3.

$$E = \sqrt{\frac{2CD_h}{\mu_h}}\,tan\left[\sqrt{\frac{C\mu_h}{2D_h}}(x-L)\right] \qquad \text{Equation F.3}$$

The influence of the electric field in inducing a change in energy levels by the resulting band bending is described through Equation F.4.

$$\Delta V_{channel} = -\int_0^L E dx = -\sqrt{\frac{2CD_h}{\mu_h}}\int_0^L tan\left[\sqrt{\frac{C\mu_h}{2D_h}}(x-L)\right]dx = -\frac{2D_h}{\mu_h}log\left(cos\left[\sqrt{\frac{C\mu_h}{2D_h}}L\right]\right)$$

Equation F.4

With the density of charge induced at the charge interface described by Equation F.5.

$$p = \frac{\varepsilon_\pi \varepsilon_0}{q}\frac{\partial E}{\partial x} = \frac{C\varepsilon_\pi\varepsilon_0}{q}\left(tan\left[\sqrt{\frac{C\mu_h}{2D_h}}(x-L)\right]^2 + 1\right) \qquad \text{Equation F.5}$$

And the total capacitance described by Equation F.6

$$\frac{\varepsilon_{ins}}{\varepsilon_{\pi}} E_{ins} = \sqrt{\frac{2CD_h}{\mu_h}} tan\left[\sqrt{\frac{C\mu_h}{2D_h}}(0 - L)\right] \qquad \text{Equation F.6}$$

References

1. Yuan, Y. and T.R. Lee, *Contact Angle and Wetting Properties*, in *Surface Science Techniques*, G. Bracco and B. Holst, Editors. 2013, Springer Berlin Heidelberg. p. 3-34.
2. Richardson, O.W. and K.T. Compton, *THE PHOTOELECTRIC EFFECT.* Science, 1912. **35**(907): p. 783-784.
3. Richardson, O.W., *THE EMISSION OF ELECTRONS FROM TUNGSTEN AT HIGH TEMPERATURES: AN EXPERIMENTAL PROOF THAT THE ELECTRIC CURRENT IN METALS IS CARRIED BY ELECTRONS.* Science, 1913. **38**(967): p. 57-61.
4. Crowell, C.R., *The Richardson constant for thermionic emission in Schottky barrier diodes.* Solid-State Electronics, 1965. **8**(4): p. 395-399.
5. Norde, H., *A modified forward I-V plot for Schottky diodes with high series resistance.* Journal of Applied Physics, 1979. **50**(7): p. 5052-5053.
6. Sato, K. and Y. Yasumura, *Study of forward I-V plot for Schottky diodes with high series resistance.* Journal of Applied Physics, 1985. **58**(9): p. 3655-3657.
7. Cheung, S.K. and N.W. Cheung, *Extraction of Schottky diode parameters from forward current-voltage characteristics.* Applied Physics Letters, 1986. **49**(2): p. 85-87.
8. Sullivan, J.P., et al., *Electron transport of inhomogeneous Schottky barriers: A numerical study.* Journal of Applied Physics, 1991. **70**(12): p. 7403-7424.
9. Bolognesi, A., et al., *Large drift-diffusion and Monte Carlo modeling of organic semiconductor devices.* Synthetic Metals, 2003. **138**(1–2): p. 95-100.
10. Nagel, L. and R. Rohrer, *Computer analysis of nonlinear circuits, excluding radiation (CANCER).* Solid-State Circuits, IEEE Journal of, 1971. **6**(4): p. 166-182.
11. Enz, C.C. and C. Yuhua, *MOS transistor modeling for RF IC design.* Solid-State Circuits, IEEE Journal of, 2000. **35**(2): p. 186-201.
12. Bartzsch, M., et al., *Device and circuit simulation of printed polymer electronics.* Organic Electronics, 2007. **8**(4): p. 431-438.
13. Hayati, M., A. Rezaei, and M. Seifi, *CNT-MOSFET modeling based on artificial neural network: Application to simulation of nanoscale circuits.* Solid-State Electronics, 2010. **54**(1): p. 52-57.
14. NeŠpůrek, S. and P. Smejtek, *Space-charge limited currents in insulators with the Gaussian distribution of traps.* Czechoslovak Journal of Physics B, 1972. **22**(2): p. 160-175.
15. Giulianini, M., et al., *Current-voltage characteristics of poly(3-hexylthiophene) diodes at room temperature.* Applied Physics Letters, 2009. **94**(8): p. 083302.
16. Shen, X.M., et al., *Space-charge-limited currents in GaN Schottky diodes.* Solid-State Electronics, 2005. **49**(5): p. 847-852.
17. Chiguvare, Z., J. Parisi, and V. Dyakonov, *Current limiting mechanisms in indium-tin-oxide/poly3-hexylthiophene/aluminum thin film devices.* Journal of Applied Physics, 2003. **94**(4): p. 2440-2448.

18. Chiguvare, Z. and V. Dyakonov, *Trap-limited hole mobility in semiconducting poly(3-hexylthiophene).* Physical Review B, 2004. **70**(23): p. 235207.